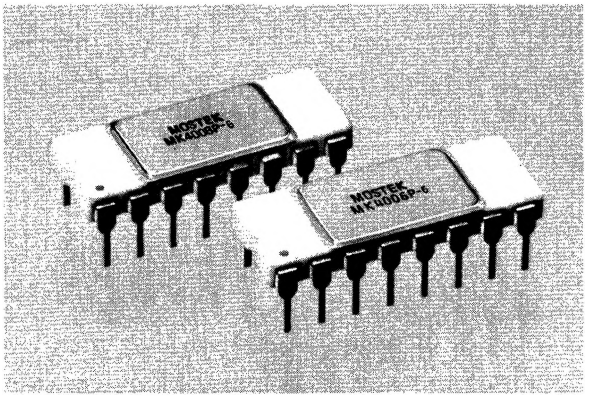
MK 4006 P-6
MK 4008 P-6

1024x1 BIT DYNAMIC
MOS Random Access Memory

MOSTEK

FEATURES:

- ☐ TTL/DTL compatible inputs
- ☐ No clocks required
- ☐ Access time:
  MK 4006 P–6 under 400 ns
  MK 4008 P–6 under 500 ns
- ☐ Standby power: under 50 mW
- ☐ 16-pin standard CDIP
- ☐ Supply voltage: +5V and −12V



DESCRIPTION

This is a family of MOS dynamic 1024x1 random-access memories having identical functional characteristics, differing only in speed. Access time in the MK 4006 P-6 is less than 400 ns; in the MK 4008 P-6 less than 500.

Full address decoding is provided internally. Information is read out non-destructively (NDRO) and has the same polarity as the input data.

TTL/DTL compatibility at all inputs allows economical use in small systems by eliminating the need for special interface circuitry. Large main-memory applications also benefit from the low drive-voltage swings as well as the packing density afforded by the standard 16-pin dual-in-line packaging and low standby power.

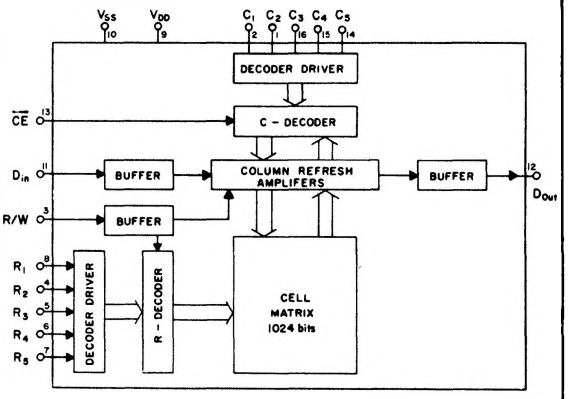
The internal memory element of this RAM is a capacitance, and refreshing must be periodically initiated (see TIMING). However, all internal decoding and sensing is static, so that precharging or clocking normally associated with dynamic memories is not required. From the user's viewpoint, memory control and addressing are essentially those of a static device.

Noise suppression measures normally employed in DTL or TTL systems are sufficient. High voltage input swings and high peak-current line drivers are unnecessary for driving memory inputs, and the memory itself does not exhibit large supply current transients.

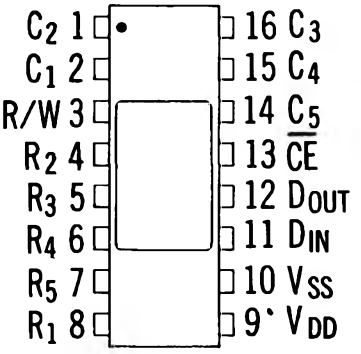
Data output is single-ended to minimize propagation delay. Output current is sourced from V_{SS} (+5V), and easily sensed using readily available components. A logic 1 at the output terminal appears as a 5,000 Ohm resistor (MK 4006) to +5V; a logic 0 as an open circuit.

The performance of this RAM is made possible by Mostek's ion-implantation process. In addition to offering low threshold voltages for TTL/DTL compatibility and utilizing conventional P-channel processing, ion-implantation allows both enhancement (normally OFF) and depletion (normally ON) MOS transistors to be fabricated on the same chip. By replacing conventional MOS load resistors with constant-current depletion transistors, operational speeds and functional density are increased.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... +0.3 to −20V

Operating Temperature ..... 0°C to +70°C

Storage Temperature Range ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS

(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
V_{SS}	Supply Voltage		+4.75		+5.25	V	
V_{DD}	Supply Voltage		−11.4		−12.6	V	
V_{IL}	Input Voltage, Logic 0				+0.8	V	
V_{IH}	Input Voltage, Logic 1		$V_{SS}-1$		V_{SS}	V	
V_{SB}	Standby Supply Voltage (Fig. 4)		$V_{SS}-4$		$V_{SS}-6$	V	Note 1

RECOMMENDED AC OPERATING CONDITIONS[2]

(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	400		500		ns	
t_{WC}	Write Cycle Time (Fig. 2)	650		900		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{WP}	Write Pulse Width (Fig. 2)	250		400		ns ns	t_{AW}=400 ns t_{AW}=500 ns
t_{AW}	Address-to-Write Delay (Fig. 2)	400		500		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	300		400		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{RDLY}	Refresh Time (Fig. 3)		2		2	ms	See Note 3.
t_{CDPD}	Chip-Disable-to-Power-Down Delay (Fig. 4)	200		200		ns	See Note 1 See Note 4

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C $\leq T_A \leq$ 70°C unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At T_A=0°C		32		32	mA	Output
	At T_A=70°C		27		27	mA	Open
P_{SDBY}	Power Dissipation, Standby		50		50	mW	$V_{SS}-V_{DD}$ = 5V; Note 1
I_{IH}	Input Current, Logic 1. Any Input	−5	+5	−5	+5	μA	$V_I=V_{SS}-1V$
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	−5	+5	μA	V_I=0.8V
I_{OH}	Output Current, Logic 1	1.0		0.8		mA	Note 5
I_{OL}	Output Current, Logic 0		5		5	μA	

AC ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{DD} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
t_{ACCESS}	Read Access Time (Fig. 1 & 1-A)		400		500	ns	Note 2
t_{CE}	Chip Enable Time (Fig. 1A & 5)		350		450	ns	Note 2
t_{CD}	Chip Disable Time (Fig. 1A & 5)		350		450	ns	
C_I	Input Capacitance, Any Input		5.0		5.0	pF	$T_A=25°C$; $V_I=V_{SS}$; f=1MHz
C_O	Output Capacitance		10		10	pF	$T_A=25°C$; $V_O=V_{SS}-5V$; f=1MHz
C_{DD}	V_{DD} Capacitance		75		75	pF	$T_A = 25°C$; Note 6

Random Access Memories

NOTES:

(1) Applies to MK 4006-6 and MK 4008-6 only.

(2) Measurement Criteria: Input voltage swing, all inputs: 0.8V to $V_{SS} - 1$
Input rise and fall times: 20 ns
Measurement point on input signals: +1.5V above ground
Measurement point on output signal: +60 mV above ground, using a load circuit of a 200 ohm resistor in parallel with a 100 pF capacitance connected to ground.

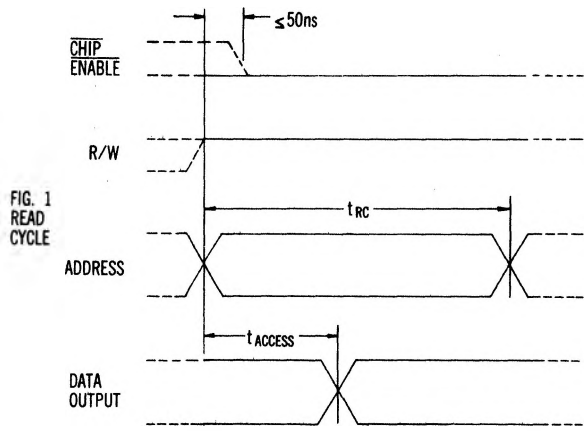
(3) t_{RDLY} is the time between refresh cycles for a given row address.

(4) The rise time of V_{IH} must not be faster than 20 ns.

(5) Steady-state values. (Refer to Fig. 1A for clarification)

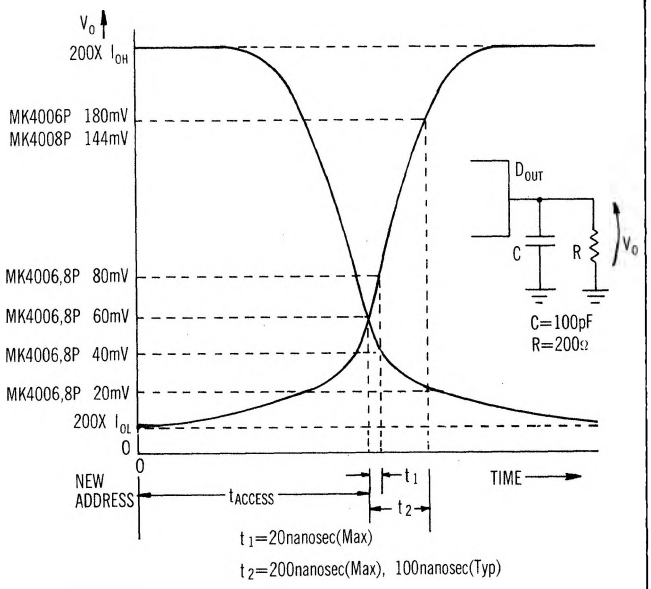
(6) Average capacitance of the V_{DD} terminal relative to the V_{SS} terminal. Measured by switching the V_{DD} terminal from OV to —12V with an applied $V_{SS} = 5V$. Peak I_{DD} is observed and the circuit replaced by a capacitance which yields the same peak current as the circuit under test.

TIMING (Note 2)



READING (Fig. 1)

Reading is accomplished with the Read/Write input held high. Data output directly follows the application of an address. As long as the address is unchanged and the chip enabled, data output will remain valid until the next refresh cycle. Input addresses can be changed as soon as output data is accessed. Any address can be applied repetitively without degrading stored data, providing that the refresh period of 2 ms is observed.



ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4006 P and the MK 4008 P.

TIMING
(Note 2)

WRITING (Fig. 2)

Writing is accomplished by bringing the Read/Write input low with valid data present at the data input and the Chip-Enable input low (chip enabled). Following the return of the Read/Write line to a high state, new address and input data can be applied. If a read-after-write operation is desired, valid data will appear at the output within one read access time following the rising edge of the Write Pulse. Read-modify-write operation is easily achieved by delaying the Write Pulse until data has been read and modification is complete.

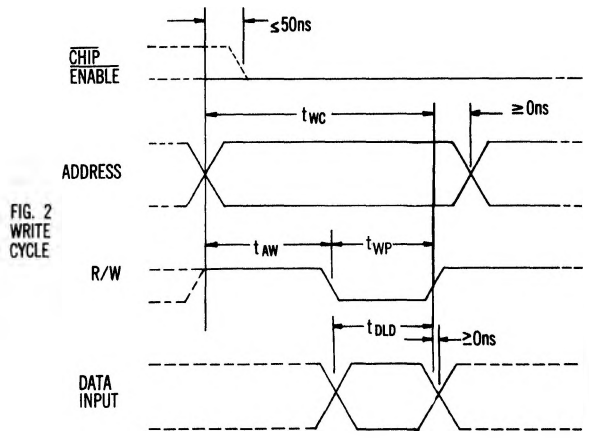


FIG. 2 WRITE CYCLE

REFRESHING (Figs. 2 & 3)

The dynamic memory cell employed in the MK 4006 P and MK 4008 P will not store data indefinitely. Stored data must be written back into the cell at least once every 2 ms. Rewriting is accomplished internally without the need to reapply external data. This rewriting operation is called *refreshing.*

Refreshing of the MK 4006 P and MK 4008 P is accomplished during both *write cycles* and *refresh cycles.* During a write cycle the state of the Row Address (R_1-R_5) determines which of the 32 memory matrix rows will be internally refreshed. An entire row (32 bits) is refreshed during one write cycle. Since it is difficult in practice to assure that each of the 32 possible R addresses is associated with a write cycle in every 2 ms period, a separate refresh cycle is normally employed.

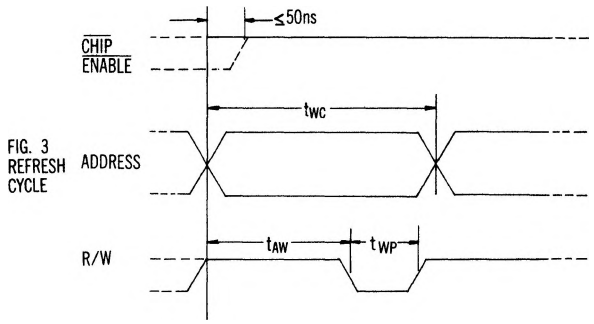


FIG. 3 REFRESH CYCLE

The refresh cycle is identical to the write cycle except that the chip is disabled while the Read/Write line is pulsed. Disabling the chip removes the data output and prevents data at the data input from being written into the memory. An entire refresh cycle consists of 32 address changes and associated write pulses, involving a total time of approximately 20 microseconds.

STANDBY MODE (Fig. 4)

Power dissipation of the MK 4006-6 P and MK 4008-6 P can be reduced below 50 mW without loss of stored data by lowering the V_{DD} supply voltage to system ground (V_{SS}-5V). Figure 4 illustrates the proper input conditions that should be observed when reducing V_{DD}. If the standby mode is maintained as long as 2 milliseconds, the V_{DD} supply should be returned to −12V and a refresh cycle initiated. Read or write cycles can commence immediately following the return of V_{DD} to −12V.

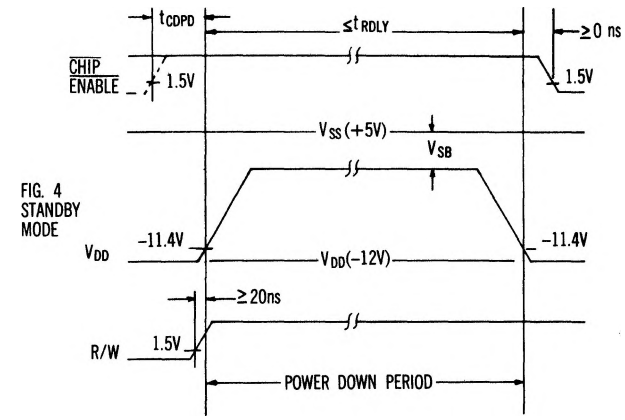


FIG. 4 STANDBY MODE

TIMING
(Note 2)

CHIP ENABLING (Fig. 5)

The negative-going $\overline{CE}$ enables the chip, and output data becomes valid within t_{CE} time. Return of the $\overline{CE}$ input to logic 1 disables the chip; data out remains for t_{CD} time.

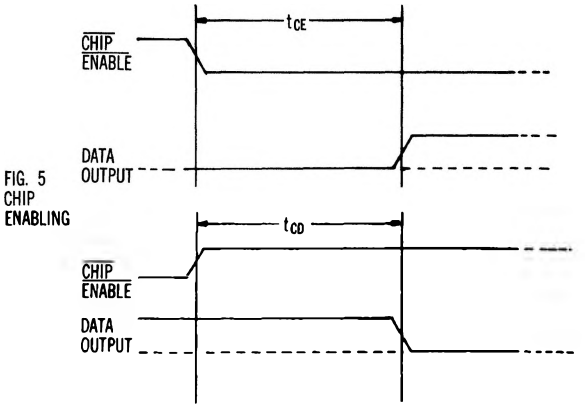


FIG. 5 CHIP ENABLING

TESTING CONSIDERATIONS

For a complete discussion of testing this memory, see Mostek's Applications Note AN-103.

The functional diagram (Fig. 6) indicates signal flow for selected row and column.

A simplified listing of functional tests is shown in Table 1. (high = Logic 1; low = Logic 0)

Tests are performed in an address sequence which requires the maximum number of changes in the row and column decoders between addresses. Addressing Rows 0 through 31 is accomplished by using the binary equivalent of the row address. The internal organization of the memory matrix requires the logic shown in Fig. 7 for column addresses; this logic provides the necessary conversion from inary equivalent to column address.

Fig. 6

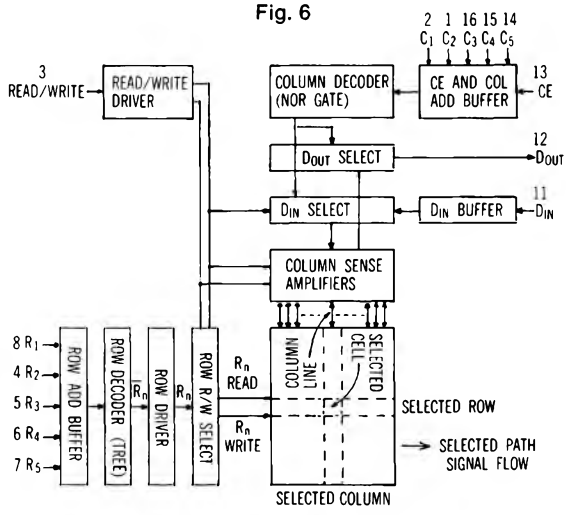


Fig. 7

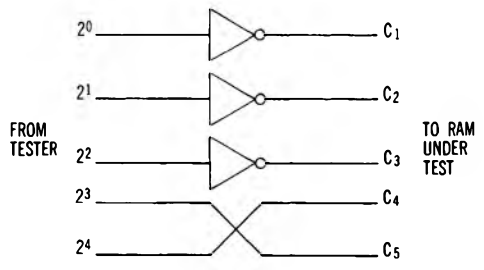
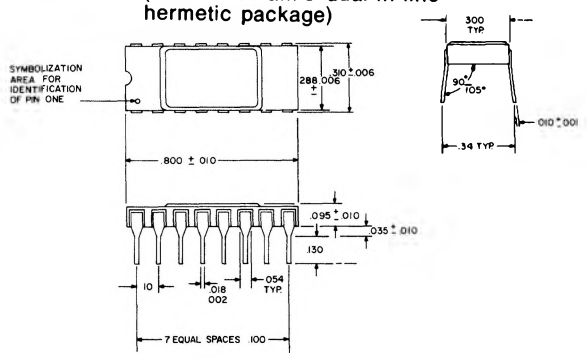


TABLE 1: FUNCTIONAL TESTS (SIMPLIFIED)

TEST DESC.	TEST SEQ.	OPER.	CHIP ENABLE	DATA INPUT	COMPARE DATA
Bit & Decoder Test[1]	First	Write	E	Parity	
	Next	Read	E		Parity
Column Shorts & No Write During Disable	First	Write	E	V-Bar	
	Next	Write	D	$\overline{\text{V-Bar}}$	
	Next	Read	E		V-Bar
Row Shorts, No Read During Disable, & Max. Power	First	Write	E	H-Bar	
	Next	Read	D	1	0
	Next	Read	E	0	H-Bar
Access Time, Refresh, Write Cycle, & Standby[1]	First	Write, Write	E	V-Bar, $\overline{\text{V-Bar}}$	
	Next	Delay	D	0	
	Next	Read	E		$\overline{\text{V-Bar}}$
Disturb Test	First	Write Row of 1's	E	1	
	Next	Write Adj. Row with 0's	E	0	
	Next	Continue Writing Same Row for Max. Refresh Delay	E	0	
	Next	Read original Row of 1's	E		1

1. Test performed as shown and repeated with complementary data.

PACKAGE (16-lead ceramic dual-in-line hermetic package)



ORDERING INFORMATION

MK 4006 P–6 1024x1 RAM/w/400 ns access time with power down
MK 4008 P–6 1024x1 RAM/w/500 ns access time with power down

APPLICATION

SENSE AMPLIFIERS FOR MK 4006/4008 RAM's

Since the interface circuitry used to convert memory signals to system logic levels strongly influences system access times, this circuitry should always be designed to meet the speed and cost requirements of the particular application.

Fig. 1-A (See "Timing") is shown to assist in the design of such amplifiers. This figure shows output voltage (across a specified load) vs. time from application of new address with several points indicated where specified voltage levels are referenced to specific times. Although all the various access times vs. output current levels cannot be shown, a few guidelines are given for interpolation between the specified points.

In Fig. 1-A, the two points at t_{access} + 20 nsec give the minimum "1" level and the maximum "0" level for this particular time (80 mV and 40 mV respectively). At t_{access} + 200 nsec, voltage levels are specified for the 90% and 10% points of the minimum "1" and maximum "0" levels.

INTERPOLATION

These interpolation guidelines are selected to give the designer a high level of confidence in his sense amplifier design.

From O to 1: This portion of the access curve can be estimated by two linear portions: (1) from the 60 mV to the 80 mV level; and (2) from the 80 mV level to 180/144 mV level.

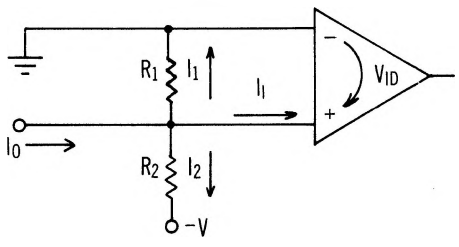
From 1 to O: This portion of the access curve can be estimated by a semi-logarithmic plot decreasing 20 mV for each decade or 10 nsec of time added to t_{access}, with the end points being 60 mV at 2 nsec and 20 mV at 200 nsec.

EXAMPLE: Let us consider how this data can be used in a sense amplifier design utilizing the 75107/108 Dual-Line-Receiver-and-Driver.

The manufacturer's data sheet for this circuit shows us that at strobe time, three conditions of the line receiver can exist: (1) the input voltage differential can be more positive than 25 mV, resulting in a logic 1 at the output (Input differential voltage is referenced to the inverting terminal); (2) the input differential can be more negative than 25 mV, resulting in a logic O at the output; (3) the input differential is less than 25 mV (absolute value), which will result in an output of an undetermined state. In other words, the line receiver has a 50 mV "window" centered around zero, and a signal must fall outside this window to provide reliable information at the output.

The standard configuration for using the 75107/108 as a sense amp is shown in Fig. 8 with the voltage and current conventions used in this analysis.

FIG. 8: Illustrating use of 75107/108 Line Receivers as sense amplifiers for the MK 4006/4008 P.



From the worst-case access at the *chip* level, one can use the interpolation technique described above to determine maximum "O" current level [I_{OLC}(MAX)] and the minimum "1" current level [I_{OH}(MIN)].

However, to use a worst-case approach to this design, in addition to the chip's characteristics, one must include in the "O" level current the effect of leakage from all outputs that are wired together. Also the input currents required by the 75107/108 (75 mA and 10 mA) must be included. Let us call this I_{OLT}(MAX):

$$I_{OLT}(MAX) = I_{OLC}(MAX) + (N\text{-}1)\ (5\ \mu A) \quad [1]$$

where N = number of outputs wired together

Using the maximum zero level at the line receiver input ($V_{ID} \leq -25mV = V_{ID}^{-}$), the following equation is derived:

$$I_{OLT}(MAX) = I_1 - I_2 + I_{IL}(MIN)$$

and $I_{IL}(MIN) = O\ \mu A$ [2]

therefore:

$$I_{OLT}(MAX) = \frac{V_{ID}^{-}}{R1} + \frac{V + V_{ID}^{-}}{R2} \quad [3]$$

Using the minimum "1" level at the line receiver input ($V_{ID} \geq +25\ mV = V_{ID}^{+}$), the equation becomes

$$I_{OH}(MIN) = I_1 - I_2 + I_{IH}(MAX) \quad [4]$$

and $I_{IH}(MAX) = 75\ \mu A$

$$I_{OH}(MIN) = \frac{V_{ID}^{+}}{R1} + \frac{V + V_{ID}^{+}}{R2} + 75\ \mu A \quad [5]$$

Solving these equations ([3] and [5]) simultaneously yields R1 and R2.

As an example, assume a memory system with 4 outputs wired-ORed to a sense amplifier, requiring a chip access time of 460 nsec. Then the associated current and resistor values are:

$I_{OLT}(MAX) = 152.3\ \mu A + 3\ (5\ \mu A) = 167.3\ \mu A$

$I_{OH}(MIN) = 511.12\ \mu A$

Therefore:

$R1 = 190\ \Omega$

$R2 = 16.5\ K\Omega$

Sense amplifiers vary from the very fast, low-threshold types to the slower, high-threshold kind. The ideal choice will depend on the application. Fig. 1-A and the guidelines in this note are intended to help the designer tailor his sense amplifier design to meet the speed and cost requirements of his particular application.

It should also be noted that a portion of the output current from the memory chip is used to charge the capacitance on the data output. If the output impedance differs greatly from the specified load, this current must also be calculated.