MOSTEK®

Z80 MICROCOMPUTER

Central Processing Unit

MK3880

FEATURES

- □ The Z80 is fully software compatible with the 8080A CPU. The 78 instructions of the 8080A are a subset of the Z80's 158 instructions.
- □ The extensive instruction set includes relative and indexed addressing, block searches and block transfers, word, byte, and bit data operations.
- □ The architecture provides duplicate sets of general purpose Flag and Index registers to allow background/ foreground programming and easier single level interrupt processing and to facilitate array and table processing.
- □ On chip Dynamic memory refresh counter
- □ Single +5 V supply
- □ Single phase system clock
- □ Vectored interrupt handling system. This system allows for a Daisy Chain arrangement of a priority interrupt scheme with little if any additional hardware.

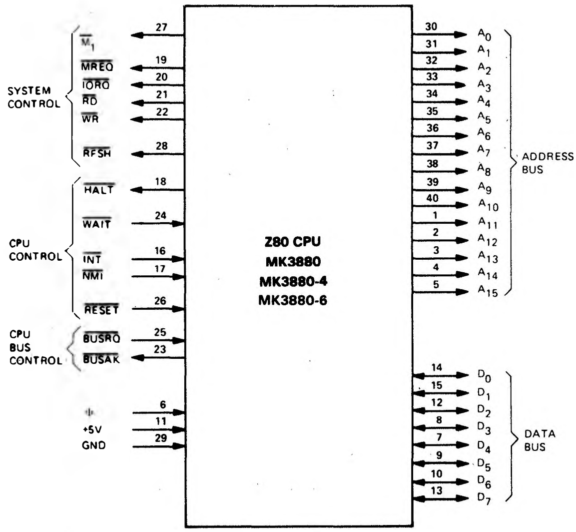
INTRODUCTION

The Mostek Z80 family of components is a significant advancement in the state-of-the-art of microcomputers. These components can be configured with any type of standard semiconductor memory to generate computer systems with an extremely wide range of capabilities. For example, as few as two LSI circuits and three standard TTL MSI packages can be combined to form a simple controller. With additional memory and I/O devices, a computer can be constructed with capabilities that only a minicomputer could previously deliver. This wide range of computational power allows standard modules to be constructed by a user that can satisfy the requirements of an extremely wide range of applications.

The Z80 Central Processing Unit is the heart of the Z80 family. It provides arithmetic and bus control to operate with the bussed peripheral controllers such as the Parallel I/O, Serial I/O, Counter/Timer, and Direct Memory Access Circuits. The Z80-CPU utilizes N channel silicon gate depletion load technology and is packaged in a 40 pin DIP.

Z80 PIN CONFIGURATION

Figure 1



Z80-CPU PIN DESCRIPTION

The Z80-CPU is packaged in an industry-standard 40 pin Dual In-Line Package. The I/O pins are shown in Figure 1, and the function of each is described below.

A_0-A_{15} (Address Bus)	Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes), data exchanges, and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to select up to 256 input or 256 output ports directly. A_0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.
D_0-D_7 (Data Bus)	Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

$\overline{M_1}$
(Machine Cycle one)

Output, active low, $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, $\overline{M_1}$ is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH, or FDH. $\overline{M_1}$ also occurs with $\overline{IORQ}$ to indicate an interrupt acknowledge cycle.

$\overline{MREQ}$
(Memory Request)

Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$
(Input/Output Request)

Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An $\overline{IORQ}$ signal is also generated with an $\overline{M_1}$ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during $\overline{M_1}$ time while I/O operations never occur during $\overline{M_1}$ time.

$\overline{RD}$
(Memory Read)

Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$
(Memory Write)

Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$
(Refresh)

Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories. A_7 is a logic zero and the upper 8 bits of the Address Bus contain the I Register.

$\overline{HALT}$
(Halt state)

Output, active low. $\overline{HALT}$ indicates that the CPU has executed a $\overline{HALT}$ software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$*
(Wait)

Output, active low. $\overline{WAIT}$ indicates to the Z80-CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

$\overline{INT}$
(Interrupt Request)

Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the $\overline{BUSRQ}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{IORQ}$ during M_1 time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 8 of the Technical Manual, which is included in section IV of this data book.

$\overline{NMI}$

Input, negative edge triggered. The non maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z80-CPU to restart to location 0066_H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a $\overline{BUSRQ}$ will override an $\overline{NMI}$.

RESET

Input, active low. $\overline{RESET}$ forces the program counter to zero and initializes the CPU. The CPU initialization will:

1) Disable the interrupt enable flip-flop
2) Set Register I = 00H
3) Set Register R = 00H
4) Set Interrupt Mode 0

During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state. No refresh occurs.

$\overline{BUSRQ}$
(Bus Request)

Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control buses to a high impedance state as soon as the current CPU machine cycle is terminated.

$\overline{\text{BUSAK}}$* Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Φ Single phase system clock.

*While the Z80-CPU is in either a $\overline{\text{WAIT}}$ state or a Bus Acknowledge condition, Dynamic Memory Refresh will not occur.

For further details on this device, please consult the MK3880 Z80 CPU Technical Manual, included in Section IV.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... Specified Operating Range
Storage Temperature .... −65°C to +150°C
Voltage on Any Pin with Respect to Ground .... −0.3 V to +7V
Power Dissipation .... 1.5 W

All ac parameters assume a load capacitance of 50 pF max.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{ILC}	Clock Input Low Voltage	-0.3		0.8	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-.6		V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.8 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −250 μA
I_{CC}	Power Supply Current			150*	mA	
I_{LI}	Input Leakage Current			±10	μA	V_{IN} = 0 to V_{CC}
I_{LO}	Tri-State Output Leakage Current in Float			±10	μA	V_{OUT} = 0.4 V to V_{CC}

*200 mA for −4, −10 or −20 devices

CAPACITANCE

T_A = 25°C, f = 1 MHz unmeasured pins returned to ground

SYMBOL	PARAMETER	MAX	UNIT
$C\Phi$	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, Unless Otherwise Noted

SIGNAL	SYMBOL	PARAMETER	3880		3880-4		3880-6	
			MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
Φ	t_c	Clock Period	400	[12]	250	[12]	165	[12]
	$t_w(\Phi H)$	Clock Pulse Width, Clock High	180	(D)	110	(D)	65	(D)
	$t_w(\Phi L)$	Clock Pulse Width, Clock Low	180	2000	110	2000	65	2000
	$t_{r,f}$	Clock Rise and Fall Time		30		30		20
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145		110		90
	$t_{F(AD)}$	Delay to Float		110		90		80
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		[13]		[24]	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		[14]		[25]	
	t_{ca}	Address Stable From $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		[15]		[26]	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		[16]		[27]	
D_{0-7}	$t_{D(D)}$	Data Output Delay		230		150		130
	$t_{F(D)}$	Delay to Float During Write Cycle		90		90		80
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		35		30	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge at Clock During M2 to M5	60		50		40	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		[17]		[28]	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		[18]		[29]	
	t_{cdf}	Data Stable from $\overline{WR}$	[7]		[19]		[30]	
	t_H	Input Hold Time	0		0		0	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low	20	100	20	85	20	70
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100		85		70
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100		85		70
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		[20]		[20]	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		[21]		[21]	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90		75		65
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110		85		70
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100		85		70
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock Clock, $\overline{IORQ}$ High		110		85		70
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100		85		70
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130		95		80
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High	15	100	15	85	15	70
	$t_{DH\overline{\Phi}(BD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110		85		70
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80		65		60
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90		80		70
	$t_{DH\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100		80		70
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		[22]		[22]	

NOTES:

A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

[Cont'd. on next page].

SIGNAL	SYMBOL	PARAMETER	3880 MIN (ns)	3880 MAX (ns)	3880-4 MIN (ns)	3880-4 MAX (ns)	3880-6 MIN (ns)	3880-6 MAX (ns)
$\overline{\text{M1}}$	$t_{DL(M1)}$	$\overline{\text{M1}}$ Delay From Rising Edge of Clock M1 Low		130		100		80
	$t_{DH(M1)}$	$\overline{\text{M1}}$ Delay From Rising Edge of Clock M1 High		130		100		80
$\overline{\text{RFSH}}$	$t_{DL(RF)}$	$\overline{\text{RFSH}}$ Delay From Rising Edge of Clock, $\overline{\text{RFSH}}$ Low		180		130		110
	$t_{DH(RF)}$	$\overline{\text{RFSH}}$ Delay From Rising Edge of Clock, $\overline{\text{RFSH}}$ High		150		120		100
$\overline{\text{WAIT}}$	$t_{S(WT)}$	$\overline{\text{WAIT}}$ Setup Time to Falling Edge of Clock	70		70		60	
$\overline{\text{HALT}}$	$t_{D(HT)}$	$\overline{\text{HALT}}$ Delay Time From Falling Edge of Clock		300		300		260
$\overline{\text{INT}}$	$t_{s(IT)}$	$\overline{\text{INT}}$ Setup Time to Rising Edge of Clock	80		80		70	
$\overline{\text{NMI}}$	$t_{w(NMI)}$	Pulse Width, $\overline{\text{NMI}}$ Low	80		80		70	
$\overline{\text{BUSRQ}}$	$t_{S(BQ)}$	$\overline{\text{BUSRQ}}$ Setup Time to Rising Edge of Clock	80		50		50	
$\overline{\text{BUSAK}}$	$t_{DL(BA)}$	$\overline{\text{BUSAK}}$ Delay From Rising Edge of Clock, $\overline{\text{BUSAK}}$ Low		120		100		90
	$t_{DH(BA)}$	$\overline{\text{BUSAK}}$ Delay From Falling Edge of Clock, $\overline{\text{BUSAK}}$ High		110		100		90
$\overline{\text{RESET}}$	$t_{s(RS)}$	$\overline{\text{RESET}}$ Setup Time to Rising Edge of Clock	90		60		60	
	$t_{F(C)}$	Delay to/from Float ($\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$)		100		80		70
	t_{mr}	$\overline{\text{M1}}$ Stable Prior to $\overline{\text{IORQ}}$ (Interrupt Ack.)	[11]		[23]		[31]	

[1] $t_{ACM} = t_w(\Phi H) + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{CA} = t_w(\Phi L) + t_r - 40$

[4] $t_{caf} = t_w(\Phi L) + t_r - 60$

[5] $t_{dcm} = t_C - 210$

[6] $t_{dci} = t_w(\Phi L) + t_r - 210$

[7] $t_{cdf} = t_w(\Phi L) + t_r - 80$

[8] $t_w(MRL) = t_c - 40$

[9] $t_w(MRH) = t_w(\Phi H) + t_f - 30$

[10] $t_w(WR) = t_c - 40$

[11] $t_{mr} = 2\,t_c + t_w(\Phi H) + t_f - 80$

[12] $t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$

[13] $t_{acm} = t_w(\phi H) + t_f - 65$

[14] $t_{aci} = t_c - 70$

[15] $t_{ca} = t_w(\Phi L) + t_r - 50$

[16] $t_{caf} = t_w(\Phi L) + t_r - 45$

[17] $t_{dcm} = t_c - 170$

[18] $t_{dci} = t_w(\Phi L) + t_r - 170$

[19] $t_{cdf} = t_w(\Phi L) + t_r - 70$

[20] $t_w(\overline{MRL}) = t_c - 30$

[21] $t_w(\overline{MRH}) = t_w(\Phi H) + t_f - 20$

[22] $t_w(\overline{WR}) = t_c - 30$

[23] $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 65$

[24] $t_{ACM} = t_w(\Phi H) + t_f - 50$

[25] $t_{aci} = t_c - 55$

[26] $t_{CA} = t_w(\Phi L) + t_r - 50$

[27] $t_{caf} = t_w(\Phi L) + t_r - 45$

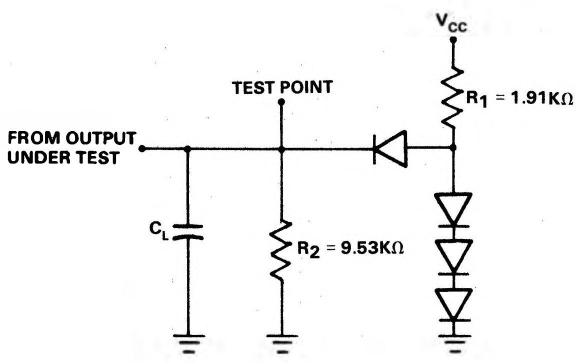
[28] $t_{dcm} = t_C - 140$

[29] $t_{dci} = t_w(\Phi L) + t_r - 140$

[30] $t_{cdf} = t_w(\Phi L) + t_r - 55$

[31] $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 50$

LOAD CIRCUIT FOR OUTPUT



NOTES (Cont'd.)

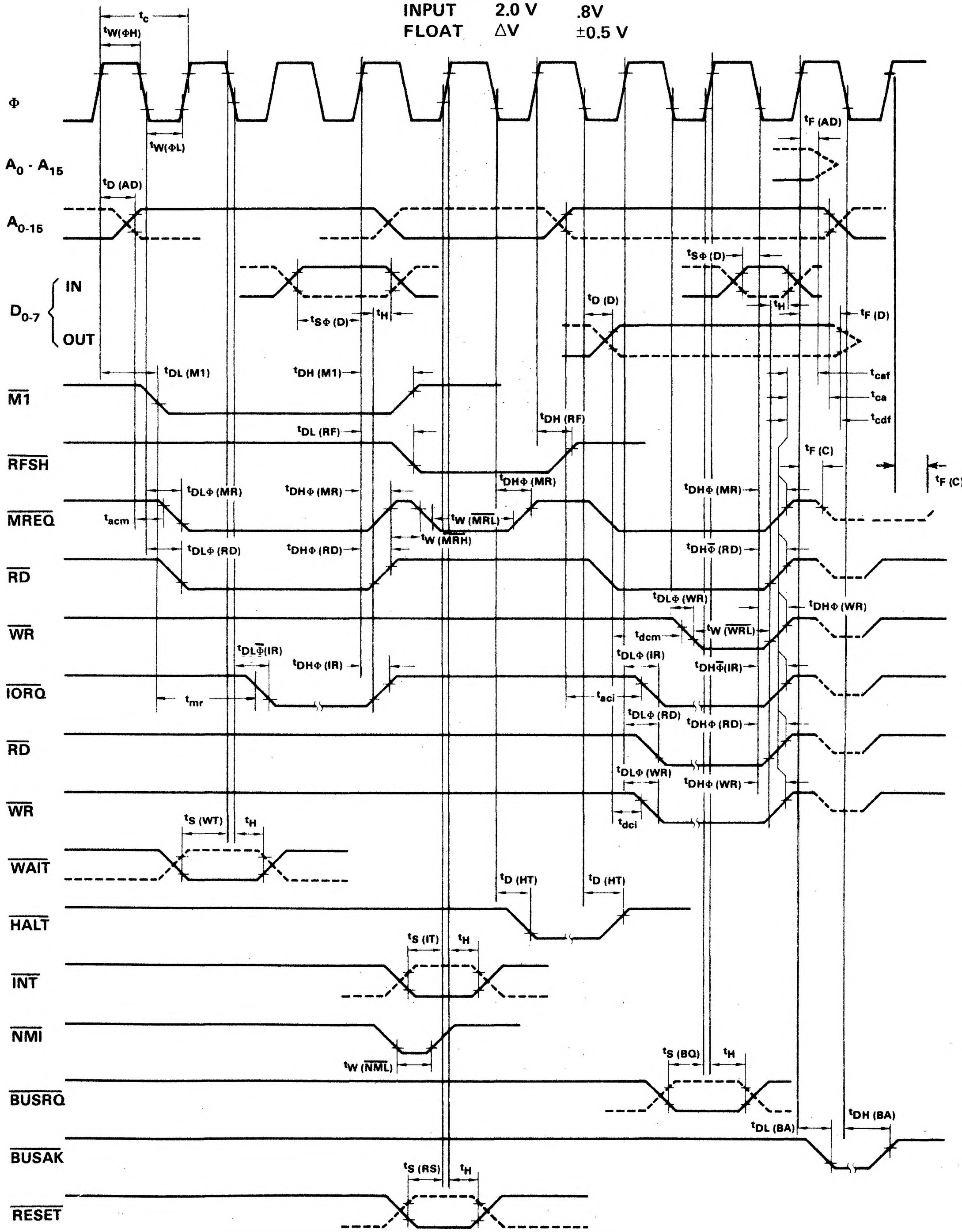
C. Output Delay vs. Load Capacitance
$T_A = 70°C$ $V_{CC} = 5\ V \pm 5\%$
Add 10 nsec delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for address and control lines.

D. Although static by design, testing guarantees $t_w(\Phi H)$ of 200 μsec maximum.

A.C. TIMING DIAGRAM

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	$V_{CC}-.6$	.8V
OUTPUT	2.0 V	.8V
INPUT	2.0 V	.8V
FLOAT	ΔV	±0.5 V



ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3880N Z80-CPU	Plastic	2.5 MHz	0° to + 70°C
MK3880P Z80-CPU	Ceramic	2.5 MHz	
MK3880N-4 Z80-CPU	Plastic	4.0 MHz	
MK3880P-4 Z80-CPU	Ceramic	4.0 MHz	
MK3880P-10 Z80-CPU	Ceramic	2.5 MHz	-40°C to +85°C