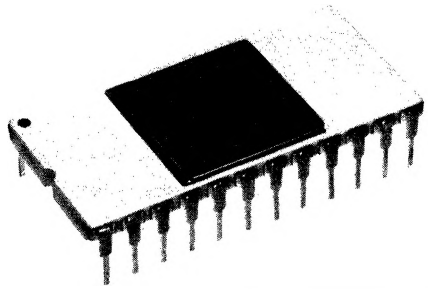
MK 28000 P

16K-BIT
MOS Read—ONLY Memory

MOSTEK

FEATURES:

- ☐ 850 ns Maximum Access Time
- ☐ 1.1 μs Maximum Cycle Time
- ☐ Low Power Dissipation —.02 mW/bit Typ.
- ☐ EA 4800/4900 Pin-for-Pin Replacement
- ☐ Options Include 2Kx8 Organization with Three-State TTL Output Capability
- ☐ 2Kx8 or 4Kx4 Organization with Open Drain Outputs
- ☐ Standard Supplies +5 Volts, — 12 Volts
- ☐ Ion-Implanted for Full TTL/DTL Compatibility



DESCRIPTION:

The MK 28000 is a mask programmable read only memory utilizing low-threshold Ion-Implant, P-channel technology. The 28000 is a pin-for-pin replacement for the EA 4800/4900. The organization may be either 2Kx8 or 4Kx4 with open drain outputs. The 2Kx8 organization may have TTL three-state outputs with only one output enable.

Output data is stored indefinitely after each memory access. If the output enables are held low during access, the outputs will be in a high impedance state.

All inputs are protected against static charge accumulation. Pullup resistors on all inputs are available as a programmable option.

PIN CONNECTIONS

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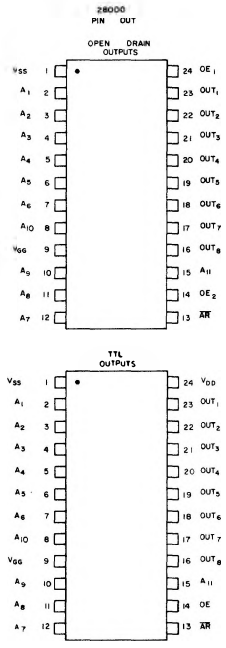
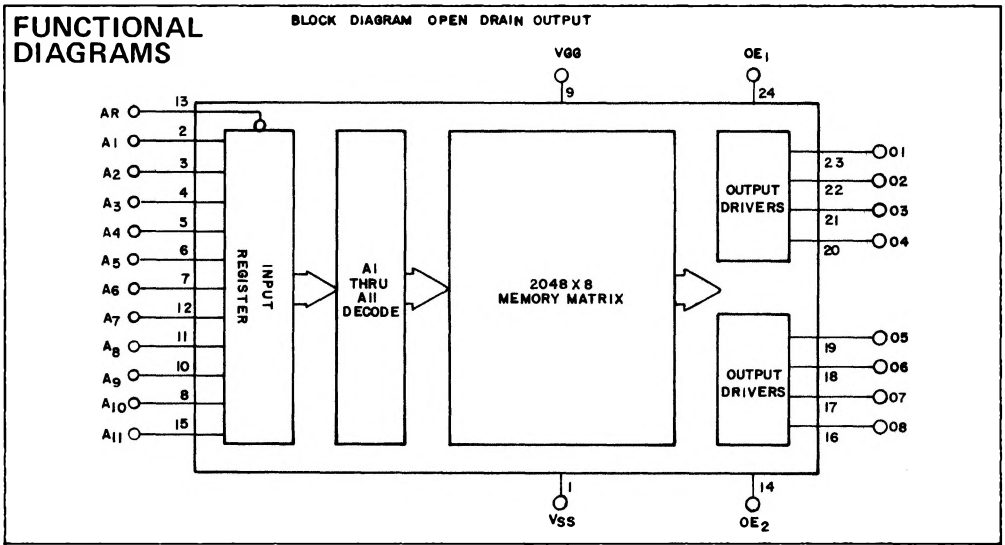
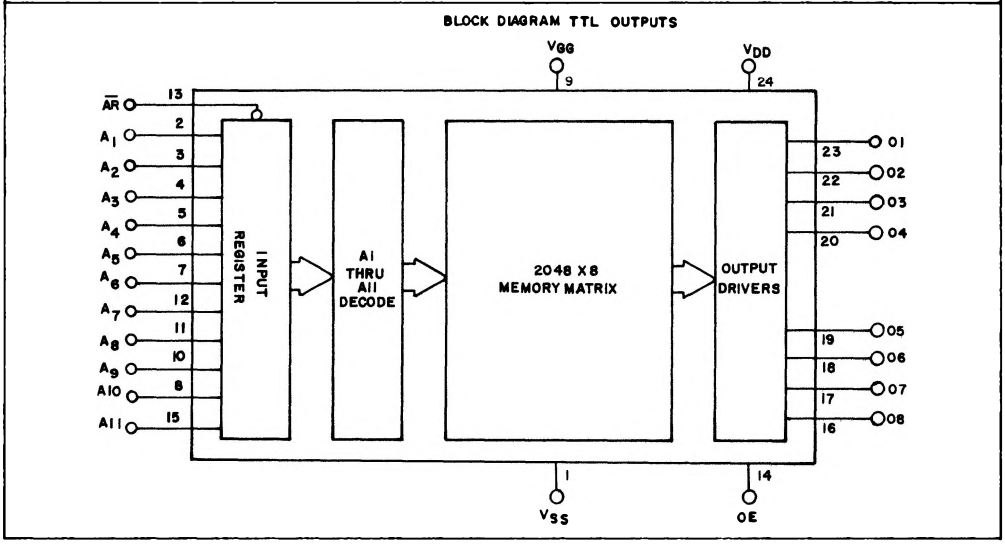


FUNCTIONAL DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} . . . . . +0.3V to −20V

Operating temperature range (Ambient). . . . . 0°C to 70°C

Storage temperature range (Ambient). . . . . −55°C to 150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

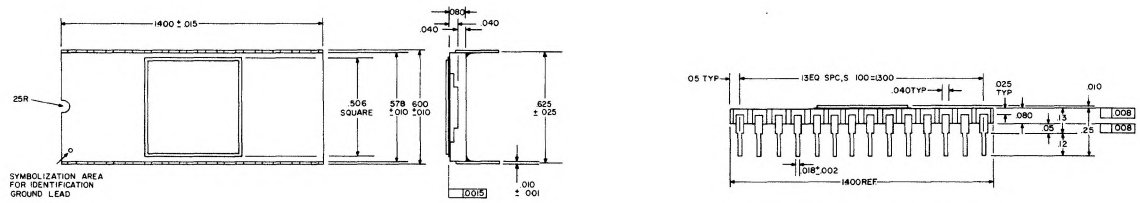
	PARAMETER	MIN	TYP	MAX	COMMENTS
V_{SS}	Supply Voltage	+4.75V	+5V	+5.25V	
V_{DD}	Supply Voltage	—	0	—	
V_{GG}	Supply Voltage	−12.6V	−12V	−11.4V	
V_{IL}	Input Voltage, Logic "0"			+.8V	
V_{IH}	Input Voltage, Logic "1"	V_{SS} − 1.5V			Pullup resistors to V_{SS} (≈5K) available as an option

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5.0V ±5%; V_{DD} = 0V; V_{GG} = −12V ±5%; $0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	COMMENTS
I_{SS}	Supply Current		12 mA	20 mA	Outputs unconnected
I_{GG}	Supply Current		12 mA	20 mA	Inputs at V_{SS}
C_{IN}	Input Capacitance			10 pF	See Note 1
I_{IN}	Input Leakage			10 μA	See Note 2
R_{IN}	Input Pullup Resistors	3 KΩ		9 KΩ	Optional
V_{OL}	Output Voltage, Logic "0"			0.4V	I_{OL} = 1.6 mA See Note 3
V_{OH}	Output Voltage, Logic "1"	2.5V			See Note 4
I_{OL}	Output Leakage Current	−10 μA		+ 10 μA	$V_O = V_{SS} - 6V$, T = 25°C (outputs disabled)

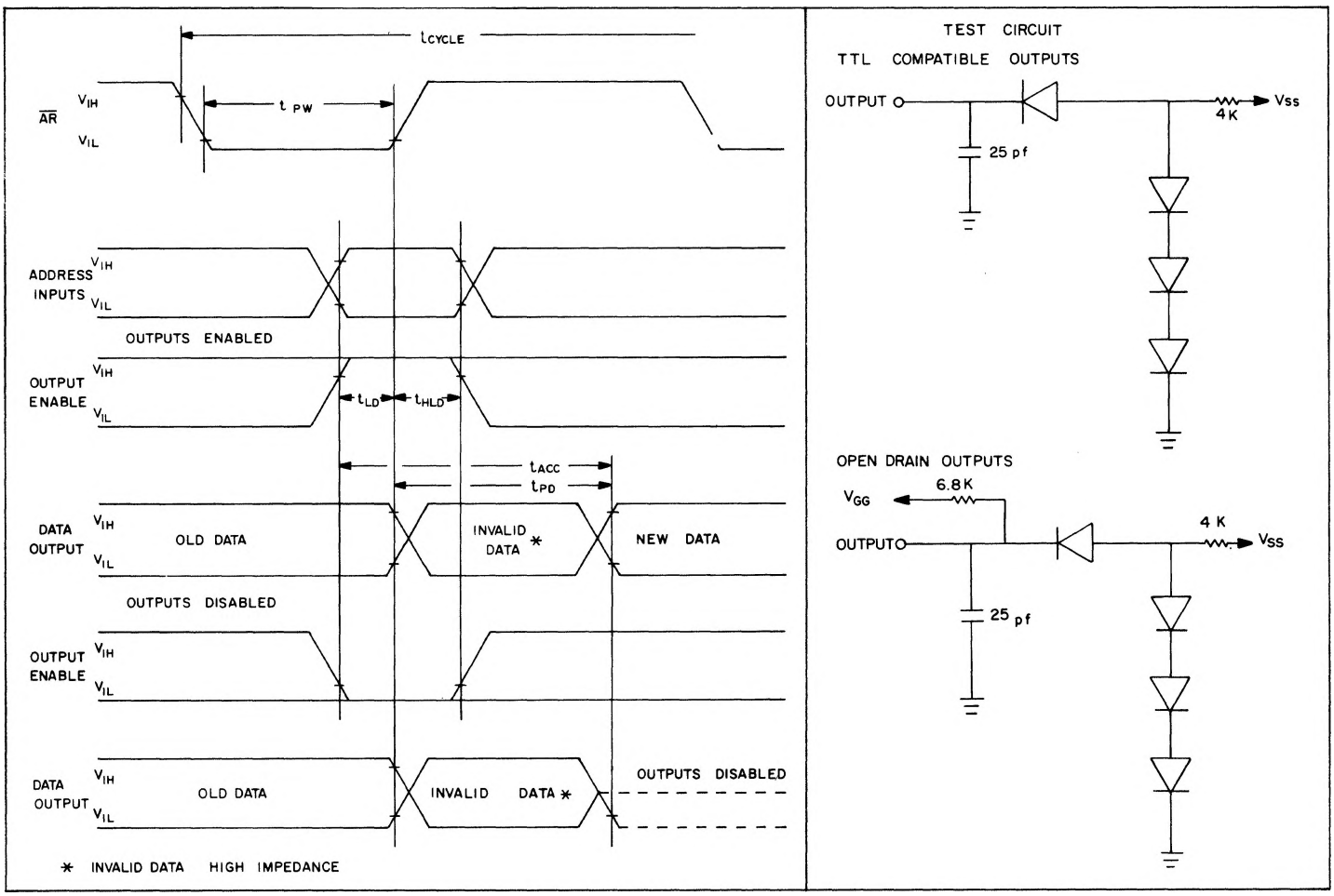
PACKAGE 28-pin ceramic dual-in-line



	PARAMETER	MIN	TYP	MAX	COMMENTS
t_{PW}	$\overline{AR}$ Pulse Width	400 ns			See timing and test circuit
t_{LD}	Address Lead Time	200 ns			
t_{HLD}	Address Hold Time	200 ns			
t_{PD}	$\overline{AR}$ to Output Delay	650 ns			
t_{ACC}	Access Time			850 ns	$t_{acc} = t_{ld} + t_{pd}$
t_{CYCLE}	Cycle Time	1.1 μs			$t_{cycle} = t_{pw} + t_{pd}$

NOTES:
1. $V_{BIAS} - V_{SS} = 0v$; f = 1 MHz
2. This parameter is for inputs without pullups (optional)
3. This parameter is for outputs with TTL compatible outputs.
4. For open drain outputs, a 6.8K Ω load to V_{GG} is assumed. (See test circuits)

TIMING



MOSTEK 28000 ROM Punched Card Coding Format[1]

First Card

Cols	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	MOSTEK Part Number[2]
10-16	Organization (2048X8 or 4096X4)
29	Outputs (1=Open Drain, ϕ=Push Pull TTL)
31	Number of Output Enable Pins (1 or 2)
33	Input Pullups (1=yes, ϕ=no)

Fourth Card

1-9	Data Format[3]
15-28	Logic – ("Positive Logic" or "Negative Logic")
35-57	Verification Code[4]

Data Cards

MOSTEK Format		or	EA Format (for EA Pin-for-Pin Replacement only)
1-4	Decimal Address		
6-13	Output B8-B1 (MSB Thru LSB)		
15-17	Octal Equivalent of Output Data		

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank
3. MOSTEK or Electronic Arrays Punched card coding format may be used. Specify which card format used by punching either "MOSTEK" or "EA". Start at column one.
4. Punched as: (a) VERIFICATION HOLD – i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS – i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED – i.e. the customer will not receive a CVDS and production will begin immediately.