MK 2500 P
MK 2600 P

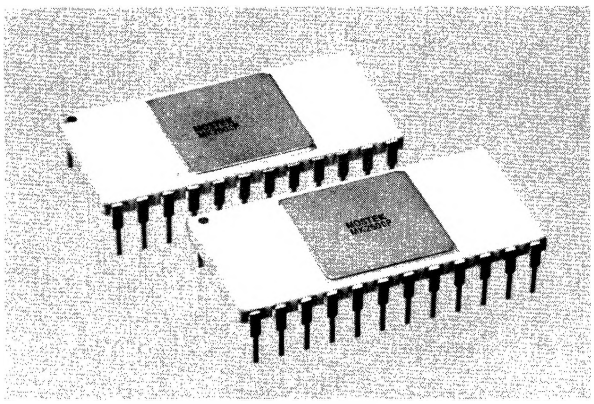
4096-BIT
MOS Read-Only Memory

MOSTEK

Read Only Memories

FEATURES

- ☐ High-speed, static operation — 400 nsec. typical access time
- ☐ Active input pull-ups provide worst-case TTL compatibility
- ☐ Push-pull outputs provide three output states: one, zero, and open
- ☐ Ion-implantation for constant current loads and lower power
- ☐ Standard power supplies: +5V, —12V
- ☐ MK 2500 P is pin-for-pin replacement for National 5232
- ☐ MK 2600 P is pin-for-pin replacement for Fairchild 3514



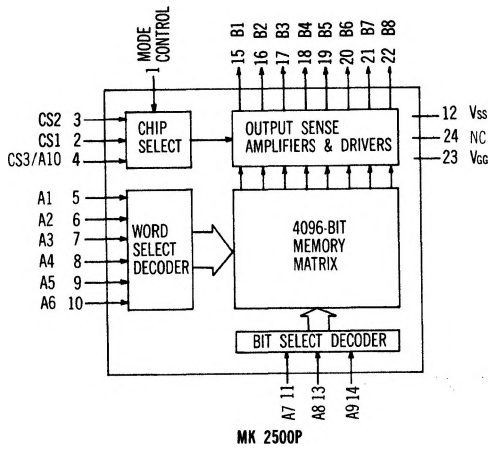
DESCRIPTION

The MK 2500 P and MK 2600 P series of TTL/DTL compatible MOS read-only memories (ROMs) are designed to store 4096 bits of information by programming one mask pattern. The word and bit organization of these ROM series is either 512W X 8B or 1024W X 4B.

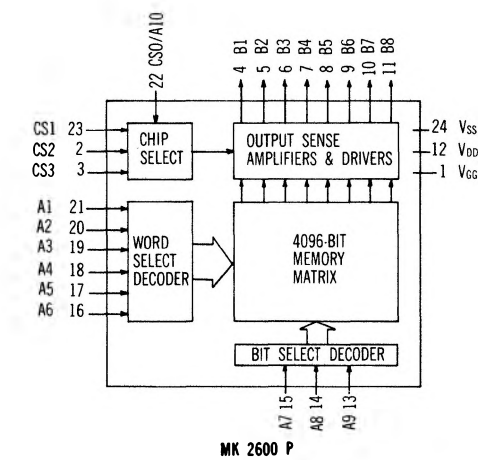
The MK 2500/2600 P series has push-pull outputs that can be in one of three states: logic one, logic zero, or open or unselected state. This, plus the programmable Chip Selects, enables the use of several ROMS in parallel with no external components. Since the ROM is a static device, no clocks are required, making the MK 2500/2600 P series of ROMS very versatile and easy to use.

Low threshold-voltage processing, utilizing ion-implantation, is used with P-channel, enhancement-mode MOS technology to provide direct input/output interfacing with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

FUNCTIONAL DIAGRAMS



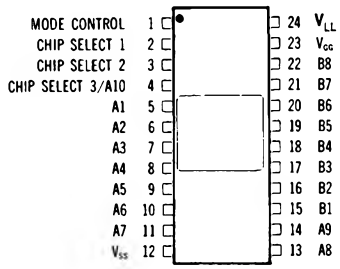
MK 2500P



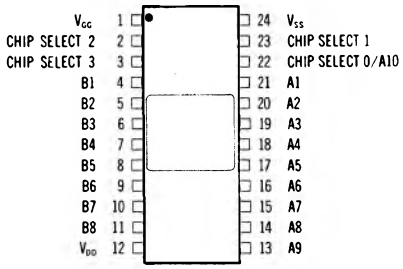
MK 2600 P

PIN CONNECTIONS

MK 2500 P



MK 2600 P



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} (except V_{GG}) ..... +0.3V to −10V
Voltage on V_{GG} Terminal Relative to V_{SS} ..... +0.3V to −20V
Operating Temperature Range (Ambient) ..... 0°C to +70°C
Storage Temperature Range (Ambient) ..... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.0	+5.25	V	
V_{DD}	Supply Voltage	——	0.0	——	V	Note 1
V_{GG}	Supply Voltage	−11.4	−12.0	−12.6	V	
V_{IL}	Input Voltage, Logic "0"			+0.8	V	
V_{IH}	Input Voltage, Logic "1"	$V_{SS}-1.5$			V	Note 2
V_{IH}	Input Voltage, Logic "1"	2.4			V	Note 3

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5.0V \pm 5\%$; $V_{DD} = 0$ V; $V_{GG} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless noted otherwise)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		19.0	28.0	mA	Note 4
I_{GG}	Supply Current, V_{GG}		19.0	28.0	mA	Note 4
$I_{I(L)}$	Input Leakage Current, Any Input			10.0	μA	$V_I = V_{SS}-6.0V$. Note 2
I_{IL}	Input Current, Logic 0, Any Input			−100.0	μA	$V_I = .4V$. Note 3
I_{IH}	Input Current, Logic 1, Any Input			−600.0	μA	$V_I = 2.4V$. Note 3
V_{OL}	Output Voltage, Logic "0"			0.4	V	$I_{OL} = 1.6mA$
V_{OH}	Output Voltage, Logic "1"	2.4			V	$I_{OH} = -40\mu A$
$I_{O(L)}$	Output Leakage Current			+10	μA	Outputs disabled ($V_O = V_{SS}-6V$)
C_{IN}	Input Capacitance			10	pF	Note 5
C_O	Output Capacitance			10	pF	Note 5
t_{ACCESS}	Address to Output Access Time	100	400	700	nsec	Refer to
t_{CS}	Chip Select to Output Delay	100	250	500	nsec	Test
t_{CD}	Chip Deselect to Output Delay	100	250	800	nsec	Note 6 Circuit

Notes: 1. This is V_{LL} on MK2500P.

2. This parameter is for inputs without active pull-ups (programmable).
3. This parameter is for inputs with active pull-ups (programmable) for TTL interfaces. As the TTL driver goes to a logic 1 it must only provide 2.4V (this voltage must not be clamped) and the circuit pulls the input to V_{SS}. Refer to the Input pull-up figure for a graphical description of the active pull-up's operation.
4. Inputs at V_{SS}, outputs unloaded.
5. $V_{Bias} - V_{SS} = OV$; $f = 1$ MHz.
6. t_{CD} is primarily dependent on the RC time constant of the load (i.e. the outputs become open circuited upon being disabled). As noted in the Timing Diagram, disabling or enabling an output with a "1" expected out does not yield a transition through the 1.5V point; this is true because the TTL equivalent load pulls the open-circuited output to approximately 2 volts.

PROGRAMMING OPTIONS

MK 2500 P

Function	OPTIONS 512 X 8	1024 X 4
Mode Control	1	0
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3/A10	1 or 0	address A10

1 = Most Positive = High Level Voltage

Pin 1 in the MK 2500 P is used as a Mode Control, setting the circuit in the 1024x4 or 512x8 mode. In the 1024x4 mode a tenth address bit is required, which is provided at Pin 4. If the circuit is in the 512x8 mode, then Pin 4 may be used for a third chip select.

Additional Options: The MK 2500 P can have the address and control inputs set by the user so that:

512x8: Mode Control — High
A10 — Low

1024x4: Mode Control — Low
A10 aid as an address
See Note 9, following page

MK 2600 P

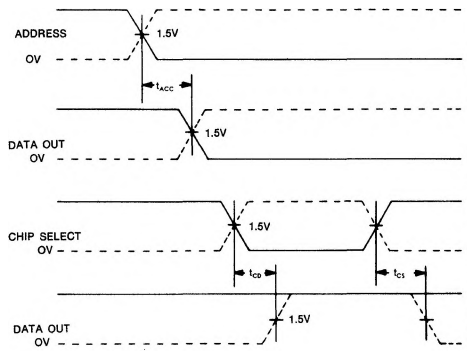
Function	OPTIONS 512 X 8	1024 X 4
Chip Select 0/A10	1 or 0	A10
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3	1 or 0	1 or 0

1 = Most Positive = High Level Voltage

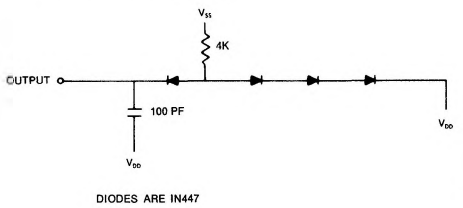
The MK 2600 P is programmed either as a 512x8 array or a 1024x4 array. In the 1024x4 arrays, Pin 22 provides the tenth address bit. When A10 is low the four bits are present at the even outputs (B2, B4, B6, and B8); when A10 is high, the bits are at the odd outputs (B1, B3, B5, and B7).

In 512x8 arrays, Pin 22 may be used to provide a fourth chip select. Thus, with four programmable chip selects, sixteen MK 2600 P ROMS in the 512x8 configuration can be arranged in an 8192x8 array requiring no external decoding.

TIMING

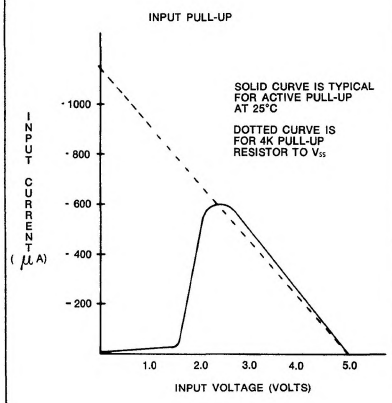


T_{ACCESS} TEST CIRCUIT

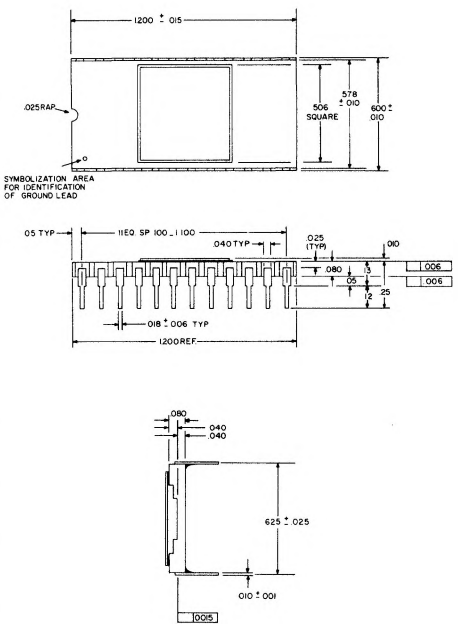


DIODES ARE IN447

INPUT



PACKAGE 24-lead ceramic dual-in-line hermatic



MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2500 P

First Card

Cols.	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[2]
10-16	Organization[3]
29	CS3[10]
30	CS2[4]
31	CS1[4]
32	Active Pull-ups[5]

Fourth Card

1-9	Data Format[6]
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]
60-67	"A10 EVEN" or "A10 ODD" (left justified)[9]

Data Cards/512x08 Organization

1-4	Decimal Address
6-13	Output B8- B1 (MSB thru LSB)
15-17	Octal Equivalent of output data[8]

Data Cards/1024x04 Organization

1-4	Decimal Address (0-1022), even addresses
6-9	Output (MSB-LSB)
11-12	Octal Equivalent of output data[8]
50-53	Decimal Address (1-1023), odd addresses
55-58	Output (MSB-LSB)
60-61	Octal Equivalent of output data[8]

MK 2600 P

First Card

Cols.	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[2]
10-16	Organization[3]
29	CS3[4]
30	CS2[4]
31	CS1[4]
32	CS0[10]
33	Active Pull-ups[5]

Fourth Card

1-9	Data Format[6]
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]

Data Cards/512x08 Organization

1-4	Decimal Address
6-13	Output B8- B1 (MSB thru LSB)
15-17	Octal Equivalent of output data[8]

Data Cards/1024x04 Organization

1-4	Decimal Address (0-1022), even addresses
6-9	Output (MSB-LSB)
11-12	Octal Equivalent of output data[8]
50-53	Decimal Address (1-1023), odd addresses
55-58	Output (MSB-LSB)
60-61	Octal Equivalent of output data[8]

Notes:

1. Positive or negative logic formats are accepted as noted in the fourtn card.
2. Assigned by Mostek Marketing Department; may be left blank.
3. Punched as "0512x08" or "1024x04".
4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.
5. A "1" indicates active pull-ups; a "0" indicates no pull-ups.
6. MOSTEK, Fairchild, or National Punched-Card Coding Format may be used. Specify which punched card format used by punching either "MOSTEK", "Fairchild", or "National". Start name at column one.
7. Punched as:
   (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.
8. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 10011110 would be separated into groups 10/011/110 and the resulting octal equivalent number is 236.
9. "A10 EVEN" and "A10 ODD" applies to the 1024 x 4 mode. "A10 EVEN" means the even outputs are enabled when A10 is high. "A10 ODD" means the odd outputs are enabled when A10 is high.
10. Punched as "2" for 1024 x 4 organization.

ASCII-TO-EBCDIC CODE CONVERTER
EBCDIC-TO-ASCII CODE CONVERTER

A_1 = LSB B_1 = LSB
A_9 = MSB B_8 = MSB

MK 2503 P

Function	512 X 8
Mode Control	1
Chip Select 1	0
Chip Select 2	0
Chip Select 3/A10	0

MK 2601 P

Function	512 X 8
Chip Select 0/A10	0
Chip Select 1	0
Chip Select 2	0
Chip Select 3	0

ASCII (ADDRESS) TO EBCDIC (DATA)

0	00000000	1	00000001	2	00000010	3	00000011	128	00100000	129	00100001	130	00100010	131	00100011
4	00110111	5	00101101	6	00101110	7	00101111	132	00100100	133	00010101	134	00000110	135	00010111
8	00010110	9	00000101	10	00100101	11	00001011	136	00101000	137	00101001	138	00101010	139	00101011
12	00001100	13	00001101	14	00001110	15	00001111	140	00101100	141	00001001	142	00001010	143	00011011
16	00010000	17	00010001	18	00010010	19	00010011	144	00110000	145	00110001	146	00011010	147	00110011
20	00111100	21	00111101	22	00110010	23	00100110	148	00110100	149	00110101	150	00110110	151	00001000
24	00011000	25	00011001	26	00111111	27	00100111	152	00111000	153	00111001	154	00111010	155	00111011
28	00011100	29	00011101	30	00011110	31	00011111	156	00000100	157	00010100	158	00111110	159	11100001
32	01000000	33	01001111	34	01111111	35	01111011	160	01000001	161	01000010	162	01000011	163	01000100
36	01011011	37	01101100	38	01010000	39	01111101	164	01000101	165	01000110	166	01000111	167	01001000
40	01001101	41	01011101	42	01011100	43	01001110	168	01001001	169	01010001	170	01010010	171	01010011
44	01101011	45	01100000	46	01001011	47	01100001	172	01010100	173	01010101	174	01010110	175	01010111
48	11110000	49	11110001	50	11110010	51	11110011	176	01011000	177	01011001	178	01100010	179	01100011
52	11110100	53	11110101	54	11110110	55	11110111	180	01100100	181	01100101	182	01100110	183	01100111
56	11111000	57	11111001	58	01111010	59	01011110	184	01101000	185	01101001	186	01110000	187	01110001
60	01001100	61	01111110	62	01101110	63	01101111	188	01110010	189	01110011	190	01110100	191	01110101
64	01111100	65	11000001	66	11000010	67	11000011	192	01110110	193	01110111	194	01111000	195	10000000
68	11000100	69	11000101	70	11000110	71	11000111	196	10001010	197	10001011	198	10001100	199	10001101
72	11001000	73	11001001	74	11010001	75	11010010	200	10001110	201	10001111	202	10010000	203	10011010
76	11010011	77	11010100	78	11010101	79	11010110	204	10011011	205	10011100	206	10011101	207	10011110
80	11010111	81	11011000	82	11011001	83	11100010	208	10011111	209	10100000	210	10101010	211	10101011
84	11100011	85	11100100	86	11100101	87	11100110	212	10101100	213	10101101	214	10101110	215	10101111
88	11100111	89	11101000	90	11101001	91	01001010	216	10110000	217	10110001	218	10110010	219	10110011
92	11100000	93	01011010	94	01011111	95	01101101	220	10110100	221	10110101	222	10110110	223	10110111
96	01111001	97	10000001	98	10000010	99	10000011	224	10111000	225	10111001	226	10111010	227	10111011
100	10000100	101	10000101	102	10000110	103	10000111	228	10111100	229	10111101	230	10111110	231	10111111
104	10001000	105	10001001	106	10010001	107	10010010	232	11001010	233	11001011	234	11001100	235	11001101
108	10010011	109	10010100	110	10010101	111	10010110	236	11001110	237	11001111	238	11011010	239	11011011
112	10010111	113	10011000	114	10011001	115	10100010	240	11011100	241	11011101	242	11011110	243	11011111
116	10100011	117	10100100	118	10100101	119	10100110	244	11101010	245	11101011	246	11101100	247	11101101
120	10100111	121	10101000	122	10101001	123	11000000	248	11101110	249	11101111	250	11111010	251	11111011
124	01101010	125	11010000	126	10100001	127	00000111	252	11111100	253	11111101	254	11111110	255	11111111

EBCDIC (ADDRESS) TO ASCII (DATA)

256	00000000	257	00000001	258	00000010	259	00000011	384	11000011	385	01100001	386	01100010	387	01100011
260	10011100	261	00001001	262	10000110	263	01111111	388	01100100	389	01100101	390	01100110	391	01100111
264	10010111	265	10001101	266	10001110	267	00001011	392	01101000	393	01101001	394	11000100	395	11000101
268	00001100	269	00001101	270	00001110	271	00001111	396	11000110	397	11000111	398	11001000	399	11001001
272	00010000	273	00010001	274	00010010	275	00010011	400	11001010	401	01101010	402	01101011	403	01101100
276	10011101	277	10000101	278	00001000	279	10000111	404	01101101	405	01101110	406	01101111	407	01110000
280	00011000	281	00011001	282	10010010	283	10001111	408	01110001	409	01110010	410	11001011	411	11001100
284	00011100	285	00011101	286	00011110	287	00011111	412	11001101	413	11001110	414	11001111	415	11010000
288	10000000	289	10000001	290	10000010	291	10000011	416	11010001	417	01111110	418	01110011	419	01110100
292	10000100	293	00001010	294	00010111	295	00011011	420	01110101	421	01110110	422	01110111	423	01111000
296	10001000	297	10001001	298	10001010	299	10001011	424	01111001	425	01111010	426	11010010	427	11010011
300	10001100	301	00000101	302	00000110	303	00000111	428	11010100	429	11010101	430	11010110	431	11010111
304	10010000	305	10010001	306	00010110	307	10010011	432	11011000	433	11011001	434	11011010	435	11011011
308	10010100	309	10010101	310	10010110	311	00000100	436	11011100	437	11011101	438	11011110	439	11011111
312	10011000	313	10011001	314	10011010	315	10011011	440	11100000	441	11100001	442	11100010	443	11100011
316	00010100	317	00010101	318	10011110	319	00011010	444	11100100	445	11100101	446	11100110	447	11100111
320	00100000	321	10100000	322	10100001	323	10100010	448	01111011	449	01000001	450	01000010	451	01000011
324	10100011	325	10100100	326	10100101	327	10100110	452	01000100	453	01000101	454	01000110	455	01000111
328	10100111	329	10101000	330	01011011	331	00101110	456	01001000	457	01001001	458	11101000	459	11101001
332	00111100	333	00101000	334	00101011	335	00100001	460	11101010	461	11101011	462	11101100	463	11101101
336	00100110	337	10101001	338	10101010	339	10101011	464	01111101	465	01001010	466	01001011	467	01001100
340	10101100	341	10101101	342	10101110	343	10101111	468	01001101	469	01001110	470	01001111	471	01010000
344	10110000	345	10110001	346	01011101	347	00100100	472	01010001	473	01010010	474	11101110	475	11101111
348	00101010	349	00101001	350	00111011	351	01011110	476	11110000	477	11110001	478	11110010	479	11110011
352	00101101	353	00101111	354	10110010	355	10110011	480	01011100	481	10011111	482	01010011	483	01010100
356	10110100	357	10110101	358	10110110	359	10110111	484	01010101	485	01010110	486	01010111	487	01011000
360	10111000	361	10111001	362	01111100	363	00101100	488	01011001	489	01011010	490	11110100	491	11110101
364	00100101	365	01011111	366	00111110	367	00111111	492	11110110	493	11110111	494	11111000	495	11111001
368	10111010	369	10111011	370	10111100	371	10111101	496	00110000	497	00110001	498	00110010	499	00110011
372	10111110	373	10111111	374	11000000	375	11000001	500	00110100	501	00110101	502	00110110	503	00110111
376	11000010	377	01100000	378	00111010	379	00100011	504	00111000	505	00111001	506	11111010	507	11111011
380	01000000	381	00100111	382	00111101	383	00100010	508	11111100	509	11111101	510	11111110	511	11111111