MOS Read-Only Memory Character Generators

MK 2000 P SERIES MK 2002 P MOSTEK

Read Only Memories

FEATURES:

- □ 64 dot-matrix (5×7) characters with column-by-column output
- □ High speed character access time and column select access time
- □ Completely static operation—no clocks required
- □ MK 2002 P is pre-programmed with ASCII encoding
- Easy interfacing to TTL/DTL
- Single mask custom programming

APPLICATIONS

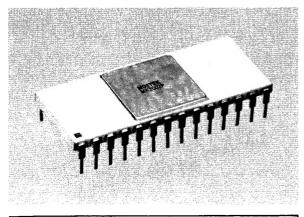
- □ CRT alphanumeric displays
- □ Light-Emitting Diode (LED) array driver
- Billboard and stock market displays

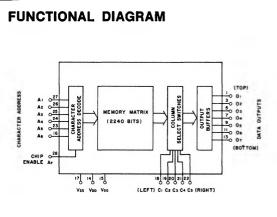
DESCRIPTION

This MK 2000 P Series MOS Read-Only Memories (ROMs) is designed specifically for dotmatrix character generation where column-by-column data output is desired. Each ROM contains 2240 bits of programmable storage, organized as 64 characters, each having 5 columns of 7 bits. P-channel, enhancement-mode, MOS technology is employed in this series. All inputs are protected to prevent damage due to static charge accumulation.

Programming is accomplished during the manufacturing process by modification of a single mask in accordance with customer specifications. The MK 2002 P is pre-programmed with ASCII-encoded characters with the font shown on the back page.

Memory operation is static and no refresh clocks are required to maintain output information. Character selection is achieved by presenting a seven-bit binary word at the address inputs. The most significant bit (A_{7}) is generally used as a Chip Enable. (See Operating Notes.) Column select lines, C₁ through C₅, select the column information that appears at the seven data outputs, (See Operating Notes.) By sequentially strobing C_1 through C_5 , the font for the addressed character would be displayed. The output buffers are open-ended current sources, sourcing current from the V_{ss} supply only in the "doton" condition.





OPERATING NOTES

"1	" = \	/00	"0"	$= V_s$	s
C,	C2	C,	C₁	Cs	Column Selected
X	х	х	х	х	None*
0	0	0	0	0	None*
1	0	0	0	0	1 (left)
0	1	0	0	0	2
0	0	1	0	0	3
۰0	0	0	1	0	4
0	0	0	0	1	5 (right)
	C ₁ X 0 1 0 0 .0	C1 C2 X X 0 0 1 0 0 1 0 0 .0 0	X X X 0 0 0 1 0 0 0 1 0 0 0 1 .0 0 0	C1 C2 C3 C4 X X X X 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0 0 1 0	C1 C2 C1 C4 C5 X X X X X 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 1 0 0

No effect on columns
Outputs open-circuited



MOS 2240-Bit Character Generators

MK 2000 P Series

MK 2002 P

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to Vss	.+0.3V to $-30V$
Operating temperature range	$-25^{\circ}C$ to $+85^{\circ}C$
Storage temperature range	55°C to +150°C

Read Only Memories

RECOMMENDED OPERATING CONDITIONS (---0°C<T_A<70°C)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V _{SS} V _{DD} V _{GG}	Supply voltage Supply voltage Supply voltage		0.0 14.0 28.0			See note 1
INPUTS	Vin(0) Vin(1)	Input voltage, logic ''0'' Input voltage, logic ''1''	V ₅₅ – 3		Vss — 11	V V	

ELE		AL CHARACTERISTICS unless note	ed othe	erwise)			·	
		PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS	
POWER	Idd Igg	Supply current (V _{DD}) Supply current (V _{GG})		13 1.5	25 3.0	mA mA	Outputs unconnected See note 2	
INPUTS	Cin Iin	Input capacitance Input leakage current			10 10	pF μA	$V_{in} = V_{SS}, f_{meas} = 1MHz$ $V_{in} = V_{SS} - 14V$	
OUTPUTS	Vout lout(on) lout(off)	Output voltage Output current, "dot-on" Output current, "dot-off"	6	12	$V_{ss}-2$ $V_{ss}-5$ $+10$	∨ ∨ mA μA	$I_{out} = 4.0 \text{ mA}$ F	See Figure #3
	t∧(on)	Character access time, I_{off} to I_{on}		320 380	700 700	ns ns	$V_{DD} = -12, V_{GG} = -24V$ F	See Figures #1, #2
RISTICS	t∧(off)	Character access time, $I_{\mbox{\scriptsize or}}$ to $I_{\mbox{\scriptsize off}}$		190 220	700 700	ns ns		and Timing
CHARACTERISTICS	t _{C(on)}	Column select delay time, I_{off} to I_{on}		90 95	250 300	ns ns	$\frac{V_{DD} = -14V, V_{GG} = -28V}{V_{DD} = -12V, V_{GG} = -24V} F_{4}$	See Figure #1 and
DYNAMIC C	t _{C(off)}	Column select delay time, I_{on} to I_{off}		180 205	250 300	ns ns	$V_{DD} = -14V, V_{GG} = -28V$ $V_{DD} = -12V, V_{GG} = -24V$	Timing
á	toe	Output enable/disable delay time		320	700	ns	$V_{DD} = -14V$, $V_{GG} = -28V$	
	tav	Character access time (V_{out})		500		ns	V_{ss} = +14V, V_{DD} =0V, V_{GG} = See Figure #4 and Timing	- 14V

NOTES: 1. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS} , e.g., $V_{SS} = +14.0V$, $V_{DD} = 0.0V$, $V_{GG} = -14.0V$.

2. $l_{ss} = l_{DD} + l_{ee}$

TIMING

Vss

400

350

300 (su)

250

200

150

100

R_{tol} = 5%

Character Access time

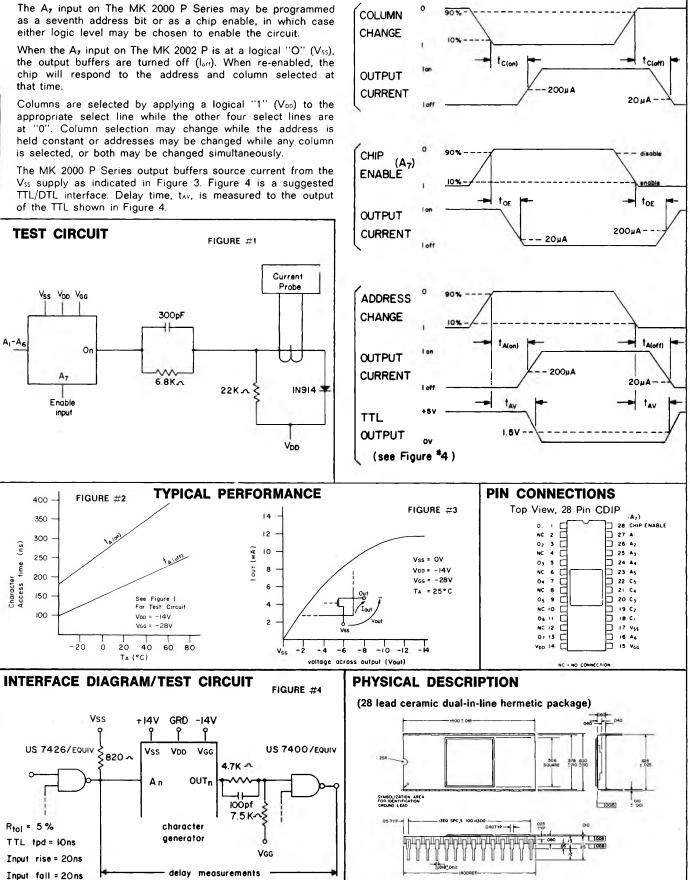
AI-A

as a seventh address bit or as a chip enable, in which case either logic level may be chosen to enable the circuit.

When the A₇ input on The MK 2002 P is at a logical "O" (Vss), the output buffers are turned off (loff). When re-enabled, the chip will respond to the address and column selected at that time.

appropriate select line while the other four select lines are at "0". Column selection may change while the address is held constant or addresses may be changed while any column is selected, or both may be changed simultaneously.

Vss supply as indicated in Figure 3. Figure 4 is a suggested TTL/DTL interface. Delay time, $t_{\text{Av}},$ is measured to the output of the TTL shown in Figure 4.



(waveforms not to scale)

Read Only Memories

CODING AND CHARACTER FONTS

ge e esent	equal to ts a vol	V _{ss} , or tage eq	an out	'0'' represents put I _{0N} , and a / _{DD} , or an outpu	logic "1" ut l₀rr.		$\begin{array}{cccccccccccccccccccccccccccccccccccc$	0 1 0 0 1 0 1 1 0 1 1 0 1 1 0 1 1 0
	MK 20	02 P		A6 A5	1 0	1	0	0 1
4.	A ₃	A ₂	Α,	COL	2	3	4	5
0	0	0	0	0		1 (19) (20) (1) (1) (1) (1) (1) (1) (1) (1) (1) (1		00 00 00 1 01 1 1 00 05 0 1 1 05 00 00 1 05 00 1 1 05 00 1 1 05 00 1 1 05 1 1 1 05 1 1 1 05 1 1 1 05 1 1 1
0	0	0	1	1		1 (00) (00) 1 1 (00) 1 (00) 1 1 1 (00) 1 1 1 (00) 1 1 1 (00) 1 1 1 (00) 1	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
0	0	1	0	2	1 (0): 1 (0): 1 1 (1): 1 (1): 1 1 (2): 1 (20: 1): 1 1 (2): 1 (2): 1 (2): 1 1 (2): 1 (2): 1 (2): 1 1 (2): 1	0 1 1 1 1 200 1 1 1 1 1 200 1 200 1 1 200 200 1 200 1 1 200 200 200 200 200 200 200 200 200 200	100 1 1 100 100 1 1 00 100 100 1 100 100 100 1 100 100 1 1 100 100 1 1 100 100 1 1 100 100 1 1 100 100 100 100 100	00 1 1 1 1 00 01 1 1 1 00 02 00 02 02 1 03 1 00 1 00 1 00 1 00 1 1 00 1 00 1 1 00 1 1 00 1 1 00 1 1 00 1 00 1 1 00 1 00 1 1 00 1 00 1 1 1 1 00 1 1 1 1 1 1 00 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0	0	1	1	3	1 00, 1 00, 1 00, 00, 00, 00, 1 1 00, 00, 00, 1 1 00, 00, 00, 1 1 00, 100, 1 1 00, 1 1 0, 00, 1	1 1 1 1 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1	の ・ 「 ・ 「 ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・	●2011 「 1 1 1 ●2115 1 1 1 1 2015 00 00 1 1 1 1 2011 00 1 1 2011 00 1 1 1 1 2011 00 1 1 00 1 1 2011 00 1 1 00 1 1 0 00 1
0	1	0	0	4			005 11 1 1 005 1 005 1 1 1 1 005 1 005 1 1 1 0 005 1 005 1 1 1 0 005 1 005 005 005 1 1 0 005 1 005 005 005 005 005 0	
0	1	0	1	5	ACC 302: 1 1 905 1 1 1 000 1 1 1002 1 1 1002 1 1 002 1 1 002 1 1 002 0 1 1 102 0 1 1 1 1 1 102 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			
0	1	1	0	6		19811111 1990年 1月11日 1月1111 1月1111 1月1111 1月1111 1月1111 1月1111 1月1111 1月11111 111111		
0	1	1	1	7				
1	0	0	0	8		第二日 - 1 - 1 - 1 - 2 - 2 - 2 - 2 - 2 - 2 - 2		97. 401 1 405. 500 1 1 105 1 1 1 801 1 405 1 1 901 1 1 1 905 902 1 1 1 905 902 1 1 1 905 902 1 1 1 905
1	0	0	1	9		Bill 1	1 1 970 1 1 1 0 000 1 1 1 0 000 1 1 1 0 000 000 1 1 1 0 000 000 1 1 1 1 000 000 000	
1	0	1	0	10	0:1 0:00 0:			1 1 1 0 ¹¹ 1 1 0 ¹¹ 1 1 1 0 ¹¹ 1 1 1 0 ¹¹ 1 1 1 1 1 1 0 ¹¹ 1 1 1 1 1 0 ¹¹ 0 ¹¹ 1 1 0 ¹¹ 0 ¹¹
1	0	1	1	11				
1	1	0	0	12				
1	1	0	1	13		유드 위비 위비 위비 위비 위비 위비 1 1 1 1 1 역 위비 위비 1 1 1 1 1 1 1		
1	1	1	0	14				
1	1	1	1	15				1 1 1 1 1 1 1 1 1 100 05 05 001 001

An example demonstrating the correspondence of device

outputs and sequence to the 5 x 7 dot matrix fonts is

MOSTEK ROM PUNCHED-CARD CODING FORMAT'

MK 2000 P

Cols. **Information Field First Card**

1-30 Customer 31-50 Customer Part Number 60-72 Mostek Part Number¹

Second Card

Engineer at Customer Site 1-30 Direct Phone Number for Engineer 31-50

Third Card

1-5 Mostek Part Number¹ 10-15 Organization²

Fourth Card

0-6 Data Format³-"MOSTEK"

- 15-28 Logic-"Negative Logic" only
- Verification Code⁴ 35-57

Data Cards

- 1-6 **Binary Address**
- 8-12 First row of character
- Second row of character 14-18
- 20-24 Third row of character
- Fourth row of character 26-30
- 32-36 Fifth row of character
- Sixth row of character 38-42
- 44-48 Seventh row of character

Notes: 1. Assigned by Mostek Marketing Department; may be left blank.

- 2. Punched as 64x5x07 or 32x5x14.
- 3. "MOSTEK" format only is accepted on this part.
- 4. Punched as: (a) VERIFICATION HOLD i.e. the customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
 - (b) VERIFICATION PROCESS i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
 (c) VERIFICATION NOT NEEDED i.e. the customer will not receive a CVDS and production will
 - begin immediately.

Read Only

Memories