MCM4064AL
MCM4064L

Advance Information / New Product

64-BIT RANDOM ACCESS MEMORY

The MCM4064AL/4064L is a 64-Bit random access memory organized as a 16-word by 4-bit array. Schottky-diode-clamped transistors are utilized to obtain fast switching speeds, and Schottky clamp diodes are used on all inputs to provide minimum line reflection. The high speed of this memory makes it ideal in scratch pad operation.

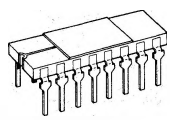
Address decoding is incorporated in the circuit providing 1-of-16 decoding from the four address lines. Separate Data In and Data Out lines, together with a Chip Enable, provide for easy expansion of memory capacity. A Write Enable is provided to enable data presented at the Data In lines to be entered at the addressed storage cells. When writing, Data Out is the complement of the Data In.

The open-collector output transistors are also Schottky barrier devices and combine greater current sinking capability with lower leakage currents, thereby increasing the wire-or capability of these devices.

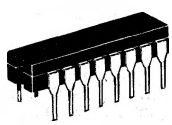
Features:

- Both Minimum and Maximum Access Times Specified
- Binary Addressing
- Chip Enable for Memory Expansion
- Outputs May Be "Wire ORed"
- Logic Levels Compatible with MDTL and All MTTL Families
- Low-Voltage Input Clamp Diodes
- Access Time < 60 ns
- Power Dissipation Typically 6 mW/bit
- Outputs Sink 15 mA

MTTL
64-BIT RANDOM ACCESS MEMORY



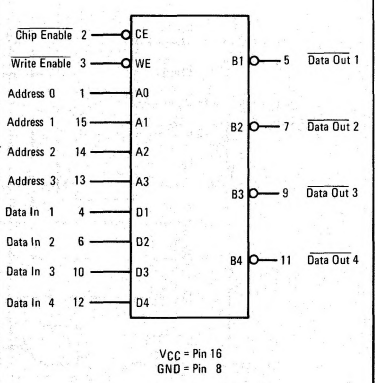
MCM4064AL
CASE 638



MCM4064L
CASE 620

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage – All Inputs	V_{in}	5.5	Vdc
Output Voltage – All Outputs	V_D	5.5	Vdc
Output Current	I_D	100	mAdc
Operating Temperature Range			
MCM4064AL (Case 638)	T_A	0 to +85	°C
Thermal Resistance, Junction to Ambient (Typical)	θ_{JA}	80	°C/W
Thermal Resistance, Junction to Case (Typical)	θ_{JC}	45	°C/W
MCM4064L (Case 620)	T_A	0 to +70	°C
Thermal Resistance, Junction to Ambient (Typical)	θ_{JA}	110	°C/W
Thermal Resistance, Junction to Case (Typical)	θ_{JC}	60	°C/W
Storage Temperature Range	T_{stg}	-65 to +160	°C



DC ELECTRICAL CHARACTERISTICS (MCM4064AL: (T_A = 0 to +85°C, Case 638;
MCM4064L: T_A = 0 to +70°C, Case 620)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Forward Current – All Inputs (V_{IL} = 0.4 Vdc, V_{CC} = 5.25 Vdc)	I_F	–	–	1.6	mAdc
Input Leakage Current – All Inputs (V_{IH} = V_{CC} = 5.25 Vdc)	I_R	–	–	80	μAdc
Input Clamp Voltage – All Inputs (I_{in} = -5.0 mAdc, V_{CC} = 4.75 Vdc)	V_C	–	–	-1.0	Vdc
Input Logic Levels – All Inputs					Vdc
(V_{CC} = 5.0 Vdc) "0" Level	V_{IL}	–	–	0.8	
"1" Level	V_{IH}	2.0	–	–	
Logic "0" Output Voltage – All Outputs (V_{CC} = 4.75 Vdc, I_{OL} = 15 mAdc)	V_{OL}	–	–	0.45	Vdc
Output Leakage Current – All Outputs (V_{CC} = V_{CEX} = 5.25 Vdc)	I_{CEX}	–	–	100	μAdc
Power Supply Current (V_{CC} = 5.25 Vdc, all inputs except WE grounded)*	I_{CC}	–	–	105	mAdc
Input Capacitance – All Inputs (V_{in} = 2.0 Vdc, V_{CC} = 5.0 Vdc)	C_{in}	–	6.0	–	pF
Output Capacitance – All Outputs (V_{out} = 2.0 Vdc, V_{CC} = 5.0 Vdc)	C_{out}	–	8.0	–	pF

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Access Times – Address Input or Chip Enable to Output Delay. (See Figures 1 and 2)	t_{A+B+}	15	–	60	ns
	t_{A-B-}	15	–	60	
	t_{A+B-}	15	–	60	
	t_{A-B+}	15	–	60	
	t_{CE+B+}	15	–	60	
	t_{CE-B-}	15	–	60	
Write Pulse Width (See Figures 1 and 3)	t_{wp}	40	–	–	ns
Write Recovery Time (See Figures 1 and 3)	t_{wr}	–	–	50	ns
Address and Data Hold Time After Write (See Figures 1 and 3)	t_{HAW}	5.0	–	–	ns

*Worst-case dc input condition.

BLOCK DIAGRAM

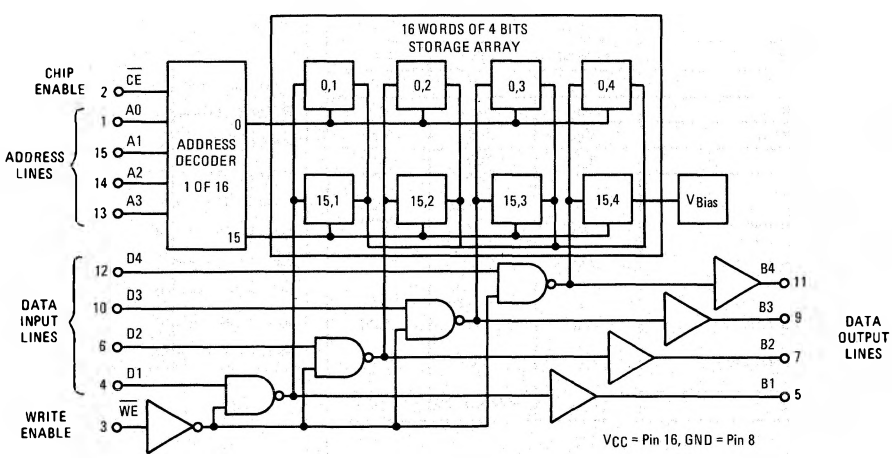


FIGURE 1 – SWITCHING TIME TEST CONDITIONS AND LOAD CIRCUIT

V_{CC} = 5.0 Vdc, T_A = 25°C

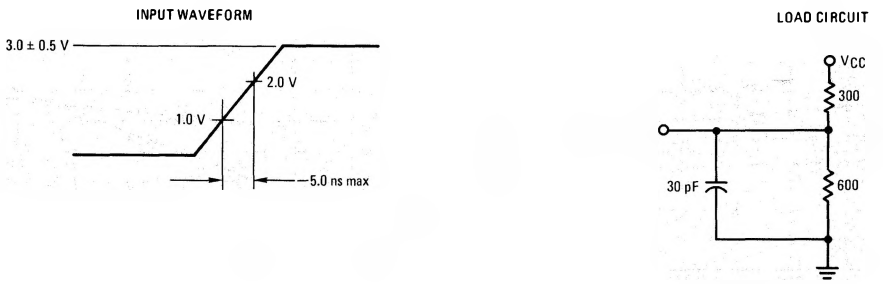
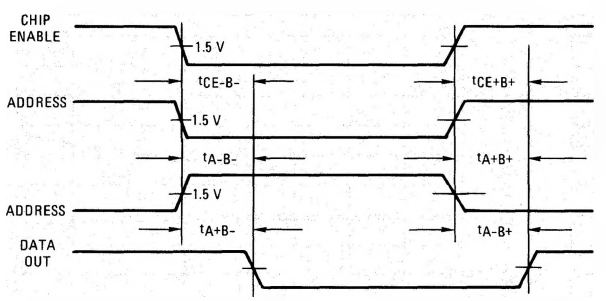


FIGURE 2 – ACCESS TIME DEFINITIONS



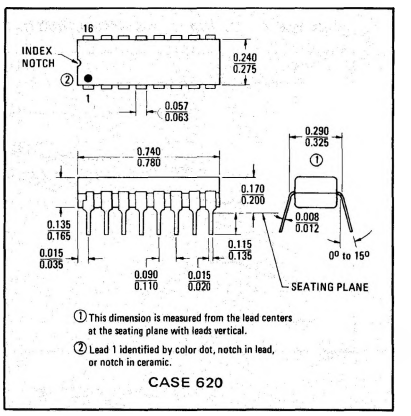
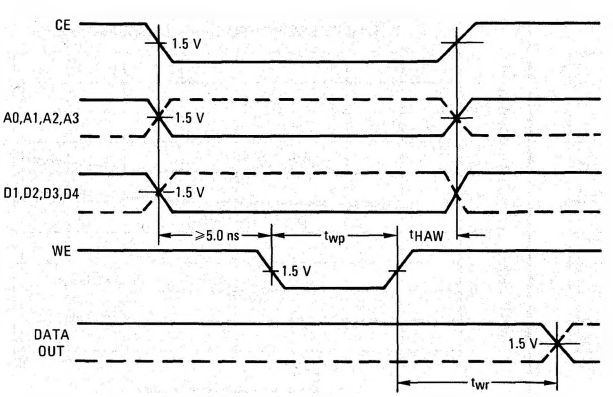
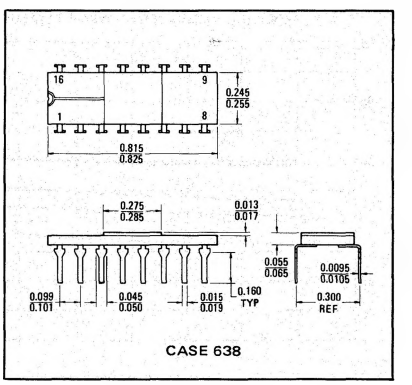


FIGURE 3 – WRITE TIME DEFINITIONS





TYPICAL ACCESS TIMES

ADDRESS TO OUTPUT

FIGURE 4 – VARIATIONS WITH SUPPLY VOLTAGE

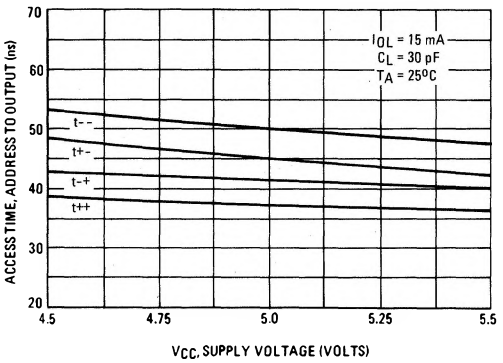


FIGURE 5 – VARIATIONS WITH LOAD CAPACITANCE

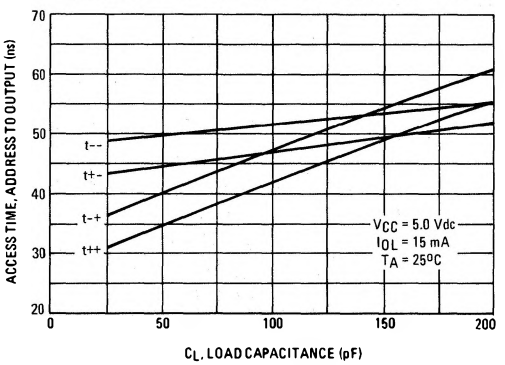
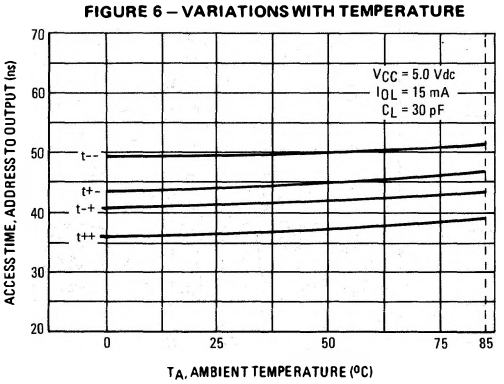


FIGURE 6 – VARIATIONS WITH TEMPERATURE



CHIP ENABLE TO OUTPUT

FIGURE 7 – VARIATIONS WITH LOAD CAPACITANCE

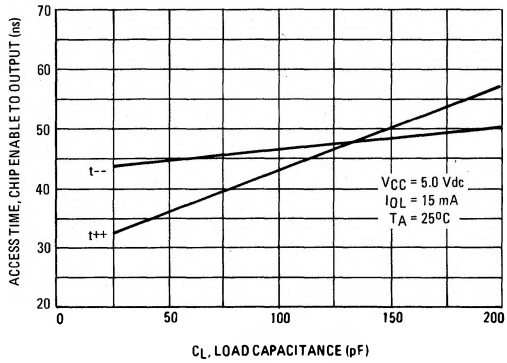


FIGURE 8 – VARIATIONS WITH TEMPERATURE

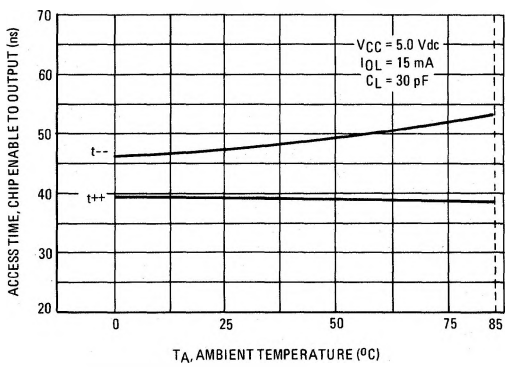
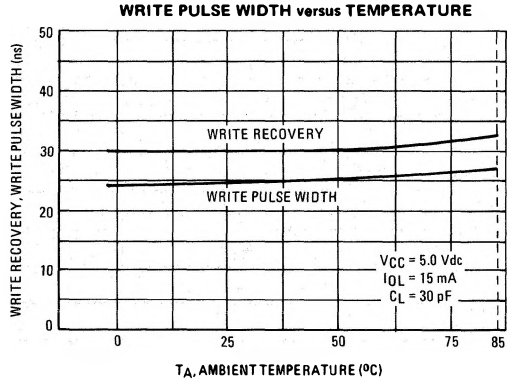


FIGURE 9 – TYPICAL WRITE RECOVERY AND WRITE PULSE WIDTH versus TEMPERATURE



TYPICAL DC CHARACTERISTICS

FIGURE 10 – TYPICAL SUPPLY CURRENT versus TEMPERATURE

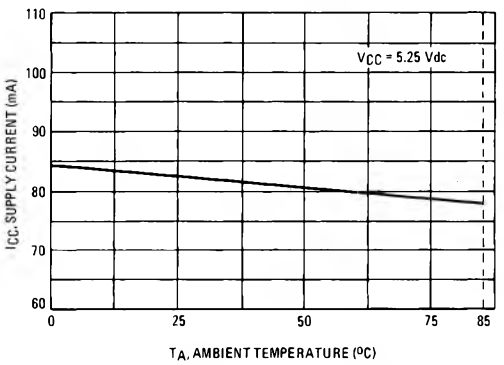
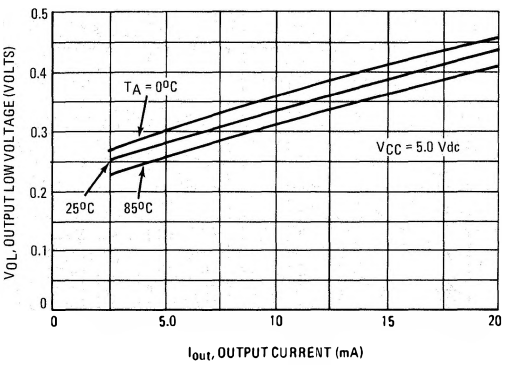


FIGURE 11 – TYPICAL OUTPUT LOW VOLTAGE versus OUTPUT CURRENT



APPLICATIONS INFORMATION

The MCM4064 64-bit MTTL RAM has several features which should be considered when designing larger systems with this device.

1. Chip Enable – This input essentially turns off the device when in the high state. The chip will neither read out nor write in data when disenabled. The open collector output devices allow Wire ORing or phantom logic for expansion into larger systems. Graphs in this data sheet show the relationship between access time and capacitance on the output due to Wire ORing.

2. Write Enable – The $\overline{WE}$ input gates the data on the data input leads into the memory cells. The output amplifiers are tied directly to the write amplifiers and follow as the inverse of the input for either state of $\overline{CE}$ as long as $\overline{WE}$ is low. There is, however, a "glitch" on the output lines just after $\overline{WE}$ returns high or goes low. For proper writing into the memory, the address and data hold time after writing (t_{HAW}) must be greater than 5.0 ns.

3. The address inputs have standard TTL-compatible input thresholds and standard TTL loading rules can be used.

The data outputs have open-collector, Schottky-clamped transistors and can be wire ORed with the incumbent cost in propagation delay. Typical output capacitance is specified for aid in system design.

Figure 12 shows a typical system design using TTL logic and the MCM4064 as a main frame store. This figure will be used to discuss several design considerations.

The four address inputs of the MCM4064 are common to all devices in the system. The gates driving these addresses have a fanout of eight, which is a typical and reasonable TTL fanout. In the diagram, each address driver shown represents four devices, one for each address. Thus, 8 x 4 or 32 inverters are required for address driving.

The chip enable inputs are used for further address expansion and a one-of-eight decoder (MC4006) is used for selecting one chip of eight with Wired OR outputs. Again a TTL fanout of eight is used. This chip enable decodings adds three address bits, A5, A6 and A7.

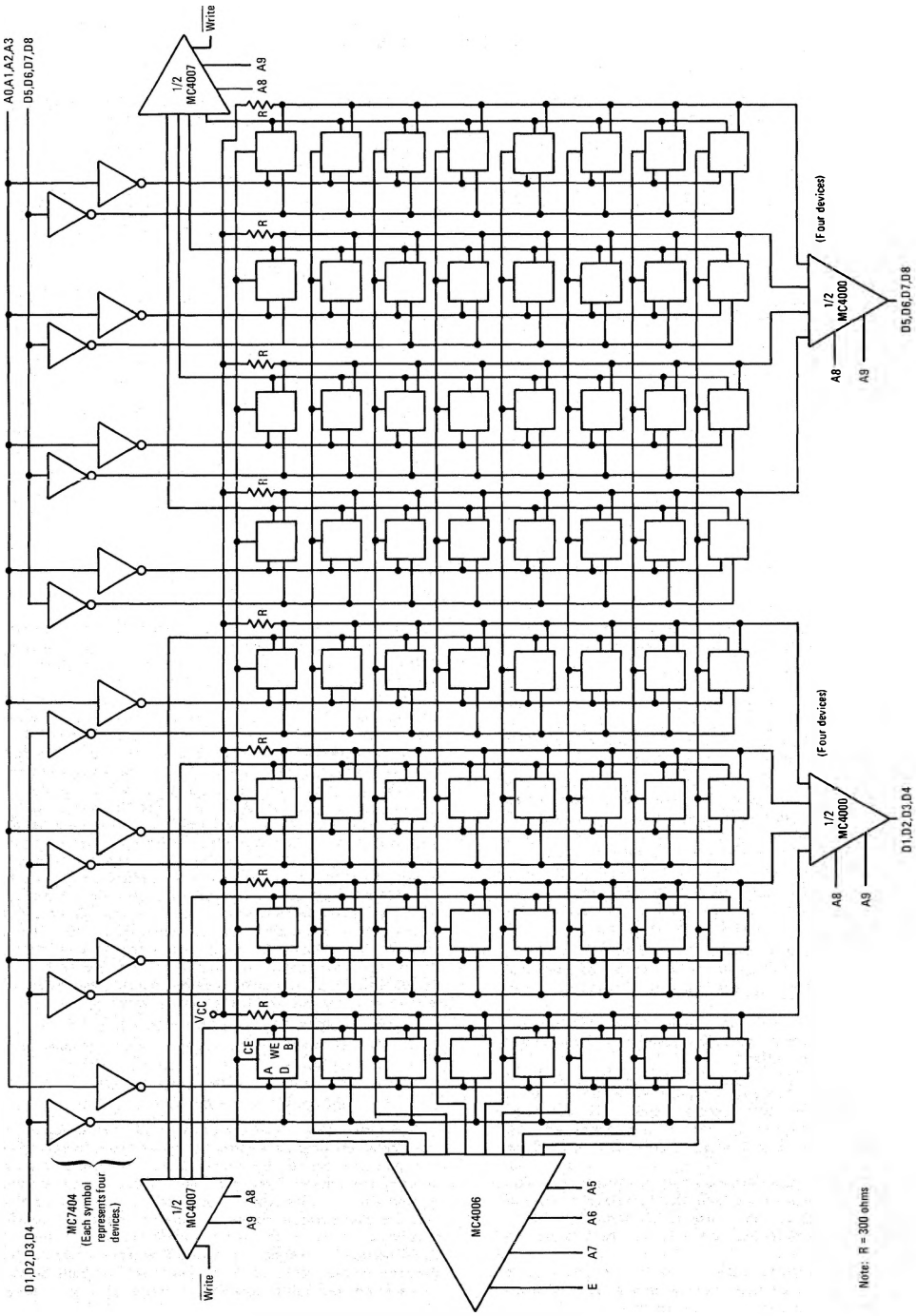
The memory chips are Wire-ORed in sections of eight. This figure of eight is used as a trade-off in decoding array time versus increase in access time due to output capacitance. The eight outputs at 8.0 pF each, plus an average of 5.0 pF for board capacitance give a total of slightly more than 100 pF for a total typical access time (from Figure 5) of about 50 ns. Each section of eight memory chips is connected to a one-of-four data selector (MC4000) which selects one of four sections. This adds a further two address bits, A8 and A9, for a total of 512 address locations. A one-of-four decoder is required for each data output and eight selectors, or four MC4000 devices, are required for the system. Four selectors give output bits D1 through D4 and the second set provides D5 through D8 from a second 8 x 4 array of memory devices.

The input data drivers shown in Figure 12 also represent four inverters, one for each data input bit, in the same manner as the address drivers and output selectors. The input data is distributed in common to both 8 x 4 memory arrays. The particular column of eight MCM4064's for which the data is intended is selected by the MC4007 data selectors which drive the write enable inputs. Only one of the eight MCM4064's in the columns will actually write in this data and is selected by the chip enable input. Thus only one device in the 8 x 4 array will actually accept the input data: that device chosen by the coincidence of the $\overline{CE}$ and $\overline{WE}$ lines.

The entire system shown, therefore, constitutes a 512-word by 8-bit memory and requires the following devices:

64	MCM4064	64 bit memories
4	MC4000	One-of-four data selectors
1	MC4006	One-of-eight decoders
1	MC4007	One-of-four decoders
11	MC7404	Hex inverters

The system access time is the total of the input decoding times, memory access times, and output selection delay times. However, this may be decreased for read-read cycles by utilizing the maximum and minimum access times. Thus, if one changes the address or chip enable inputs every 60 ns, there is at least 15 ns of valid data on the memory output. Therefore, an output buffering scheme which can latch up the memory contents within 15 ns could be used to reduce the read-read access time to 60 ns plus the address/chip enable skew times which are invariably present. A similar technique could be used for read-write and write-write cycles.


A0,A1,A2,A3
D5,D6,D7,D8
Write
1/2 MC4007
A8
A9
R
VCC
CE
WE
A
D
B
MC7404
(Each symbol represents four devices.)
D1,D2,D3,D4
MC4006
A5
A6
A7
E
(Four devices)
1/2 MC4000
D5,D6,D7,D8
D1,D2,D3,D4
Note: R = 300 ohms