

OPERATIONAL AMPLIFIERS

MCBC1741 MCB1741F

Advance Information

MONOLITHIC OPERATIONAL AMPLIFIER

Beam-lead sealed-junction technology and fabrication make the MCBC1741 and MCB1741F devices excellent choices for military, aerospace, and commercial applications; usages requiring a high degree of reliability under environmental conditions of severe temperature extremes, mechanical shock, and high humidity. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metalized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+22 -22	Vdc
Differential Input Signal	V_{in}	± 30	Volts
Common Mode Input Swing (Note 1)	CMV_{in}	± 15	Volts
Output Short Circuit Duration (Note 2)	I_S	Continuous	
Power Dissipation Derate above $T_A = +25^\circ\text{C}$ (Flat Package)	P_D	500 3.3	mW mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

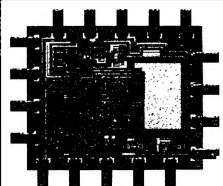
Note 2. Supply voltage equal to or less than 15 V.

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

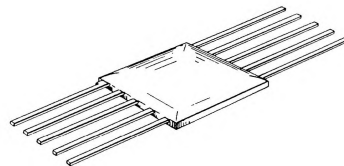
MONOLITHIC SILICON



BEAM LEAD



BEAM-LEAD CHIP
MCBC1741



MCB1741F
CASE 665
CERAMIC PACKAGE

SCHEMATIC PIN CONNECTIONS

Chip	A	B	C	D	E	F	G
"F" Package	2	3	4	5	6	7	8

FIGURE 1 — CIRCUIT SCHEMATIC

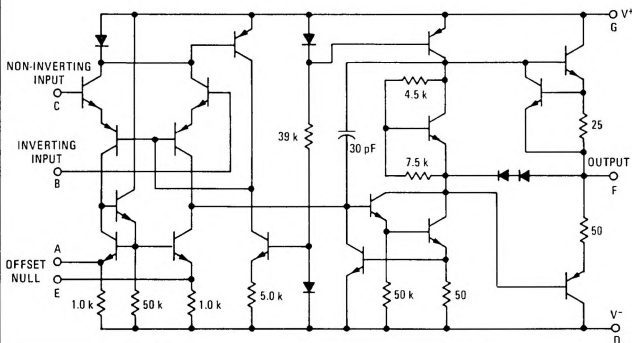
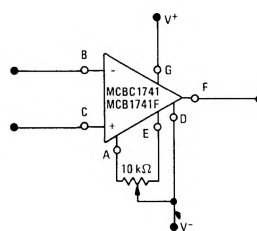


FIGURE 2 — OFFSET ADJUST CIRCUIT



This is advance information on a new introduction and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

MCBC1741, MCB1741F (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	MCBC1741, MCB1741F			Unit
		Min	Typ	Max	
Open Loop Voltage Gain ($R_L = 2.0\text{ k}\Omega$) ($V_O = \pm 10$ V, $T_A = +25^\circ\text{C}$) ($V_O = \pm 10$ V, $T_A = -55$ to $+125^\circ\text{C}$)	A_{VOL}	50,000 25,000	200,000 —	— —	—
Output Impedance ($f = 20$ Hz)	Z_O	—	75	—	Ω
Input Impedance ($f = 20$ Hz)	Z_{in}	0.3	1.0	—	Meg Ω
Output Voltage Swing ($R_L = 10\text{ k}\Omega$) ($R_L = 2.0\text{ k}\Omega$) ($R_L = 2.0\text{ k}\Omega$, $T_A = -55$ to $+125^\circ\text{C}$)	V_O	± 12 ± 10 ± 10	± 14 ± 13 —	— — —	V_{peak}
Input Common-Mode Voltage Swing	CMV_{in}	± 12	± 13	—	V_{peak}
Common-Mode Rejection Ratio ($f = 20$ Hz)	CM_{rej}	70	90	—	dB
Input Bias Current ($T_A = +25^\circ\text{C}$) ($T_A = -55^\circ\text{C}$)	I_b	— —	0.2 0.5	0.5 1.5	μA
Input Offset Current ($T_A = +25^\circ\text{C}$) ($T_A = -55$ to $+125^\circ\text{C}$)	$ I_{IO} $	— —	0.03 —	0.2 0.5	μA
Input Offset Voltage ($T_A = +25^\circ\text{C}$) ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)	$ V_{IO} $	— —	1.0 —	5.0 6.0	mV
Step Response Gain = 100, $R_1 = 1.0\text{ k}\Omega$, $R_2 = 100\text{ k}\Omega$, $R_3 = 1.0\text{ k}\Omega$	t_f t_{pd} dV_{out}/dt ①	— — —	29 8.5 1.0	— — —	μs μs V/ μs
Gain = 10, $R_1 = 1.0\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$, $R_3 = 1.0\text{ k}\Omega$	t_f t_{pd} dV_{out}/dt ①	— — —	3.0 1.0 1.0	— — —	μs μs V/ μs
Gain = 1, $R_1 = 10\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$, $R_3 = 5.0\text{ k}\Omega$	t_f t_{pd} dV_{out}/dt ①	— — —	0.6 0.38 0.8	— — —	μs μs V/ μs
Average Temperature Coefficient of Input Offset Voltage ($R_S = 50\text{ }\Omega$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$) ($R_S = 10\text{ k}\Omega$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)	$ TC_{VIO} $	— —	3.0 6.0	— —	$\mu\text{V}/^\circ\text{C}$
Average Temperature Coefficient of Input Offset Current ($T_A = -55$ to $+125^\circ\text{C}$)	$ TC_{VIO} $	—	50	—	pA/ $^\circ\text{C}$
DC Power Dissipation (Power Supply = ± 15 V, $V_O = 0$)	P_D	—	50	85	mW
Positive Supply Sensitivity (V^- constant)	S^+	—	30	150	$\mu\text{V}/\text{V}$
Negative Supply Sensitivity (V^+ constant)	S^-	—	30	150	$\mu\text{V}/\text{V}$
Power Bandwidth ($A_V = 1$, $R_L = 2.0\text{ k}\Omega$, THD = 5%, $V_O = 20\text{ V}_{p-p}$)	PBW	—	10	—	kHz

① dV_{out}/dt = Slew Rate

MCBC1741, MCB1741F (continued)

TYPICAL CHARACTERISTICS (continued)

($V^+ = +15\text{ Vdc}$, $V^- = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

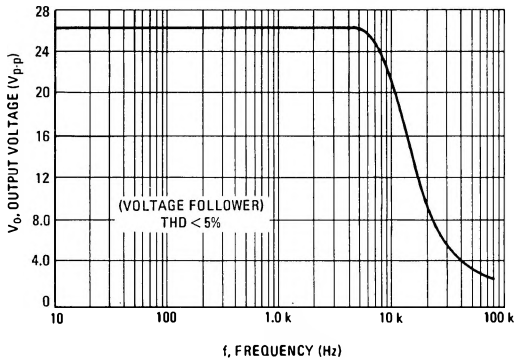


FIGURE 4 – OPEN LOOP FREQUENCY RESPONSE

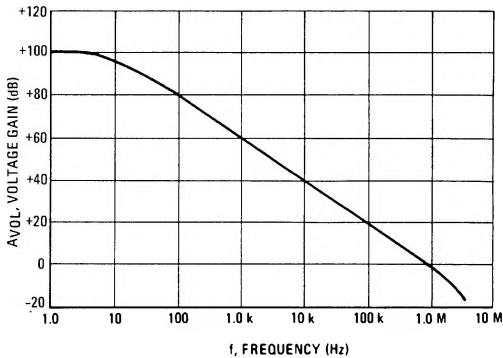


FIGURE 5 – OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

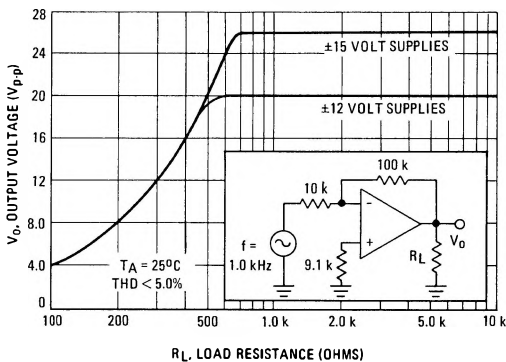


FIGURE 6 – COMMON-MODE REJECTION
RATIO versus FREQUENCY

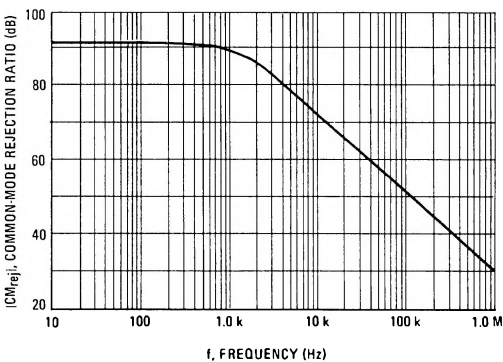


FIGURE 7 – INPUT OFFSET CURRENT
versus TEMPERATURE

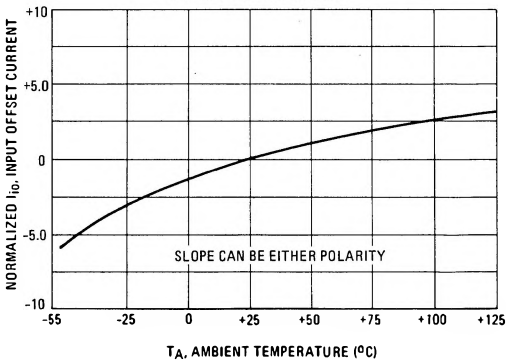
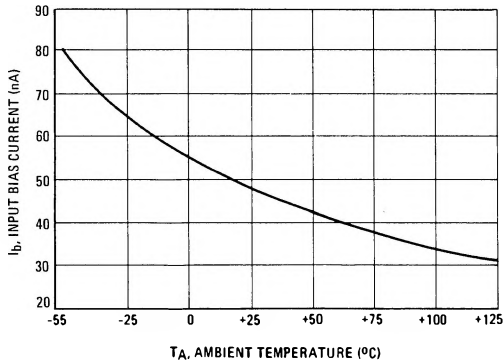


FIGURE 8 – INPUT BIAS CURRENT
versus TEMPERATURE



MCBC1741, MCB1741F (continued)

TYPICAL CHARACTERISTICS (continued)

($V^+ = +15\text{ Vdc}$, $V^- = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 9 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

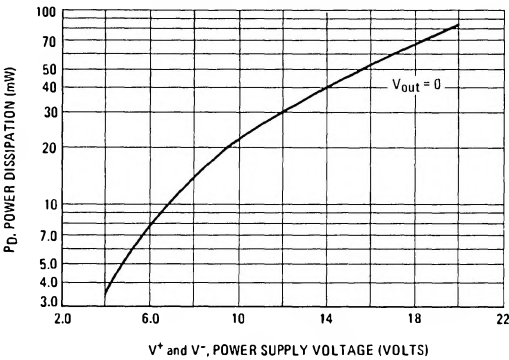


FIGURE 10 – OUTPUT NOISE versus SOURCE RESISTANCE

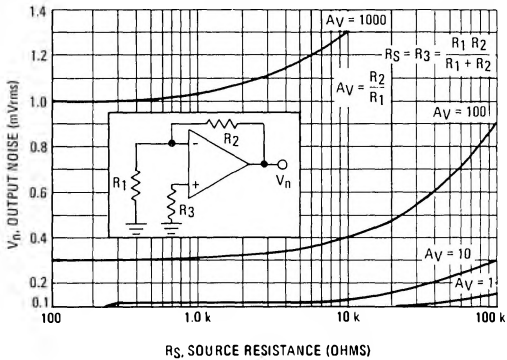
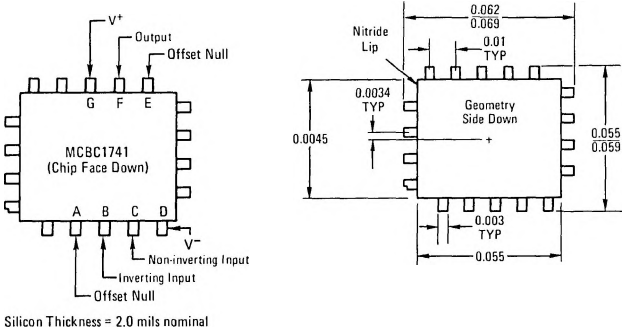


FIGURE 11 – BONDING DIAGRAM



PACKAGING AND HANDLING

The MCBC1741 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.