# MC5400/7400 series

## **DECADE COUNTER**

# MC5490F, L\* MC7490F, L,P\*

#### RESET/COUNT TRUTH TABLE

R	RO R9				OUT	PUT	
Pin 2	Pin 3	Pin 6	Pin 7	<b>Q</b> 3	Q2	Q1	00
1	T1	0	×	0	0	0	0
1	1	×	0	0	0	0	0
×	) ×	1	1	1 1	0	0	1
×	0	×	-0		COL	TNL	
٥	×	0	×		COL	JNT	
0	×	×	0		COL	JNT	
×	0	0	×		COL	JNT	

X = Don't care.

# COUNT SEQUENCE TRUTH TABLE

COUNT		OUT	PUT	
COUNT	Q3	Ω2	Q1	00
0	0	0	0	0
1 1	0	0	0	1
2	0	0	1 1	0
3		0	1 1	1
4	0	1	0	0
5		1	0	1
6	0	1	1	0
7	0	1	1 1	1
8	1	0	0	0
9	1	0	lol	1

Q0 connected to C1.

Input Loading Factor:

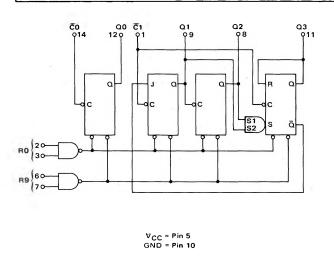
RO, R9 = 1 C0 = 2

₹1 = 4

Output Loading Factor = 10

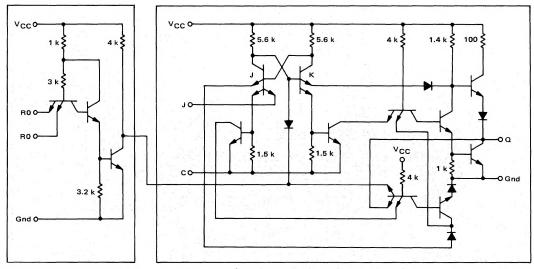
Total Power Dissipation = 160 mW typ/pkg Propagation Delay Time = 20 ns typ/bit

This 4-bit counter is comprised of a divide-by-two section and a divide-by-five section. These sections can be used independently, or can be connected to perform the counting function or the simple divide-byten function with an output duty cycle of 50%. Two sets of direct RESET inputs are provided to allow setting all outputs to a logic "0" or to the BCD count of 9.



# TYPICAL RESET GATE

# TYPICAL FLIP-FLOP

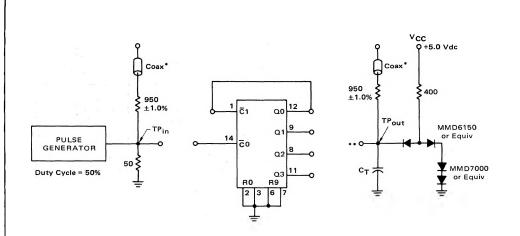


<sup>\*</sup>F suffix = TO-86 ceramic flat package (Case 607). L suffix = TO-116 ceramic dual in-line package (Case 632). P suffix = TO-116 plastic dual in-line package (Case 605).

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Symbol   Tested in the same   MC490   State	ELECTRICAL CHARACTERISTICS	ACTER	ISTICS	•						5.		TEST C	URREN	0/ 7	TAGE	VALUE	TEST CURRENT / VOLTAGE VALUES (All Temperatures)	erature	8				
MC5490   Test limits   MC7490   Test limits   Test Current / Volt / Mc4   Very   V	Test procedures are sho	wn for o	nly one							E	Ą					%	ts						
Properties   Pro	of each reset gate is ter	sted in th	e same							ام	_ĕ		>	V IH		۷ په ۱	۷* ه	V <sub>th L</sub>	20		V <sub>CCH</sub>		
ite Symbol Test limits MC490 T	manner.								MC5490		-0.4	0.4	2.4	5.5		2.0	0.8	0.7	5.0		5.5		
tic Symbol Test MC490Test Limits MC490T									MC/490	16	-0.4	-	2.4	5.5	4.5	2.0	0.8	9.0	2.0	4.75	5.25		
1			Pin Under		490 Test 5 to +1;	Limits 25°C	D <sub>N</sub>	7490 Tes	t Limits 0°C			TEST CL	IRRENT	/ VOLT	AGE A	PPLIED	TO PINS LI	STED BE	LOW:		-	Pulce	
1 Fig. 1 F. 2	Characteristic	Symbol			Max	Unit	Ä	_	-tim	ام ا	-ы	V <sub>II</sub>		/ HH		۸ په ۱	۷# ۰	V# L	νςς		VCCH	-	Gnd
Fig.			·			m Ado		4	m Ado							ž ų			9.5		u		5
\$\text{At \$0}\$ \$\text{Big}\$ \$\text{Right}\$ \$R		H	9 41	1.1	-1.6	-	y i	-1.6		1		9 4	1,1	1 1	) <u> -</u>			1.7	17	, i	,		10
RB 1R1 6 6	SIC		1	. "	-6.4	-	. '	-6.4	-	1	,	1		1	-	. 1	-	-1		,	-		2,10
© © 0		IRI	20.00	1 1	40	μAde		40	μAdc	1 1		1 1	2.6	, ,		13	1 1	101	1 1	i i	- 22		3,10
R0	1010		14	1.1	80	-		80	-		<u>.</u>	1.1	14		, ;	1.1		1.1	1 1	1.1	-		1000
Qu ① Vol. 12 - 0.4 Vdc - 0.4 Vdc 112 14 5 5 - 17   14 5   15   15   15   15   15   15   1	RO	I <sub>R2</sub>	2 0	1	1.0	mAdc		1.0	mAdc		1	1	1	27 0			1		1.		2		3,10
Qu ⊕ Vol. 12 -	R 00		14				i		8.	1 1		1 1	, ,	14	1 1	1 1			i ,		_	1 1	7,10
Qu ① Vol. 12 - 0.4 Vde - 18 -57 mAde - 12 - 0.4 Vde 12 - 0 - 0 - 0.4 Vde 12 - 0 - 0 - 0 - 0 - 0 - 0 - 0 - 0 - 0 -	SIC		-		-	-		-	•		1	1	1	-	1	,	1		1	1	-		10
1 Sc		NOL	- 12	* P* .	0.4	Vdc	100	0.4	Vdc	12				1		2,3,14	6.7		. Gr	വ	ir .	. 1	10
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Short-Circuit Current	¹sc		-20	-57	mAdc		-57	mAdc	1	1	1 -	1,	4	1.	1	2,3,6,7	14	1	. 1	ro	14	10,12
1 ⊕ V <sub>OL</sub> 9 - 0.4 Vdc - 18 -57 mAdc - 1 0.4 Vdc 9 2.3 6.7 1 - 5    V <sub>OH</sub>	Output Voltage	VOH	•	2.4		Vdc	2.4		Vdc		12			1	1	:	2,3,6,7,14	ı,	-1	S	1		10
1 sc	Q1 (I)	VOL	6-		0.4	Vdc	1	0.4	Vdc	6	1	i	. 1	TY.		2,3	6,7	1	i.	2	,		10
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		1sc		-20	-57	mAdc		-57	mAdc	1	1	1	. ·		•		2,3,6,7	1	ı	1	വ	ч	9,10
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		МОН	•	2.4	1	Vdc	2.4		Vdc	1	6	91		1	1	•	2,3,6,7	-	1	2		- 1	10
1 Sc	Q2 ①	VOL	- α	1,3	0.4	Vdc	1	0.4	Vdc	∞	. '	,			. 1	i.	2,3,6,7	1	1	2	7	,	10
V <sub>OH</sub>		, sc		-20	-57	mAdc		-57	mAdc	ı		i in				ï	7	i	1.	1	2	-	8,10
3 ⊕ V <sub>OL</sub> 11 - 0.4 Vdc - 0.4 Vdc 11 2,3.6,7 1 - 5 I <sub>SC</sub>		Мон	-	2.4	1	Vdc	2.4	i	Vdc	1	80	1	1			ı,	-	1		2	1 -	1	10
<sup>1</sup> SC	Q3 ①		11	i	0.4	Vdc		0.4	Vdc	11	i'.	1	1		1		2,3,6,7	1		2	,		10
V <sub>OH</sub> v 2.4 - V <sub>dc</sub> 2.4 - V <sub>dc</sub> - 11 6,7 2,3 v - 5		ISC		-20	-57	mAdc		-57	mAdc	1		-1	.1	1	. 1.	6,7	2,3	4.1	i	1.	2		10,11
		Мон	•	2.4	•	Vdc	2.4		Vdc	1	11	1	d.	1.	ı	2.9	2,3	-	11	ည	i	1	10
	Power Requirements (Total Device)									5									l la				
TpD c dql	Power Supply Drain	IPD	2	i.	46	mAdc	1	53	mAdc			1	ī	- I.,	1		,	. 1	1		2	i	6,7,10

## SWITCHING TIME TEST CIRCUIT



 $f_{Tog} = 10 \text{ MHz min}$ 

 $C_T$  = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

- <sup>a</sup>The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.
- \*\*A load is connected to each output during the test.

# **VOLTAGE WAVEFORMS AND DEFINITIONS**

