

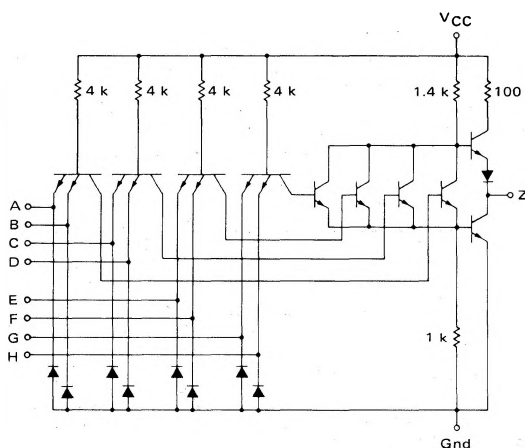
4-WIDE 2-INPUT
"AND-OR-INVERT" GATE

MC5400/7400 series

MC5454 • MC7454

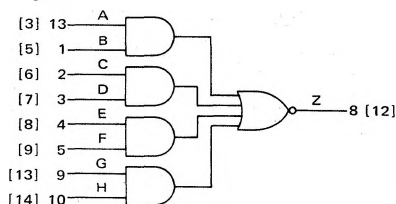
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7454 only.

CIRCUIT SCHEMATIC



VCC = Pin 14 [4]
Gnd = Pin 7 [11]

[FLAT] DIL
Pkg Pkg
Pin Pin



Positive Logic:

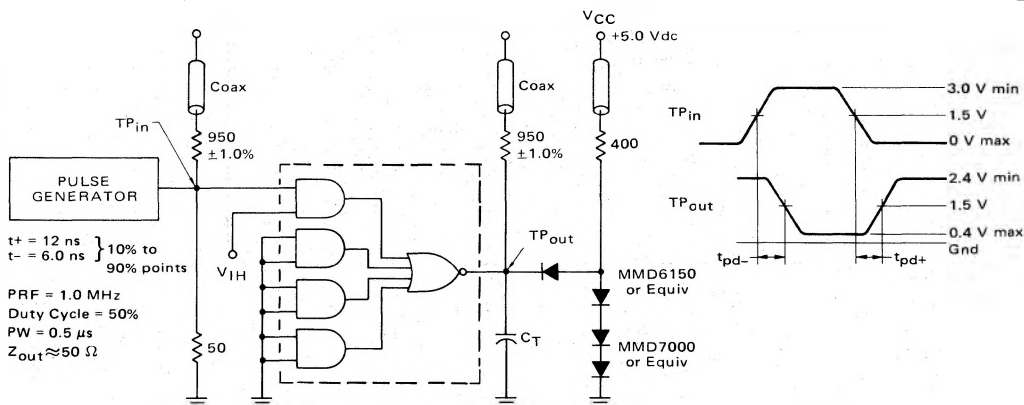
$$Z = (A \bullet B) + (C \bullet D) + (E \bullet F) + (G \bullet H)$$

Negative Logic:

$$Z = (A + B) \bullet (C + D) \bullet (E + F) \bullet (G + H)$$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 22 mW typ/pkg
Propagation Delay Time = 13 ns typ

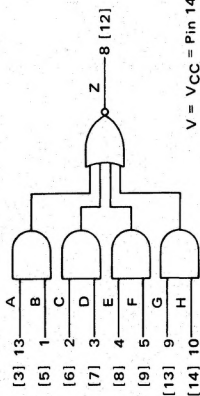
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



$C_T = 15$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

[FLAT]	DIL
Pkg	Pkg
Pin	Pin



Test procedures are shown for only one input. To complete testing, sequence through remaining inputs in the same manner.

$V = V_{CC} = \text{Pin } 14 [4]$
 $\text{Gnd} = \text{Pin } 7 [11]$

[illegible]

† Only one output should be shorted at a time.

*Tested only at 25°C.