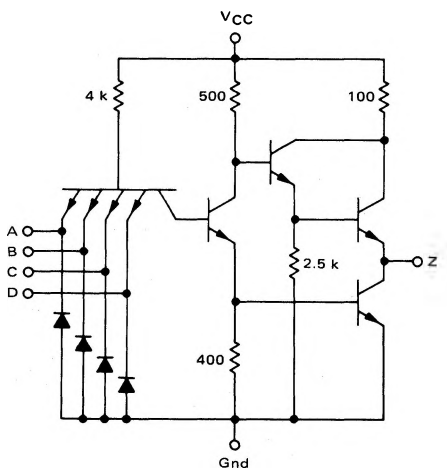
DUAL 4-INPUT "NAND" BUFFER

MC5440 • MC7440

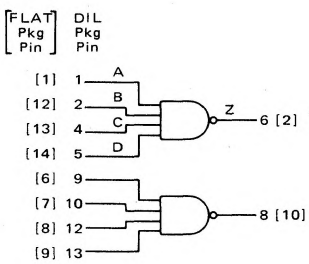
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7440 only.

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

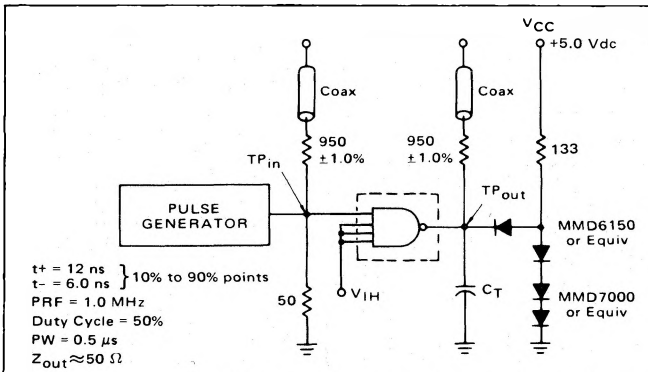
This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (30).

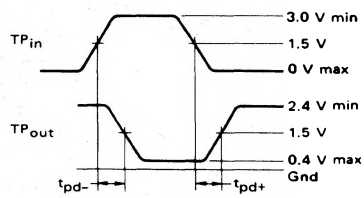


Positive Logic: $Z = \overline{A \bullet B \bullet C \bullet D}$
Negative Logic: $Z = \overline{A + B + C + D}$

Input Loading Factor = 1
Output Loading Factor = 30
Total Power Dissipation = 50 mW typ/pkg
Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



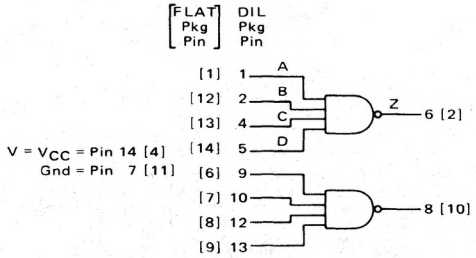


C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}
MC5440	48	-1.2	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
MC7440	48	-1.2	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5440 Test Limits −55 to +125°C Min	Max	Unit	MC7440 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	-	A	-	-	B,C,D	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	-	A	-	-	-	-	-	-	-	V	B,C,D*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	A	-	-	-	-	-	-	V	B,C,D*
Output																					
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	A,B,C,D	-	-	V	-	*
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	B,C,D	-	-	A	-	V	-	*
Short-Circuit Current	I_{SC}†	Z	-20	-70	mAdc	-18	-70	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B,D,D,Z*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	V	-	27	mAdc	-	27	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B,C,D*
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	-	B,C,D	-	-	-	-	-	V	-	-	*
Turn-Off Delay	t_{pd+}	A,Z	-	22**	ns	-	22**	ns	A	Z	-	B,C,D	-	-	-	-	-	V	-	-	*

Pin 7[11] is grounded for all tests in addition to the pins listed below:

*Ground inputs to gate not under test.
**Tested only at 25°C.
†Only one output should be shorted at a time.