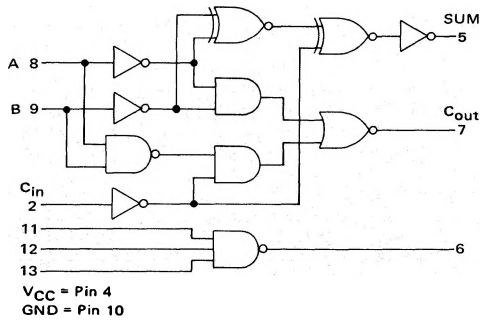
MC4326F,L • MC4327F,L*
MC4026F,L,P • MC4027F,L,P*



These full adders are designed for serial and ripple-carry parallel adder systems. True Sum and Carry are produced at the output from the input information. A separate 3-input NAND gate is provided on the monolithic chip to provide the inverted Sum or Carry output.

Input Loading Factor:
A, B = 2
C_{in}, Pins 11, 12, 13 = 1

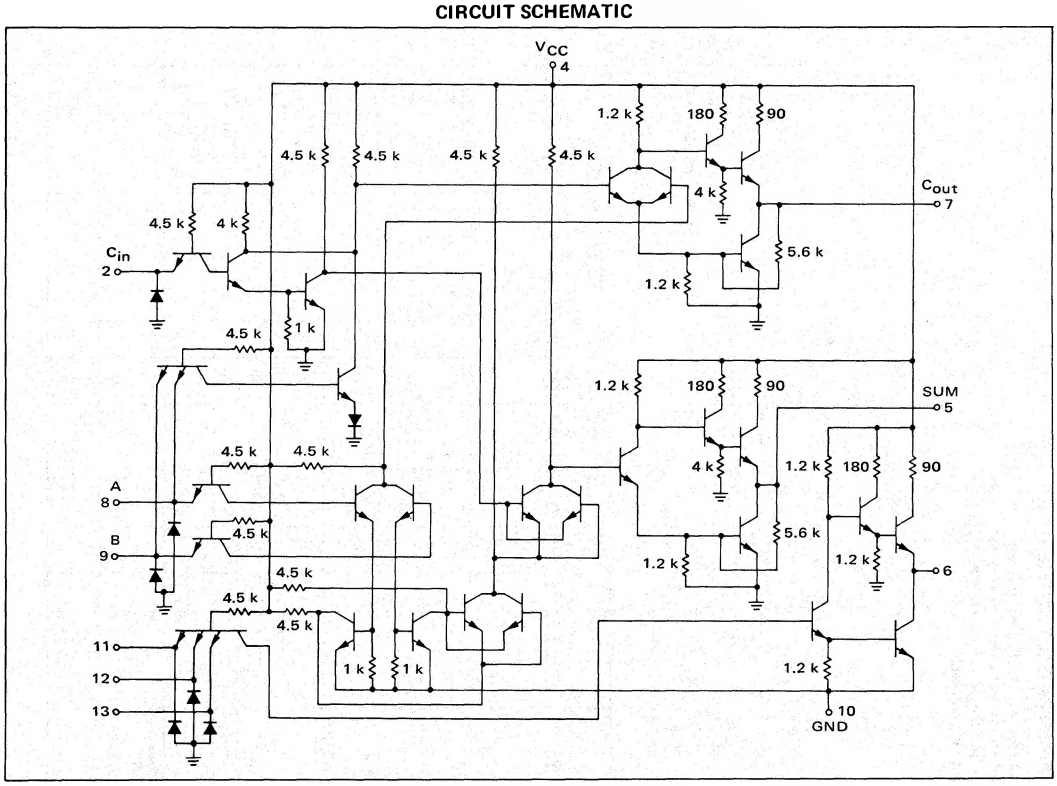
Output Loading Factor:
MC4326 = 15 MTTL I Loads
MC4327 = 7 MTTL I Loads
MC4026 = 12 MTTL I Loads
MC4027 = 6 MTTL I Loads

TRUTH TABLE

Input Pins			Output Pins	
8	9	2	5	7
A	B	C_{in}	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Total Power Dissipation = 90 mW typ/pkg
Add Delay = 25 ns typ
Carry Delay = 13 ns typ

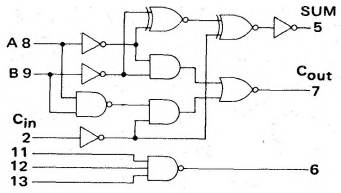
CIRCUIT SCHEMATIC



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for inputs A and C_{in}. Other inputs are tested in the same manner. Output tests should be completed according to the truth table.

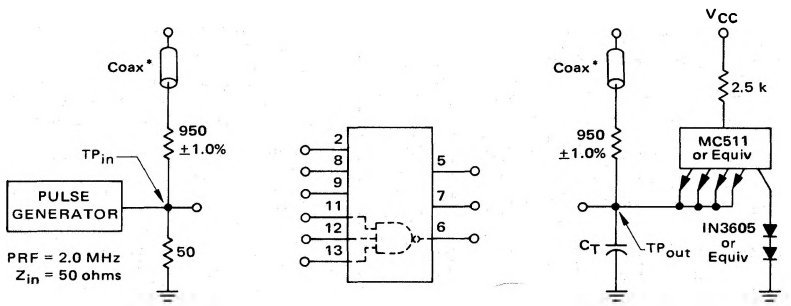


	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES: mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	Volts I_{in}	$2I_{in}$	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{max}	V_{CC}
MC4326*, MC4327	−55°C	20	10	-2.2	-1.2	-	-	0.45	2.8	4.5	2.0	0.9	5.5	-	5.0
	+25°C	20	10	-2.2	-1.2	1.0	2.0	0.45	2.8	4.5	1.7	1.0	5.5	8.0	5.0
	+125°C	20	10	-2.2	-1.2	-	-	0.45	2.8	4.5	1.4	0.8	5.5	-	5.0
MC4026*, MC4027	0°C	20	10	-2.2	-1.2	-	-	0.45	3.0	4.5	1.9	1.0	5.5	-	5.0
	+25°C	20	10	-2.2	-1.2	1.0	2.0	0.45	3.0	4.5	1.8	1.0	5.5	7.0	5.0
	+75°C	20	10	-2.2	-1.2	-	-	0.45	3.0	4.5	1.7	1.0	5.5	-	5.0

Characteristic	Symbol	Pin Under Test	MC4326, MC4327 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4026, MC4027 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{max}	V_{CC}	Gnd
Input																												
Forward Current	I_F	2	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	8,9,11,12,13	-	-	-	-	4	2,10
		8	-	-2.66	-	-2.66	-	-2.66	-	-3.32	-	-3.32	-	-3.32	mAdc	-	-	-	-	-	-	2,9,11,12,13	-	-	-	-	4	8,10
Leakage Current	I_R	2	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	2	-	-	-	-	4	8,9,10,11,12,13
		8	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	-	8	-	-	-	-	4	2,9,10,11,12,13
Inverse Beta Current	I_L	2	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	2	-	-	-	-	4	10
		8	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	-	8	-	-	-	-	4	10
Breakdown Voltage	BV_{in}	2	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	-	-	-	4	8,9,10,11,12,13
		2	-	-	↓	-	-	-	-	-	↓	-	-	-		-	-	2	-	-	-	-	-	-	-	-	4	10
		8	-	-		-	-	-	-	-		-	-	-		-	-	-	8	-	-	-	-	-	-	-	4	2,9,10,11,12,13
		8	-	-		-	-	-	-	-		-	-	-	↓	-	-	-	8	-	-	-	-	-	-	-	4	10
Output																												
Output Voltage	V_{out} "0"	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	5	-	-	-	-	-	-	-	2,8,9	-	-	4	10
	V_{out} "1"	5	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	5	-	-	-	-	-	2	8,9	-	-	4	10
Leakage Current	I_{OLK}	5	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	2,8,9	-	-	-	5	-	4	10
Short-Circuit Current	I_{SC}	5	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	2,8,9	-	-	-	-	-	4	5,10
Output Voltage	V_{OL}	5	-	0.4	-	0.4	-	0.45	-	0.4	-	0.4	-	0.45	Vdc	5	-	-	-	2,8,9	-	-	-	-	-	-	4	10
	V_{OH}	5	2.8	-	3.1	-	3.15	-	3.0	-	3.1	-	3.15	-	Vdc	-	5	-	-	-	2,8,9	-	-	-	-	-	4	10
Power Requirements (Total Device)																												
Maximum Power Supply Current	I_{max}	4	-	-	-	38	-	-	-	-	-	47	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	2,8,9,10,11,12,13
Power Supply Drain	I_{PDH}	4	-	27	-	27	-	27	-	35	-	35	-	35	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	10
	I_{PDL}	4	-	32	-	32	-	32	-	41	-	41	-	41	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	2,8,9,10,11,12,13

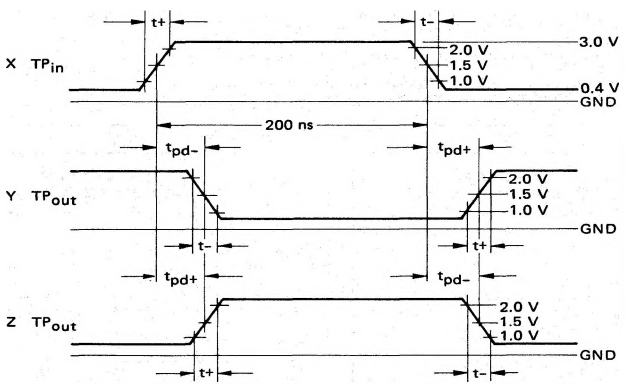
*Prime Fan-Out

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	PINS UNDER TEST (In/Out)	INPUT PIN					OUTPUT PIN			LIMITS
		8 A	9 B	11	12	13	5 SUM	6	7 C_{out}	ns max
t_{pd+}	9/5	Open	X	Open	Open	Open	Z	–	–	35
t_{pd-}	9/5	Open	X	Open	Open	Open	Z	–	–	35
t_{pd+}	11/6	Open	Open	X	3.0 V	3.0 V	–	Y	–	20
t_{pd-}	11/6	Open	Open	X	3.0 V	3.0 V	–	Y	–	20
t_{pd+}	8, 9/7	X	X	Open	Open	Open	–	–	Z	20
t_{pd-}	8, 9/7	X	X	Open	Open	Open	–	–	Z	20
t+	Tested during each of the above tests.									8.0
t-										5.0