



This device consists of seven Exclusive NOR gates connected to check even parity. The output will be in the logic "1" state as long as the "1" state is present on an even number of inputs. The additional Exclusive NOR gate can be used to connect two 8-bit parity trees to form a 16-bit parity tree, or it can be used to convert the parity tree to check odd parity by connecting one gate input to the output of the parity tree and grounding the other input. This conversion can also be accomplished by connecting a simple inverter to the output of the parity tree.

> Input Loading Factor = 2 Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg Propagation Delay Time = 15-30 ns typ



t_{pd-} (1 Gate)

150

120

TYPICAL PROPAGATION DELAY TIMES

*F suffix = TO-86 ceramic flat package (Case 607).

V_{CC} = 5.0 Vdc

30

 $T_A = 25^{\circ}C$ Fan-Out = 1 = 25°C

24

20

16

12

o

L suffix = TO-116 ceramic dual in-line package (Case 632). P suffix = TO-116 plastic dual in-line package (Case 605).

60

tpd+ (1 Gate

90

CL, LOAD CAPACITANCE (pF)



TA, AMBIENT TEMPERATURE (°C)



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and output in the same manes. To com-plete testing, test all input-output combina-tions according to the logic equation.



								TEST CUR	RENT	VOLT	AGE	VALUE	S						
				2	An							Volt	s		-				
		© Test Temperatur	1011 a	1012	HOI	lin	9	VIL	HIV	٧F	V _R	VRH	Vmax	VCC	VCCL	VCCH	ХНІУ		
		-55°	c 16	18.4	-1.6	1	1	1.1	2.0	0.4	2.4	4.0	į	5.0	4.5	5.5	-		-
MC43	80	+25°	c 16	18.4	-1.6	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.4		
		+1250	c 16	18.4	-1.6	1	1	0.8	1.8	0.4	2.4	4.0	ŀ	5.0	4.5	5.5	1		
		00	c 16	17.6	-1.6	1	1	1.1	2.0	0.4	2.5	4.0	1	5.0	4.75	5.25	I		
MC40	8	+260	c 16	17.6	-1.6	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.4		
		+75%	c 16	17.6	-1.6	1	1	0.9	1.8	0.4	2.5	4.0	1	5.0	4.75	5.25	T		
Test Limi	2						TEST	T CUBBENT/VOLT	AGE AF	11 Ide	DIC	DINS L	STED B	FLOW					
5°C	+750	0					1				[t			_
Max 1	Ain A	Max Unit	1701	1012	но	-in	9	VIL	HIN	4	ς,	VRH	Vmax	vcc	VCCL	VCCH	VIHX	Gnd	
-3.2	1	3.2 mAd	1	1	1	1	1	I	1	1	1	13	1	1	1	14	1	7	
80	1	80 µAdd	1	1	1	1	1	1	1	1	-	1	1	1	1	14	1	7,13	
-1	1	- Vdc	1	1	1	-	1	1	1	1	1	1	1	1	1	14	1	7,13	
-1.5	1	- Vdc	1	1	I.	1	-	1	1	1	1	1	1	1	14	ł,	-	7	
	-																		_

												Ĩ		-			0.11		2.1	2	1.1	0.1	+ 5	2.4	2.	2.1	2.0	2	0.40	1.1	
														-	+75°C	16	17.6	-1.6	1	1	0.9	1.8	0.4	2.5	4.0	1	5.0	4.75	5.25	I	
		ä		MC	34308	Test L	imits			Ŵ	C4008	Test L	imits							Ĩ	ST CURRENT/VOLTE	GE A	PPLIEL	TO	INS LI	STED	BELOW				
		Under	ľ	55°C	÷	20°2	Ŧ	25°C		000	Ŧ	25°C	£+	5°C				-	F					T							
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Mir	Max	Min	Max	Min	Max	Unit	1701	10L2	HOI	1 lin	9	VIL	HIN	۲F	ч К	VRH	Vmax	VCC	VCCL	VCCH	VIHX	Gnd
Input Forward Current	L.	-	1	-3.2	1	-3.2	1	-3.2	1	-3.2	1	-3.2	1	-3.2	mAdo	1	1	1	1	I	-	1	-	1	13	1	1	1	14	1	7
Leakage Current	8	F	1	80	Ĩ	8	1	80	I.	80	1	80	1	80	μAdc	1	1	!	1	1	1	1	1	-	1	1	1	1	14	1	7,13
Breakdown Voltage	BVin	-	1	1	5.5	i	1	1	1	1	5.5	1	1	1	Vdc	1	1	1	-	1	1	1	1	1	1	1	1	1	14	1	7,13
Clamp Voltage	^Q N	-	1	1	1	-1.5	1	1	1:	1	1	-1.5	1.	1	Vdc	1	1	1	1	-	1	1	1	1	1	1	1	14	1	1	7
Output Output Voltage	NoL		artí.	0.4	11	0.4	L	0.4	. 1.	0.4	1	0.4	1	0.4	Vdc	80	10	1	. 1	1	2,3,9,10,11,12,13		1	1	1	1.	-1	1	14	1	7
		8	1	0.4	1	0.4	1	0.4	1	0.4	1	0.4	1	0.4	Vdc	1	8	1	1	1	2,3,9,10,11,12,13	-	1	1	1	1	1	14	1	-	
	NOH	80	2.4	-	2.4	1	2.4	E.	2.5	1	2.5	-	2.5	1	Vdc	-	1	8	-	1	1,2,3,9,10,11,12,13	1	-	1	1	1	1	4	1	1	7
Short-Circuit Current	Isc	80	-20	-65	-20	-65	-20	-65	20	-65	-20	-65	-20	-65	mAdc	1	1	1	1	1	1,2,3,9,10,11,12,13	i	ł	1	1	1	14	1	1	-	7,8
Power Requirements (Total Device) Maximum Power Supply Current	Imax	4	1. 1.	1	1. J.	28		i I	. 1	1		28	1	1	mAdc	I	1	1	1	1	2 - 1 - 8-	ł	I.	1	5,13	14	1	1		1	1,2,3,4,7 9,10,11,12
Power Supply Drain	Odi	14	1	1	15	45	1	1	1	1	1	45	1	1	mAdc	1	1	1	1	1	I ·	1	I	1	5,13	Ι.,	14	1	1	1	1,2,3,4,7 9,10,11,12
Switching Parameters	1.1.1			1	3	4.2			-							Pul	se In	Puls	e Out											1	
Turn-On Delay	t-bd-1	1,8	1	1	1	46	1	1	1	1	1	46	1	1	su		-		8	1	.1.	1	1	1	1	1	14	1	1	2,3,9,10,11,12	7,13
	tpd-2	4,6	1	1	1	23	1	1	1	1	1	23	1	1	su		4		9	J	-	1	1	1	1	1	14	1	!	1.	5,7
Turn-Off Delay	t+bd+1	1,8	1	1	1	46	1	I	1	1	1	46	1	1	su		-		80	1	1	1	I	1	1	1	14	1	1	2,3,9,10,11,12	7
	tpd+2	4,6	1	1	1	23	1	1	1	1	1	23	1	1	su		4		9	I	-	I.	1	1	1	١	14	1	1	+	5,7

MC4308F,L, MC4008F,L,P (continued)

MC4308 MC4308 MC4008 MC4008 INPUT OUTPUT INPUT OUTPUT LOADING LOADING LOADING LOADING FAMILY FACTOR FACTOR FAMILY FACTOR FACTOR MC4300 1.0 10 MC4000 10 10 MC500 1.2 12 MC400 1.0 10 MC2100 0.8 8 MC2000 0.67 6 MC3000 MC3100 0.8 8 0.7 8 MC5400 1.0 10 MC7400 1.0 10 MC930 MC830 1.0* 10 1.15 12

INPUT AND OUTPUT LOADING FACTORS with respect to MTTL and MDTL families

Applies only when input is being driven by MDTL gate with 2.0 kilohm pullup resistor. Logic ''1'' state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.



SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS





APPLICATIONS INFORMATION

A parity generation tree (simple parity) for a 20-bit word is shown in Figure 5. It uses two MC4308/4008 8-bit parity trees and one MC4310/4010 dual 4-bit parity tree. If a parity word containing odd parity is required (i.e., the 20-bit word plus the parity bit are to contain an odd number of "1's"), the direct output from the parity tree (output A) is used as the parity bit. If even parity is required, the extra Exclusive-NOR gate in one MC4308/4008 provides the inversion when connected as indicated for output B.



A parity detection circuit for a 20bit word is shown in Figure 6. The 20-bit word is connected to a two-stage parity tree identical to that used for the 20-bit parity generator; however, for the detection circuit the output of the tree must be compared with the input parity bit. The parity bit serves as an input to the second stage of the tree. For odd parity detection, output A will be a logic "1" if no error has occurred. For even parity detection, a logic "1" will appear at output B if no error has been introduced. Longer word lengths can be examined in a similar manner.