

The MC4042 and MC4043 are designed for magnetic memory driver/selector applications.

The MC4042 monolithic quad predriver consists of four highspeed switching transistors, each driven by an MTTL compatible NOR gate. Each NOR gate has an individual address input and a common timing input. The inputs of the MC4042 can be driven directly with standard MTTL decoders such as the MC4006 binary to one-of-eight decoder or the MC4007 dual binary to one-of-four decoder. The open-collector output transistor of the MC4042 will sink 50 mA.

The MC4043 monolithic dual line selector consists of two highspeed 400 mA switches driven by MTTL compatible NOR gates. Each NOR gate has an individual address input and a common timing input. The address and timing inputs of the MC4043 can also be driven directly with standard MTTL decoders such as the MC4006 and MC4007.

The MC4042 and MC4043 input circuits are the same, but the output circuitry is different as shown in the device schematics. The output transistors of both devices have a minimum  $BV_{CEX}$  of 15 volts, and are gold doped to increase switching speeds.

Many memory predriver applications employ transformer coupling between the predriver and driver stages. In such designs, large voltage overshoots occur due to the transformer inductance and high-speed switching currents. The collector of the MC4042 is internally clamped to prevent the collector from exceeding the maximum rated voltage during the switching transitions. The voltage applied to the diode clamp, pin 5, should be the same or greater than the collector voltages at pins 1, 7, 8, and 14, to prevent the diode clamp from being forward biased during nonswitching periods. The output transistor is driven with a conventional totem pole arrangement to provide active pullup and pulldown.

MC4300/MC4000 series

The collectors of the pullup transistors of the MC4043 are available at pins 1 and 7. An external load resistor to  $V_{CC}$  must be provided. This reduces power dissipation of the package and provides a means by which the speed of the device can be varied by changing the value of the pullup resistance.

The internal decoding circuitry of the MC4043 is such that both switches can be turned on at one time. However, due to power limitations, care must be taken to ensure that only one switch is turned on at any one time.

The MC4042 and MC4043 can provide a memory system with an inexpensive, reliable, fast drive system. They are also useful as relay or lamp drivers, high fan-out gates, and MOS drivers.



### 2,3,6,9,10,11,13 3,10 3,5,10 3,10 Gnd 3,10 3,103,103,10 3,10 3,10 3,10 3,10 3,10 ( V<sub>cc 2</sub> ) V<sub>cc2</sub> 12 12 12 1.1 . . . . . , ŝ 1.1 . . ī ß V<sub>CCH</sub> V CCH 5.25 5.25 5.25 . ï 4 4 4 4 5.4 ÷ ī • 4 . ł V<sub>cct</sub> 4.75 4.75 4.75 د در , ł 1.1 . . . . 4 4 44 4 ı ī 5.0 5.0 20 5.0 د د . . . 1.1 ï 4 1.1 . . . 4 4 4 FEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW V max 7.0 , . . . í. . 4 . . 1.1 1.1 . . . 1 Volts 1 Vout V out TEST CURRENT/VOLTAGE VALUES 15 15 ï 15 i 1 . . - -, , . . • • ï 11 2,6,9,13 2.5 2.5 2,11 2.5 >" = ~ ī > 1 • . . . . . 1.0 1.7 0.4 > 0.4 1.0 1.4 0.4 >" 2 [] . . . . 101 10 . ı . ı ı. 2.0 > ># . i 1 1.5 1.1 • • ~ = ī • , ï 1.0 > > ī . . . . 1.1 0.1 ÷ ł ī 11 ÷ \_0 , 10 , ٩ -Pulse Out • • , 6.4 1 1 1 1 --4 l. 4 | 4.0 4,0 4.0 , Pulse In 1.1 1.1 1 1.1 ÷ i 1 Ā Ξ : മ 1.0 1,0 1.0 \_<u>.</u>£ \_. 1 ÷ i • , 2 ٠ , . Pulse In ~ ◄ ~ ŏ 50 20 20 \_d , 1 1 ----ł . , 1 +25°C +75°C **Femperature** °° mAdc μ Adc μ Adc µAdc µAdc mAdic mAdc mAde Ę @ Test ns Vdc Vdc Vdc Vdc ns -1.6 -6.4 Min Max 0.5 160 160 250 250 42 . . 1.1 , . +75°C MC4042 Test Limits 5.5 1.1 1.1 1.1 a i ï . • i ï . -1.6 -6.4 Min Max 0.5 40 160 250 1.5 52 +25°C 36 42 25 1.1 5.5 1.1 1.1 . 1.1 . . ı. ï . , . Max -1.6 0.0 250 250 40 160 1.1 42 . . . . So Min 5.5 E. 1.1 . 1.1 . . , ÷ ï . ï Pin Under Test 11,1 11,1 -4 4 4 2 1 ~ 1 - -- -1 2 Symbol BV <sup>1</sup>PDL PDH\_ I max <sup>1</sup>CEX vol 2 +pd+ tpd-H IR I Output Leakage Current Turn-On Delay Time Switching Parameters Power Supply Drain Power Requirements Breakdown Voltage Characteristic Forward Current Maximum Power Supply Current Leakage Current Turn-Off Delay **Output Voltage** Clamp Voltage Output but

## MC4042F, L, P, MC4043F, L, P (continued)

ELECTRICAL CHARACTERISTICS - MC4042

Test procedures are shown for the timing input, one address input, and one output. Test other inputs and outputs in the same manner.

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Test procedures are shown for the timing input, one address input, and one output. Test other inputs and outputs in the same mannet.

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								- (0)	1		mA						>	olts						
							•	Temper	ature	lor	s	2 l <sub>in</sub>	V <sub>IL</sub>	<ul><li>H</li></ul>	۷F	< R	Vout	V <sub>CEX</sub>	Vmax	Vcc	VccL	V <sub>cch</sub>		
									0°C	400*	1.0	2.0	1.1	2.0	0.4	2.5	5.5	15		5.0	4.75	5.25		
								+	-25°C	400*	1.0	2.0	1.1	1.8	0.4	2.5	5.5	15	7.0	5.0	4.75	5.25		
		1	1.4			1		+	-75°C	400*	1.0	2.0	0.9	1.8	0.4	2.5	5.5	15	,	5.0	4.75	5.25		
		Dia		N	AC404	3 Test	Limits				4	FEST CUR	RENT/VC	I TAG	F APP	I IFD T(	SNIG (	ISTED	BFLOW					
		Under	0	°°	+2	2°C	+75	D°C												F				
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	ы_	s	2 In	<"	×	>"	< 	Vout	VCEX	Vmax	< CC	VccL	Vcch	*	Gnd
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Leakage Current	IR	2 5	1.1	40 80	1.1	40 80	1.1	40 80	µAdc µAdc	1.1	1.1	) f	1.1	1.1	1.1	2 10	i r				1, 1	4 4		3,5,6,10 2,3,6,10
Breakdown Voltage	BVin	2 5	5.5	1.1	5.5	1.1	5.5	1 1	Vdc Vdc	1.1	- 2	נע ו	1.1	1.1		1.1					і. 1 т	4 4		3,10 3,10
Output Output Voltage	v <sub>oL</sub> *	14 14	11	0.5	i ana	0.5	1.1	0.5	Vdc Vdc	14 14			5.5	1 - i - i	01 10	- 7 a a	· · · · · ·				ন্দ ক	1.1		3,10 3,10
Output Leakage Current	<sup>I</sup> CEX 1	14 14	1.1	2.0	u ai	2.0	ar i	2.0	mAdc mAdc	1.1	i i	1 - 1-	1.1	5 22			- 1 - 1	14 14			44		1.1	3,10 3,10
	<sup>I</sup> CEX 2	1	1 1	500 500	ar d	500	1.1	500 500	μ Adc μ Adc	1.1	1.1		2 5	2 5	1.1.	.1.5		<u>т</u> .		1 1		4 4		3,10 3,10
Power Requirements Maximum Power Supply Current	Imax	4			i en en	<b>3</b> 5	- 		mAdc			1		. ()	1	1		1	4	14 M		1		3,10
Power Supply Drain	IPD	44		12 12	1.1	12 12	1.1	12 12	mAdc mAdc	1.1	1 L.		6 2	1.1	າຍ	1 C	1. í.	1.1	-1 <sup>-</sup> 1	44	i. i			3,10 3,10
Switching Parameters				inger. Austri						Pulse In A	Pulse B	-	out		1.00									
Turn-On Delay Time	t <sub>pd-</sub>	5,14	l.	1.5	3	35	1	i.	ns	5	2 2		1:	1	1.1	1		,	1	4	١.	1		3,10
Turn-Off Delay Time	t <sub>pd+</sub>	5,14	$\langle \hat{k} \rangle$	1	1	26	1	i.	su	2	5		1:	,	÷.,		1.1		1	4	1		1	3,10

MC4042F,L,P, MC4043F,L,P (continued)

\*Pulsed, 40% duty cycle @ 1.0 MHz. \*\*Connect pins to  $V_{\rm CC}$  through a 75-ohm resistor.



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

MC4042 TYPICAL SWITCHING TIMES

tpd+, TURN-OFF DELAY TIME (ns)







16 (su) TURN-OFF DELAY TIME 15  $V_{CC} = 5.0 V dc$ 14 13 30 mA out 12 lout = 50 mA 11 10 tpd+, 9.0 25 50 75 0 T<sub>A</sub>, AMBIENT TEMPERATURE (<sup>o</sup>C)

### FIGURE 4 - TURN-OFF DELAY TIME versus POWER SUPPLY VOLTAGE



FIGURE 2 - TURN-OFF DELAY TIME versus TE



TA, AMBIENT TEMPERATURE (°C)

MC4043 TYPICAL SWITCHING TIMES

t<sub>pd</sub>, PROPAGATION DELAY TIME (ns)

# MC4042F, L, P, MC4043F, L, P (continued)



Figure 11 illustrates a typical core memory driver/selector using MC4042 and MC4043 devices. The source circuit for the X or Y drive line consists of an MC4042 predriver transformer coupled to a fast high-current transistor. The sink circuit is the MC4043 line selector. The source and sink circuits are used in pairs and are arranged to permit bipolar currents to pass through a selected drive line. Supply voltage and resistor values are determined by system requirements.



### FIGURE 11 - X or Y DRIVE SELECTION MATRIX