QUAD PREDRIVER

MC4042F, L, P*

DUAL LINE SELECTOR

MC4043F, L, P*

The MC4042 and MC4043 are designed for magnetic memory driver/selector applications.

The MC4042 monolithic quad predriver consists of four highspeed switching transistors, each driven by an MTTL compatible NOR gate. Each NOR gate has an individual address input and a common timing input. The inputs of the MC4042 can be driven directly with standard MTTL decoders such as the MC4006 binary to one-of-eight decoder or the MC4007 dual binary to one-of-four decoder. The open-collector output transistor of the MC4042 will sink 50 mA.

The MC4043 monolithic dual line selector consists of two highspeed 400 mA switches driven by MTTL compatible NOR gates. Each NOR gate has an individual address input and a common timing input. The address and timing inputs of the MC4043 can also be driven directly with standard MTTL decoders such as the MC4006 and MC4007.

The MC4042 and MC4043 input circuits are the same, but the output circuitry is different as shown in the device schematics. The output transistors of both devices have a minimum $BV_{\mbox{\footnotesize{CEX}}}$ of 15 volts, and are gold doped to increase switching speeds.

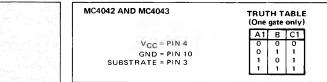
Many memory predriver applications employ transformer coupling between the predriver and driver stages. In such designs, large

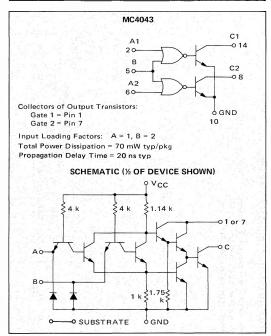
voltage overshoots occur due to the transformer inductance and high-speed switching currents. The collector of the MC4042 is internally clamped to prevent the collector from exceeding the maximum rated voltage during the switching transitions. The voltage applied to the diode clamp, pin 5, should be the same or greater than the collector voltages at pins 1, 7, 8, and 14, to prevent the diode clamp from being forward biased during nonswitching periods. The output transistor is driven with a conventional totem pole arrangement to provide active pullup and pulldown.

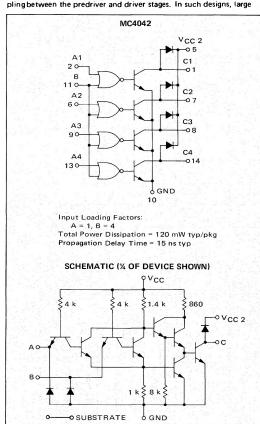
The collectors of the pullup transistors of the MC4043 are available at pins 1 and 7. An external load resistor to V_{CC} must be provided. This reduces power dissipation of the package and provides a means by which the speed of the device can be varied by changing the value of the pullup resistance.

The internal decoding circuitry of the MC4043 is such that both switches can be turned on at one time. However, due to power limitations, care must be taken to ensure that only one switch is turned on at any one time.

The MC4042 and MC4043 can provide a memory system with an inexpensive, reliable, fast drive system. They are also useful as relay or lamp drivers, high fan-out gates, and MOS drivers.







*F suffix = TO-86 ceramic flat package (Case 607).

L suffix = TO:116 ceramic dual in-line package (Case 632).

P suffix = TO-116 plastic dual in-line package (Case 605).

MC4042F,L,P, MC4043F,L,P (continued)

ELECTRICAL CHARACTERISTICS - MC4042

Test procedures are shown for the timing input, one address input, and one output. Test other inputs and outputs in the same manner.

									L					TEST	GR	ENT/V	TEST CURRENT/VOLTAGE VALUES	ALUES						
								@ 100	 ;		шA						×	Voits	ŧ.					
							_	Temperature	ature	_6	-ie	4 In	٩	V _R	>	>	>	> o	ر سوم م	νςς	ر در	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V _{CC 2}	
									٥٥	20	1.0	4.0		1.0	2.0	4.0	2.5	15		5.0	4.75	5.25	12	
								+	+25°C	50	1.0	4.0	10	1.0	1.7	0.4	2.5	15	7.0	5.0	4.75	5.25	12	•
				4				+	+75°C	20	1.0	4.0		1.0	1.4	4.0	2.5	15		5.0	4.75	5.25	12	
		Pi.		2	C404;	2 Test	1C4042 Test Limits					=	ST CLIRE	ENT	OITAG	F APP	TEST CHREENT/VOLTAGE APPLIED TO PING LISTED RELOW.		1	S				
		Under	٥°C	ې	+25°C	v	+75°C	٠		-														•
Characteristic	Symbol	Test	Mi.	Max	Min Max		Min	Max	Gnit		_e	4 I.	_0	>"	>	>"	>"	٧	/ mex	>	ស >	\ \ \ \ \ \	V _{CC2}	9ug
Input		c	76	-	$\overline{}$	-	-	9	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	11	1.	ł,			1		:	À	- 1	19	4			Ç
rorward current	H	7 =	Fil	-6.4		-6.4			mAdc	, ,	, ,		i.a			7 =	2,6,9,13	,		6.1	, i	7 7		3,10
Leakage Current	$^{\rm I}_{\rm R}$	2	3.1	40 160	5.6	40	1.1	40 160	μAdc μAdc			49	3.3		23	1.1	2 11	i i			٠.	ক ক	1.1	3,10 3,10
Breakdown Voltage	BVin	2 11	5.5	1.7	5.5	r r	5.5	11	Vdc	1.1	2 -	- 1	43	4.1	1.1	, ,	- 1	4.1	1.1	1.5	ાર્લ	44	1 1	3,10 3,10
Output								-																
Output Voltage	N _{OL}		3.1	0.5	11	0.5		0.5	Vdc			i i	1 1	2 11		11 2					কক	5.4		3,10 3,10
Output Leakage Current	CEX		1 1	250 250		250 250	7 1	250 µ	μAdc μAdc		1.4		1.1	0.0	2 []	11 2			1.1	0.0	44			3,10 3,10
Clamp Voltage	v _D	-				1.5		-	Vdc				-				2,11			١.	4	٠	·	3,5,10
Power Requirements								-	-															
Maximum Power Supply Current	Imax	4				36		-	m Adc	1		,	1	-	•		•	ı	4		•	•	1	3,10
Power Supply Drain	IPDL	4		42		42	- 10	42 n	n) Adc	-	-	,	-	,	,	,		•	,	4	'			2,3,6,9,10,11,13
	PDH	4	-	23		23	-	23 n	mAdc	-	-	-	-		-			٠		4		٠		3,10
Switching Parameters	2 /			1						Pulse In A	Pulse B	_	Pulse Out											
Turn-On Delay Time	t pd-	11,1				25	,	•	su	8	11		-	1		1		ı		4	1	•	2	3,10
Turn-Off Delay	t pd+	11,1	1			25			su	2	11		1	,						4	1		2	3,10

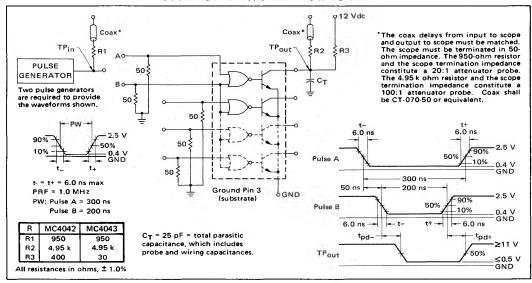
MC4042F,L,P, MC4043F,L,P (continued)

ELECTRICAL CHARACTERISTICS - MC4043 Test procedures are shown for the timing input, one address input, and one output. Test other inputs and outputs in the same manner.

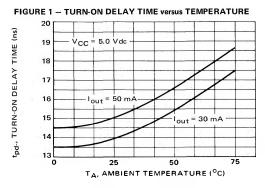
									_				F	EST CL	JRREN	1/00	TEST CURRENT/VOLTAGE VALUES	ALUES						
								(-		mA							Volts						
								© lest Temperature	ature	101	e	2 lin	V _{II}	>	>"	>~	Vout	V _{CEX}	V	20	VccL	СССН	,	
									္ ၁	*00+	1.0	2.0	1.1	2.0	0.4	2.5	5.5	15	-	5.0	4.75	5.25		
								+	+25°C	400*	1.0	2.0	1.1	1.8	0.4	2.5	5.5	15	7.0	5.0	4.75	5.25		
								+	+75°C	400*	1.0	2.0	6.0	1.8	0.4	2.5	5.5	15	,	5.0	4.75	5.25		
		Pin		V	MC4043 Test Limits	Test	Limits					TEST CUI	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW	VOLTA	GE AP	TIED .	O PIN	SLISTEL	BELOW					
		Under		J ₀ 0	+25°C	ွ	+75°C	ې																
Characteristic	Symbol	Test		Min Max	Min Max		Min	Max	Unit	 ō		2 I.	>=	>=	>_	>"	> ont	VCEX	Vmax	ک ک	700	V _{CCH}	*	Gnd
Input Forward Current	$I_{ m F}$	5 2	. 64	-1.6	1.1.1.	-1.6		-1.6	mAdc mAdc	11	1.1	11	- 1	ri	21.02	5,6	1.1	1.1	111	111		44	1.1	3,10 3,10
Leakage Current	IR	21 12	11	40	1 1	40	1 1	80	μAdc μAdc	1.1	1 1)- ,r	1 1	1.1	1. 1.	2 5	rr	1 1	1 1	1.1	1, 1	4 4		3,5,6,10 2,3,6,10
Breakdown Voltage	BVin	5 2	5.5	1. 1	5.5	1 1	5.5	1 1	Vdc	LI	2 -	. دی ا	T I	1-1	1.1	1.1		1 1	1.1	1.1	1 1	44	1 1	3,10 3,10
Output Output Voltage	vol.*	14 14	1.1	0.5	1.1	0.5	1.1	0.5	Vdc	14 14			2.2	1.1	27.10	- 7 j. j.	1.1		1 1	1.1	44	1.1	нн	3,10 3,10
Output Leakage Current	ICEX 1	14 14	1 1	2.0	11.1	2.0	11.1	2.0 I	mAdc mAdc	1 1	I · I	1 - 1 -	1.1	2	1 (,1 1,	. 1	14 14	1.1	1 1	44	1 1	1 1	3,10 3,10
	ICEX 2		1 1	500	1 1	500	1.1	500	μ Adc μ Adc	1 1	1 1	1 1	22	2	1 1	ri	11	1 1	1.1	1 1	1 1	4 4		3,10 3,10
Power Requirements Maximum Power Supply Current	Imax	4			1	35			mAdc		1	1	1 d 1	. 12	1		- 1 in 1	t	4	ř	-	t		3,10
Power Supply Drain	СГ	4 4	j	12	1.1	12	1 1	12 1	mAdc mAdc	1.1	i L	1.1	6 2	1.1	ດເວ	1.0	1 1	111	-1 1	44	1. 1			3,10
Switching Parameters		13				3				Pulse In A	Pulse In B		Pulse Out											
Turn-On Delay Time	tpd-	5,14	100		ì	35	1	i.	ns	3	2		1.5	1		1		,	-	4	1.	-	1	3,10
Turn-Off Delay Time	tpd+	5,14	ji.	1		26	1	î.	Su	2	2		14	,			1.5	1	1	4	-	1	1	3,10

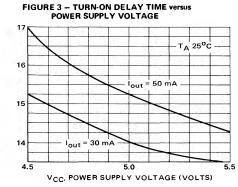
*Pulsed, 40% duty cycle @ 1.0 MHz. **Connect pins to $V_{\rm CC}$ through a 75-ohm resistor.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

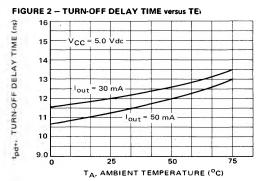


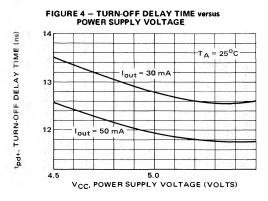
MC4042 TYPICAL SWITCHING TIMES





tpd-, TURN-ON DELAY TIME (ns)





15

50

100 150

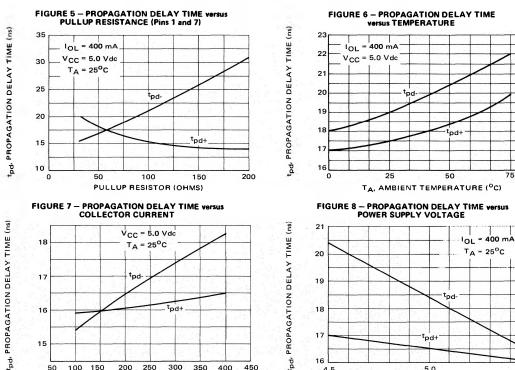
200 250

IC, COLLECTOR CURRENT (MA)

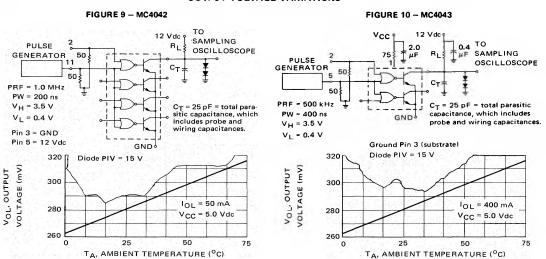
300

350 400 450

MC4043 TYPICAL SWITCHING TIMES



OUTPUT VOLTAGE VARIATIONS



17

16

4.5

,pd

t_{pd}-

5.0

VCC, POWER SUPPLY VOLTAGE (VOLTS)

TYPICAL APPLICATION

Figure 11 illustrates a typical core memory driver/selector using MC4042 and MC4043 devices. The source circuit for the X or Y drive line consists of an MC4042 predriver transformer coupled to a fast high-current transistor. The sink circuit is the MC4043 line selector. The source and sink circuits are used in pairs and are arranged to permit bipolar currents to pass through a selected drive line. Supply voltage and resistor values are determined by system requirements.

FIGURE 11 - X or Y DRIVE SELECTION MATRIX

