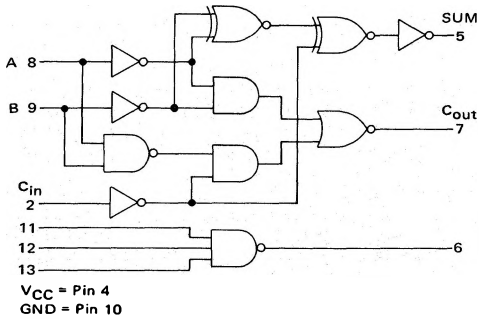


FULL ADDERS

MC4300/MC4000 series

MC4326F,L • MC4327F,L*
MC4026F,L,P • MC4027F,L,P*



Input Loading Factor:

A, B = 2
 C_{in}, Pins 11, 12, 13 = 1

Output Loading Factor:

MC4326 = 15 MTTL I Loads
 MC4327 = 7 MTTL I Loads
 MC4026 = 12 MTTL I Loads
 MC4027 = 6 MTTL I Loads

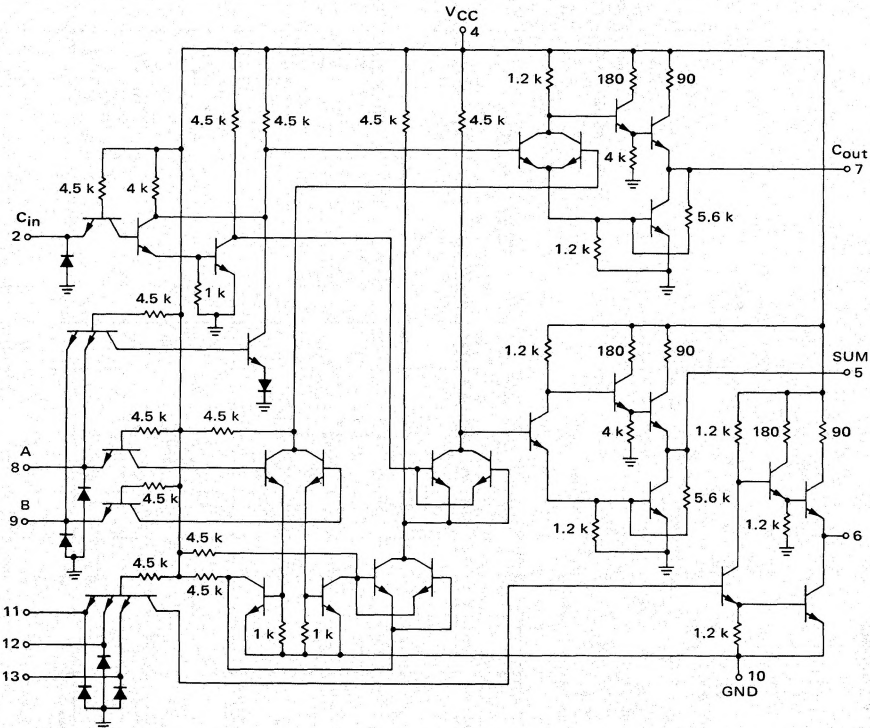
These full adders are designed for serial and ripple-carry parallel adder systems. True Sum and Carry are produced at the output from the input information. A separate 3-input NAND gate is provided on the monolithic chip to provide the inverted Sum or Carry output.

TRUTH TABLE

Input Pins			Output Pins	
8	9	2	5	7
A	B	C _{in}	SUM	C _{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Total Power Dissipation = 90 mW typ/pkg
 Add Delay = 25 ns typ
 Carry Delay = 13 ns typ

CIRCUIT SCHEMATIC



*F suffix = TO-86 ceramic flat package (Case 607).

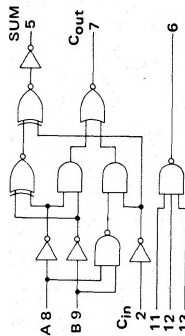
L suffix = TO-116 ceramic dual in-line package (Case 632).

P suffix = TO-116 plastic dual in-line package (Case 605).

MC4326F,L, MC4327F,L, MC4026F,L,P, MC4027F,L,P (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for inputs A and C_{in}. Other inputs are tested in the same manner. Output tests should be completed according to the truth table.



Characteristic		Pin Under Test		MC4326, MC4327 Test Limits										TEST CURRENT/VOLTAGE VALUES																		
				MC4326, MC4327 Test Limits										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																		
				-55°C		+25°C		+125°C		0°C		+25°C		+75°C		mA					Volts											
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	I _{OL}	Pr ⁺	Std	I _{in}	2I _{in}	V _{IL}	V _{IH}	V _{th1}	V _{th0}	V _{out}	V _{max}	V _{CC}					
Input	Forward Current	I _F	2	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAAdc	-	-	-	-	-	-	-	-	-	-	4	2.10				
		I _R	8	-	-2.66	-	-2.66	-	-2.66	-	-3.32	-	-3.32	-	-3.32	mAAdc	-	-	-	-	-	-	-	-	-	-	-	4	8.10			
	Leakage Current	I _L	8	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAAdc	-	-	-	-	-	-	-	-	-	-	-	-	4	8.9,10,11,12,13		
		I _L	2	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAAdc	-	-	-	-	-	-	-	-	-	-	-	-	4	2.5,10,11,12,13		
Breakdown Voltage	BV _{in}	2	-	-	5.5	-	-	-	-	-	-	-	-	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	4	10		
		2	-	-	-	-	-	-	-	-	-	-	-	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	4	8.9,10,11,12,13		
		2	-	-	-	-	-	-	-	-	-	-	-	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	4	10		
		8	-	-	-	-	-	-	-	-	-	-	-	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	4	2.5,10,11,12,13		
Output	Output Voltage	V _{out} "yy"	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	-	4	10	
		V _{out} "11"	5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	2.5	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	-	4	10	
	Leakage Current	I _{OLK}	5	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	4	10
		I _{SC}	5	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	4	5,10
Power Requirements (Total Device)	Output Voltage	V _{OL}	5	-	0.4	-	0.4	-	0.45	-	0.4	-	0.4	-	0.45	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	4	10
		V _{OH}	5	2.8	-	3.1	-	3.15	-	3.0	-	3.1	-	3.15	-	3.15	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	-	4	10
	Power Supply Drain	I _{max}	4	-	-	-	-	-	-	-	-	-	-	-	-	mAAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2.8,9,10,11,12,13	-
		I _{PDH}	4	-	27	-	27	-	27	-	35	-	35	-	35	mAAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	10
Power Supply Drain	I _{PDL}	4	-	32	-	32	-	32	-	41	-	41	-	41	mAAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2.8,9,10,11,12,13
		4	-	32	-	32	-	32	-	41	-	41	-	41	mAAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2.8,9,10,11,12,13	

A 8

B 9

C_{in} 2

11

12

13

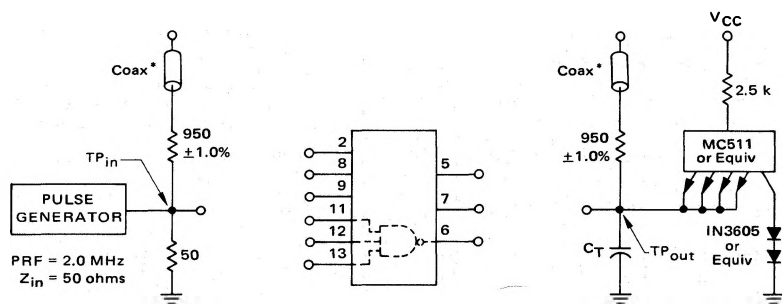
6

7

C_{out}

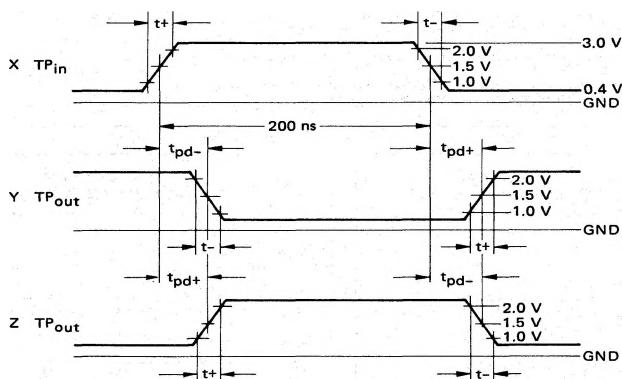
MC4326F,L, MC4327F,L, MC4026F,L,P, MC4027F,L,P (continued)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



$C_T = 15 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

* The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

[illegible]