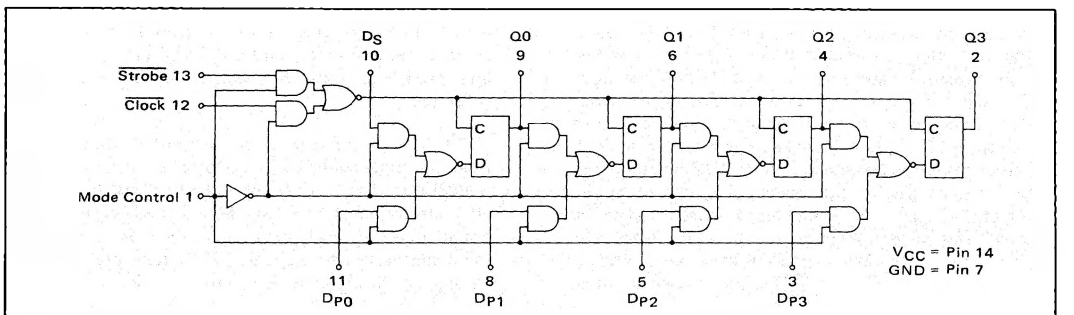
4-BIT SHIFT REGISTER

MC4012L, P*

This 4-bit register provides parallel or serial data entry and retrieval, determined by the logic state of the mode control input. For parallel operation, set the mode control to the logic "1" state and strobe the information at the Dp inputs into the register. Serial left-shift operation is achieved in this mode by connecting the Q outputs to the Dp inputs of the previous stage. For serial right-shift operation, set the mode control to logic "0" and clock data into the register from D_S.



Input Loading Factor:
Mode Control = 5
Other Inputs = 1

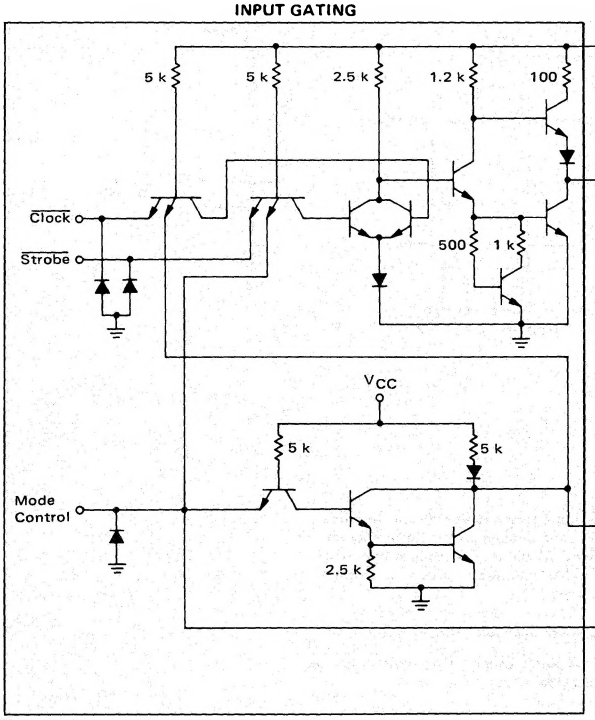
Output Loading Factor = 10

Total Power Dissipation = 180 mW typ/pkg

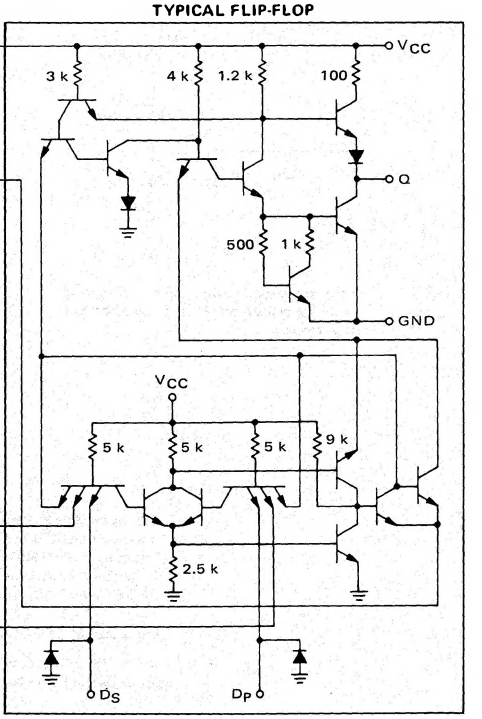
Propagation Delay Time = 25 ns typ/bit
t_{setup} "0" (Mode Control) = 25 ns typ
t_{setup} "1" (Mode Control) = 12 ns typ
t_{setup} "0" (D_{P0}, D_S) = 4.0 ns typ
t_{setup} "1" (D_{P0}, D_S) = 3.0 ns typ

t_{hold} "0" (Mode Control) 5.0 ns typ
t_{hold} "1" (Mode Control) 9.0 ns typ
t_{hold} "0" (D_{P0}, D_S) = 7.0 ns typ
t_{hold} "1" (D_{P0}, D_S) = 11 ns typ
f_{Tog} = 35 MHz typ @ 25°C

INPUT GATING



TYPICAL FLIP-FLOP



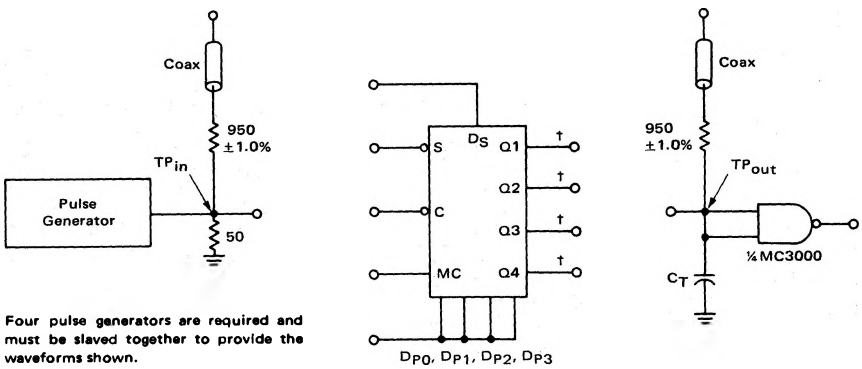
*L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

OPERATING CHARACTERISTICS

This shift register can be operated in the serial or parallel mode by properly setting the mode control. Data present on the four parallel inputs, D_{P0} through D_{P3}, can be strobed into the register by applying a logic "1" level to the mode control input and applying a positive pulse to the strobe input. The mode control must be in the logic "1" state a minimum of 30 ns prior to the strobe pulse. Operation in the serial mode can be achieved by setting the mode control input to a logic "0" state and applying a positive pulse to the clock input. The mode control must be set to the logic "0" state at least 20 ns prior to the clock pulse. The clock must be in the low state when the mode control is changed from the "0" to the "1" state. The strobe must be in the low state when the mode control is changed from the "1" to the "0" state. Information present on the data inputs between the setup and hold times will be transferred into the register during the negative transition of the clock or strobe.

To operate the register in the serial shift-right mode when the mode control is in the logic "0" state, serial data is applied to D_{P0}, and the clock input is toggled. To operate in the serial shift-left mode, externally connect each output to the parallel data input of the previous stage, set the mode control to the logic "1" state, apply serial data to D_{P3}, and clock the strobe input.

SWITCHING TIME TEST CIRCUIT



Four pulse generators are required and must be slaved together to provide the waveforms shown.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

†Load should be connected to each output during test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

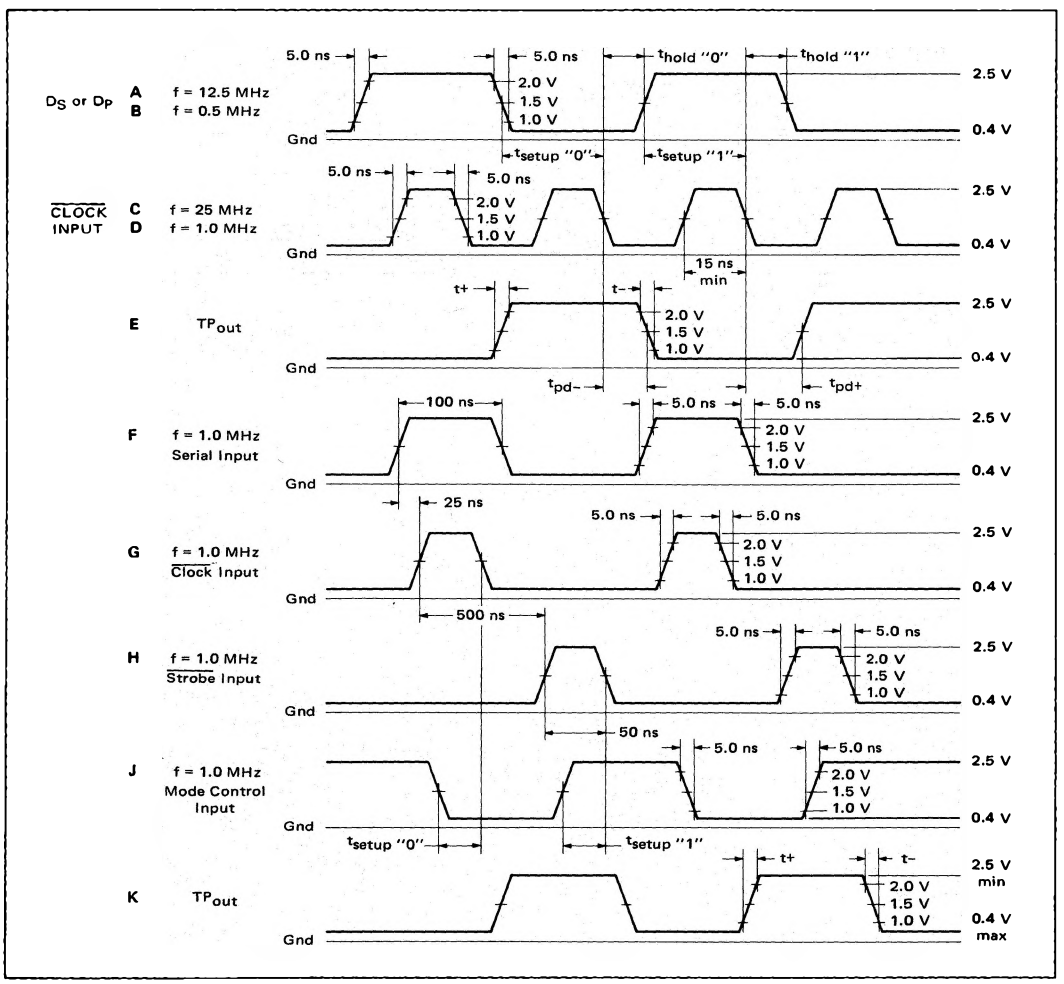
INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family

**Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.

VOLTAGE WAVEFORMS AND DEFINITIONS



DC ELECTRICAL CHARACTERISTICS
(T_A = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input			
Forward Current — MC	I_{F1}	-8.0 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 5.25 Vdc
Others		-1.6 mAdc max	
MC	I_{F2}	-7.0 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 4.75 Vdc
Others		-1.4 mAdc max	
Leakage Current — MC	I_R	200 μAdc max	V_{in} = 2.5 Vdc, V_{CC} = 5.25 Vdc
Others		40 μAdc max	
Breakdown Voltage	BV_{in}	5.5 Vdc max	I_{in} = 1.0 mAdc, V_{CC} = 5.25 Vdc, T_A = 25°C
Clamp Voltage	V_D	-1.5 Vdc max	I_D = -10 mAdc, V_{CC} = 4.75 Vdc, T_A = 25°C
Threshold Voltage	V_{th} "1"	2.0 Vdc	T_A = 0°C
		1.8 Vdc	T_A = +25°C, or T_A = +75°C
	V_{th} "0"	1.1 Vdc	T_A = 0°C, or T_A = +25°C
		0.9 Vdc	T_A = +75°C
Output			
Output Voltage	V_{OL}	0.4 Vdc max	I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
		0.4 Vdc max	I_{OL} = 17.6 mAdc, V_{CC} = 5.25 Vdc
	V_{OH}	2.5 Vdc min	I_{OH} = -1.6 mAdc, V_{CC} = 4.75 Vdc
Short-Circuit Current	I_{SC}	-20 to -65 mAdc	V_{out} = 0 Vdc, V_{CC} = 5.0 Vdc