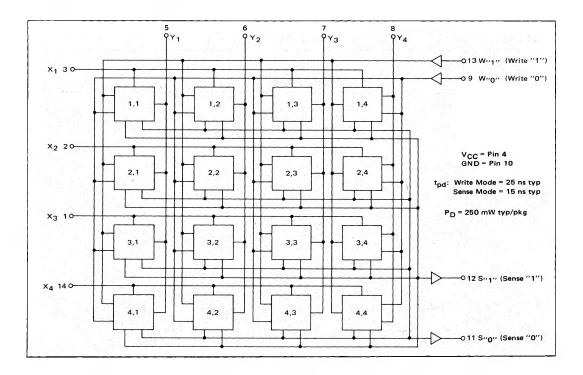
16-BIT SCRATCH PAD MEMORY CELL

MC4304F, L • MC4305F, L* MC4004F, L, P • MC4005F, L, P*

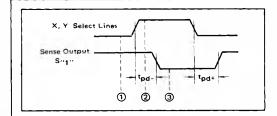
This 16-Bit memory cell serves as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

The memory contains 16 flip-flops arranged in a fourby-four matrix. A single bit of the matrix is selected by driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many devices can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two write amplifiers allow a "1" or a "0" to be written into a selected bit.



- OPERATING SEQUENCE -





- (1) All X and Y selection lines and both write inputs are low (less than +0.8 V).
- 2 Desired bit selected by driving the appropriate X and Y select lines more positive than +2.1 V.
- 3 After the turn-on delay time(tpd_), the S"1" output will be low (less than +0.45 V) and the S"0" output will be high (more than +2.5 V), providing that a "1" is stored in the selected bit.

*F suffix = TO-86 ceramic flat package (Case 607). L suffix = TO-116 ceramic dual in-line package (Case 632).

P suffix = TO-116 plastic dual in-line package (Case 605).

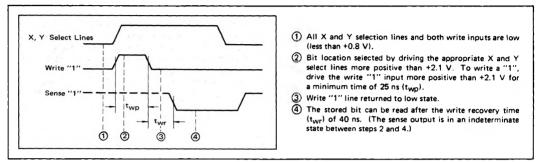
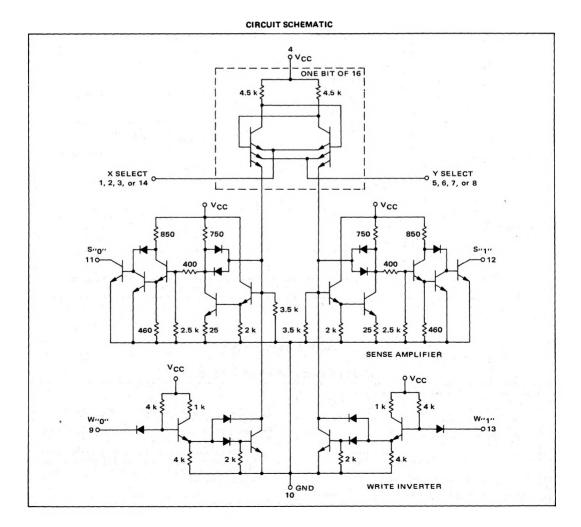


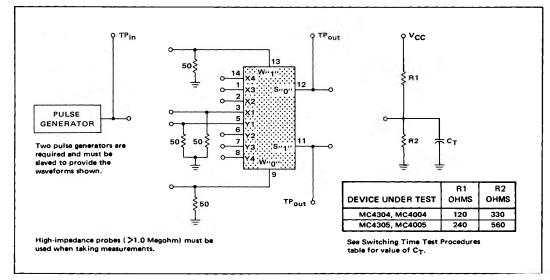
FIGURE 2 - WRITE MODE TIMING DIAGRAM



ted in the same manner. Final transmission of the first transmission of the frame manner. Symbol Test Min Max Min Max Min	MC4304*, MC4304*, MC4304*, MC4004*, MC4004*, MC4004*, MC4004*, MC4004*, MC400	@ E	5	اه"و"	Am						Volts					
A304, MC4305 Test Limits Ast Limits 35C +25°C +175°C 0 Max Min Max Min Max -11 -11 -11 -11 - -11 -11 -11 -11 - -11 -11 -11 - - -11 -11 -11 - - -113 -11.33 -11.33 - - -1.133 -11.33 - - - -1.133 - 0.4 - 0.4 - -1.133 - 0.1 - 0.1 - -1.133 - 0.1 - 0.1 - 0.1 - 0.4 - 0.4 - 0 - 5.5 - 5.5 - 5.5 - 5.5 - 0.45 - 0.45 - 0.45 - 0 0.45 - <th>MC4304', MC 4304', MA 4004', MA (14004', MC4005', MA 28' 21' 21' 21' 21' 21' 21' 21' 21' 21' 21</th> <th>@ E</th> <th>ts</th> <th>-0s</th> <th></th> <th></th> <th></th> <th></th> <th>ł</th> <th></th> <th></th> <th></th> <th></th> <th></th> <th>_</th> <th>_</th>	MC4304', MC 4304', MA 4004', MA (14004', MC4005', MA 28' 21' 21' 21' 21' 21' 21' 21' 21' 21' 21	@ E	ts	-0s					ł						_	_
Fin MC4304, MC4305 Test limits International free limits MC4304, MC4305 Test limits Prime Test Min MAX H125 Yr 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	MC4304', MK MC4304', MK C4004', MK C4004', MC4005', MK AN Min Max M Min Max M Min Max M Min 1 0.4 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.61.68 0.6		ture	Pr* Std	-	~	V	V., J	V	, ,	>	~	7	V.r.	BV	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	MC4304*, MC MC4004*, MC4004*, MC MC4004, MC4005 MI MI MM MM MM MM MM MM MM MM MM MM MM			+	1.0	3.0	0.75	0.85	+	•	4.5	2.2	5.5	+	·	T
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	MC4004, MC4004, MC4004, MC4004, MC4005, MC405, MC5005, MC405, MC5005,	-	L	+	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0	7.0	T
Fin MC(3304, MC(3305, Test timits) It It No Min Min Min Min It 3	Mc4004', Mi (4004', Mi 2004', Mc4005' 2004', Mi 2004', Mi 2005', Mi 200			40 20	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0		-
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	MC4004; MC4005; MC4005; MC4005 (C4004, MC4005 ax Min Max Min Max Min Max Min Max Min 13.5 3.5, 5, 1-13.5 6.6 - 1-13.5 6.6 - 1-1.66 - 1-1.66 - 1-1.66 - 1, 1.	.)	0°C	40 20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0		-
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	(c4004, MC4005 ax Min Max M ax M ax Min Max M Ax Min M Ax Min Max M Ax Min M Ax M Ax Min M Ax Min M Ax Min M		+25°C	40 20	1.0	3.0	0.8	1.0	1,0	0	4.5	2.1	5.5	5.0	7.0	-
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Action Mc4005 A25C A25C A8 Min A8 - 13.5 B6 - 13.5 B6 - 11.08 B6 - 11.08 B1 - 0.4 B1 - 0.1 B - 0.1 B - 5.5	+	+75°C		1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	+25°C Min Max 	lest Limits					FST CHRR	FNT/VOLT	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED RELOW	D TO PINS	LISTED REI	.WO				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Min Max 	J°77+														
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		X	Unit	1so.	M	Ixr	, , ,	V in 2	<	× K	>"	**	Vour	Vcc	BV _{ckt}	Gnd
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$								-								
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		-13.5	mAdc			·	1. j			<i></i>	5,6,7,8	2		4 4	•••	1,2,9,10,13,14
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		-1.66	Adc							0	LTICIOIT	1		4		1 2.3.5.6.7.8.10.13
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	- 0.4 - 0.4 - 0.1 - 0.1 - 0.1 - 0.1 - 0.1 - 0.1 - 0.1	-1.66	mAdc				-	- (i)		13		• •		. 4		1,2,3,5,6,7,8,9,10,14
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	- 0.1 - 0.1 5.5 - 5.5 -	0.4	mAdc			• •	10.		1.1		е и		• •	4.4	• •	1,2,5,6,7,8,9,10,13,14
	- 0.1 5.5 - 5.5 -	0.1	mAde		-		-				6			4		1,2,3,5,6,7,8,10,13,14
Were BY(II) 3 5, 5, 5 5, 5, 5 5, 5, 5 5 5, 5 5 5, 5 5 5, 5 5 5, 5 5 5, 5 5 5, 5 5	5.55 5.55 1.1	0.1	Adc	-				1	1		13		'	4		1,2,3,5,6,7,8,9,10
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	5.5 -		Vdc Vdc	ņ		ო თ	÷н.	·	• •		1			44	• •	1,2,5,6,7,8,9,10,13,14
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	5.5 -	5.5	Vdc		9 13	1.1	• •	- i - i	•••				•••	4.4	• •	1,2,3,5,6,7,8,10,13,14 1,2,3,5,6,7,8,9,10,14
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$									3							
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		- 1		3	1	'	'		đ	,	,	3 5 13		4		126781014
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	45 - 0.45 -	0.45	Vdc	12	1							3,5	,	+	1	1,2,6,7,8,9,10,13,14
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	· · · · · ·						3,5			13	6			4	Ľ	1,2,6,7,8,10,14
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	- 0.45	- 0.45	Vdc	12	•	•	1,	•	•	1 -		3,5		4	'	1,2,6,7,8,9,10,13,14
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$.н 2	14		-		13	•		3,5,9		4	1	1,2,6,7,8,10,14
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	45 - 0.45 -	0.45	Vdc	11				•				3,5	•	4	'	1,2,6,7,8,9,10,13,14
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	-	•					3,5	••	•	6	13			4		1,2,6,7,8,10,14
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	45 - 0.45 -	0.45	Vdc	11			1.			•	•	3,5	•	4	'	1,2,6,7,8,9,10,13,14
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		-			1.1		-	-	6	1.1		3,5,13	-	4		1,2,6,7,8,10,14
at 100 100 100 100 100 100 100 100 100 10	45 - 0.45 -	0.45	Vdc	12					•	×.	•	3, 5	•	4	•	1,2,6,7,8,9,10,13,14
at <u>10LK</u> 12 - 0.25 - 0.25 - 0.25						1		•	6	•	•	3,5,13	•	4		1,2,6,7,8,10,14
	- 0.25	- 0.25 n	mAdc	•	-	•	•	3,5	•		•	•	12	4	•	1,2,6,7,8,9,10,13,14
		- 1-		,				•	13		•	3,5,9	•	4		1,2,6,7,8,10,14
Leakage Current I _{OLK} 11 - 0.25 - 0.25 - 0.25 - 0.25	- 0.25	- 0.25 n	mAdc	•	•	•		3,5		-			11	4		1,2,6,7,9,10,13,14
Write "1" **			-		-	•	-	•			13	3,5,6,7,8	-	4	-	1,2,9,10,14
Leakage Current IOLK 11 - 0.25 - 0.25 - 0.25 - 0.25	25 - 0.25 -	0.25	mAdc	-	- 1.54	1	•	,	1	1	•	3,5,6,7,8	11	4	-	1,2,9,10,13,14
				-		'				1	6	3,5,6,7,8	•	4	'	1,2,10,13,14
Leakage Current IOLK 12 - 0.25 - 0.25 - 0.25 - 0.25	- 0.25	- 0.25	mAde			•	•	•				3,5,6,7,8		4	'	1,2,9,10,13,14
Power Requirements 1 5 5 5 5 5 5 5 5 7 72 Power Suppy Drain I _{PD} 4 - 65 - 65 - 65 - 72	- 72	- 72	mAdc				•		'		1		'	4	'	1,2,3,5,6,7,8,9,10,13,14
Power Supply Breakdown Ickt 4 95	- 105	-	mAdc	•	•						1-	i.		•	4	1,2,3,5,6,7,8,9,10,13,14

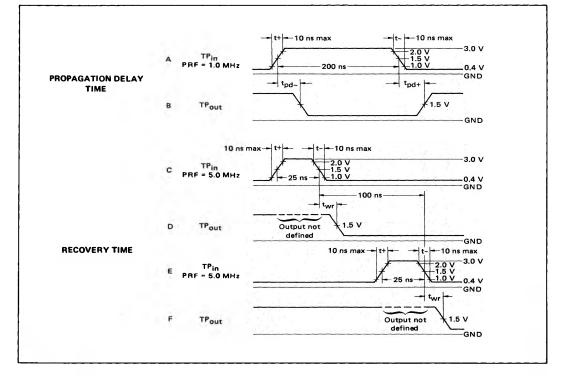
MC4304F,L, MC4305F,L /MC4004F,L,P, MC4005F,L,P (continued)

^{*}Prime Fan-Out Note 1. Output logic "0" voltage and leakage current measurements are made as part of a functional test of a memory. Note 1. Output logic "0" voltage ya a coule asterisk (**) are preconditioning procedures for the subsequent test. All power supply and input voltages must be maintained between tests.



SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



MC4304F,L, MC4305F,L /MC4004F,L,P, MC4005F,L,P (continued)

SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms)

		Pin Under Test	Input Pin										Output			Limits	
Test	Symbol		3 ×1	2 X2	1 X3	14 X4	5 Y1	6 Y ₂	7 Y ₃	8 Y4	9 W"0"	13 W"1"	11 S~0″			MC4304-5 ns max	MC4004-5 ns max
Turn-Off Delay Time		-	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	_	-	-	-	
(Address Lines to	••	- 1	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	-	-	-		_
Sense "0" Output)	tpd+	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	-	30	23	23
	tpd+	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	-	200	35	35
Turn-Off Delay Time		- 1	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	-	-	-	-	_
(Address Lines to	···	-	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	-	-	-	-	-
Sense "1" Output)	tpd+	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	-	В	30	23	23
	tpd+	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	-	в	200	35	35
Turn-On Delay Time (Address Lines to Sense "0" Output)		-	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	-		-	-	-
	••		3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	-	~	-	-	
	tpd-	11	Α	Gnd	Gnd	Gnd	Α	Gnd	Gnd	Gnd	Gnd	Gnd	В	-	30	23	23
	tpd-	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	в	-	200	35	35
Turn-On Delay Time (Address Lines to Sense "1" Output) Turn-Off Delay Time	••	-	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	-	-	-	-	-
	••	- 1	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	-	-	-	-	-
	^t pd-	12	Α	Gnd	Gnd	Gnd	Α	Gnd	Gnd	Gnd	Gnd	Gnd	-	B	30	23	23
	tpd-	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	-	в	200	35	35
			3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	-	-	-	-	-
(4 Bits) (Address Lines	••	-	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	-	-	-	-	-
to Sense "O" Output)	tpd+	11	A	Gnd	Gnd	Gnd	A	Α	A	A	Gnd	Gnd	В	-	30	35	35
Turn-Off Delay Time		-	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	-	-	-	-	-
(4 Bits) (Address Lines		-	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	-	-	-	-	1
to Sense "1" Output)	t _{pd+}	12	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	-	в	30	35	35
Write Recovery Time	1 wr	12	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	c	-	D	30	40	40
		11	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	С	F	-	30	40	40
																ns min	ns min
Write Pulse Width	two	-					Tes	ted du	ring t _v	, tests						25	25

*Capacitance value for load of the Switching Time Test Circuit

• • Preconditioning procedures for subsequent test.