Objective short data sheet

1 General description

The PT2001 is a SMARTMOS programmable gate driver IC for solenoid control in automotive application. The typical application is engine control. A wide range of system configurations is also supported.

The general architecture comprises the combination of a set of programmable microcores, integrated high-side (x5) and low-side (x7) predrivers for discrete logic level MOSFETs, end of injection detection and means for diagnostics and protection against external faults. Both battery voltage and booster voltage level high-side configurations are supported. The chip communicates with the main controller through an SPI bus and a flexible set of direct interface signals.

The main characteristic of this component are:

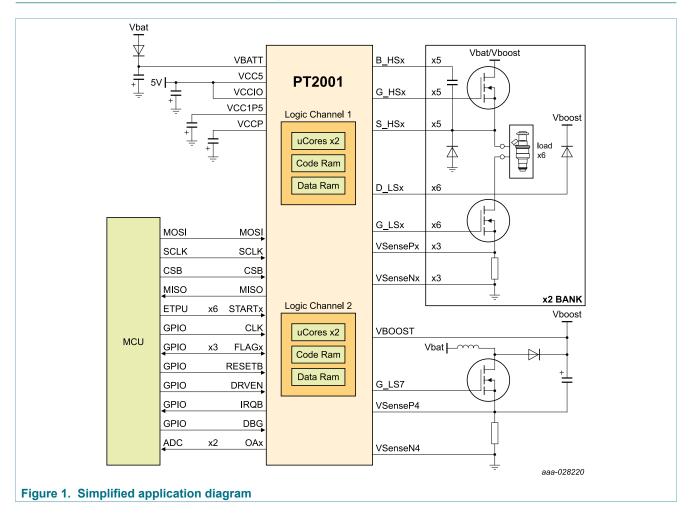
- The programmable architecture: the four dedicated microprocessor cores optimized to control power MOSFETs with small latency time. Thus a high level of flexibility during design and at runtime can be achieved.
- The high level of integration: all interfaces are designed to use as few external components as possible.

2 Features and benefits

- Programmable integrated End-of-Injection (EOI) measurement function
- · Outputs configurable into 2-bank operation
- Five high-side / seven low-side:
 - PWM Frequency: 100 kHz
 - Four programmable slew rates: 12.5 V/μs to 300 V/μs
- Flexible current profile management through four programmable microcores running at 6 MHz
- Automatic free-wheeling control
- Programmable integrated diagnostics:
 - open-load
 - undervoltage
 - overvoltage
 - overcurrent
 - overtemperature
- Independent DRVEN pin for safety
- ISO 26262 compliant development
- · Embedded encryption for microcode protection
- · 16-bit SPI control with IRQB plus three interrupt flags
- 36 V tolerant digital IOs



3 Simplified application diagram



4 Applications

- Automotive (12 V), truck and industrial (24 V) powertrain
- Gasoline Direct Injection (GDI)
- Diesel Direct Injection (DDI)
- · CNG / LNG engines
- Variable Valve Actuators (VVA)
- · Active suspension systems
- · Transmission solenoid drivers (CVT, DCT, AT)

5 Ordering information

This section describes the part numbers available to be purchased along with their differences.

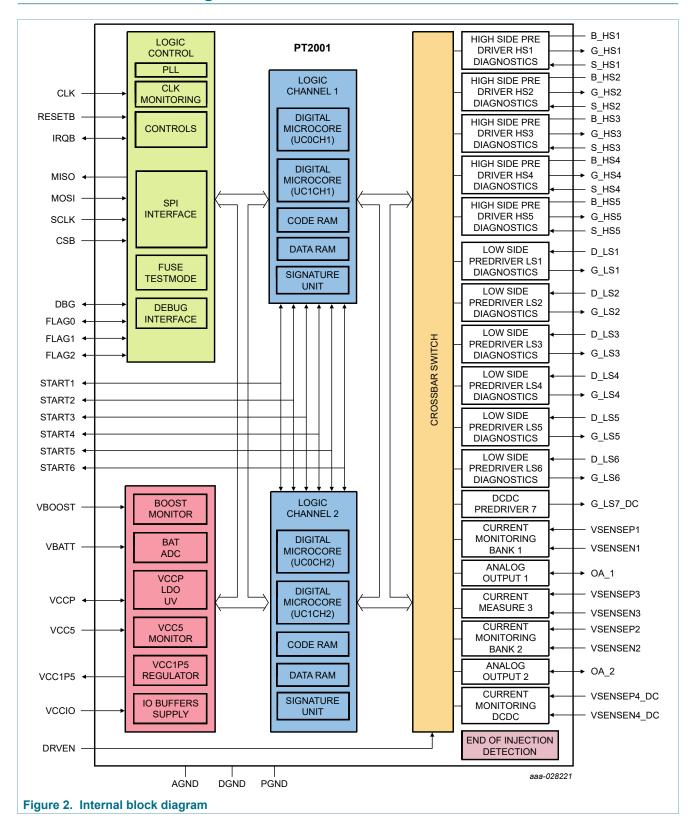
Table 1. Orderable parts

Table II Gradianie parte				
Part number [1]	Temperature (T _A)	Package		
PC33PT2001AE	−40 °C to 125 °C	64-pin LQFP with exposed pad		

^[1] To order parts in tape and reel, add the R2 suffix to the part number.

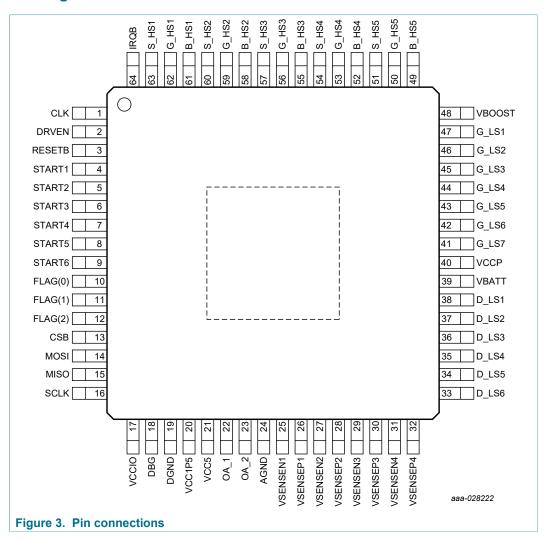
Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search.

6 Internal block diagram



7 Pinning information

7.1 Pinning



7.2 Pin description

Table 2. Pin definitions

Table 2. Fill definitions						
Pin number	Pin name ^{[1][2][3]}	Pin function	Definition	Pull-up/pull-down	Reset	
1	Clk	In	Clock pin (low frequency reference for internal PLL)	Weak PU ^[4]	Input	
2	DrvEn	In	Driver enable input	Weak PD [5]	Input	
3	ResetB	In	Reset pin	Weak PU	Input	
4	Start1	In/Out	Trigger pin actuator 1 / Flag_bus(3)	PU/PD ^{[6][7]}	Input	
5	Start2	In/Out	Trigger pin actuator 2 / Flag_bus(4)	PU/PD	Input	
6	Start3	In/Out	Trigger pin actuator 3 / Flag_bus(5)	PU/PD	Input	

MC33PT2001_SDS

All information provided in this document is subject to legal disclaimers.

Pin number	Pin name ^{[1][2][3]}	Pin function	Definition	Pull-up/pull-down	Reset
7	Start4	In/Out	Trigger pin actuator 4 / Flag_bus(6)	PU/PD	Input
8	Start5	In/Out	Trigger pin actuator 5 / Flag_bus(7)	PU/PD	Input
9	Start6	In/Out	Trigger pin actuator 6 / Flag_bus(8)	PU/PD	Input
10	Flag(0)	In/Out	Flag_bus(0) (general purpose I/O)	Weak PD	Input
11	Flag(1)	In/Out	Flag_bus(1) (general purpose I/O)	Weak PD	Input
12	Flag(2)	In/Out	Flag_bus(2) (general purpose I/O)	Weak PD	Input
13	Csb	In	SPI chip select	PU	Input
14	Mosi	In	SPI slave input	Weak PU	Input
15	Miso	Out	SPI slave output	_	Output: HiZ
16	Sclk	In	SPI clock	Weak PU	Input
17	VccIO	_	I/O voltage supply 3.3 V or 5.0 V	_	_
18	Dbg	In/Out	Debug port / Flag_bus(12)	Weak PU	Input
19	Dgnd	_	Digital ground	_	_
20	Vcc1p5	_	1.5 V voltage regulator decoupling	_	Regulator off
21	Vcc5	In	Power supply 5.0 V	_	_
22	OA_1	In/Out	Opamp output current sense 1 / Flag_bus(10)	Weak PD	Input
23	OA_2	In/Out	Opamp output current sense 2 / Flag_bus(11)	Weak PD	Input
24	Agnd	_	Analog ground	_	_
25	VsenseN1	In	Current sense 1 –	_	_
26	VsenseP1	In	Current sense 1 +	_	_
27	VsenseN2	In	Current sense 2 -	_	_
28	VsenseP2	In	Current sense 2 +	_	_
29	VsenseN3	In	Current sense 3	_	_
30	VsenseP3	In	Current sense 3	_	_
31	VsenseN4	In	Current sense 4	_	_
32	VsenseP4	In	Current sense 4	_	_
33	D_ls6	In	Drain pin low-side MOSFET actuator 6	_	_
34	D_ls5	In	Drain pin low-side MOSFET actuator 5	_	_
35	D_ls4	In	Drain pin low-side MOSFET actuator 4	_	_
36	D_ls3	In	Drain pin low-side MOSFET actuator 3	_	_
37	D_ls2	In	Drain pin low-side MOSFET actuator 2	_	_
38	D_ls1	In	Drain pin low-side MOSFET actuator 1	_	_
39	Vbatt	In	Battery voltage and drain pin for high-side predrivers	_	_

Pin number	Pin name ^{[1][2][3]}	Pin function	Definition	Pull-up/pull-down	Reset
40	VccP	_	7.0 V Voltage regulator decoupling	_	Regulator off
41	G_ls7	Out	Gate pin low-side MOSFET for DC/DC converter	_	Output: low
42	G_ls6	Out	Gate pin low-side MOSFET actuator 6	_	Output: low
43	G_ls5	Out	Gate pin low-side MOSFET actuator 5	_	Output: low
44	G_ls4	Out	Gate pin low-side MOSFET actuator 4	_	Output: low
45	G_ls3	Out	Gate pin low-side MOSFET actuator 3	_	Output: low
46	G_ls2	Out	Gate pin low-side MOSFET actuator 2	_	Output: low
47	G_ls1	Out	Gate pin low-side MOSFET actuator 1	_	Output: low
48	Vboost	In	Boost voltage and drain pin for boost predrivers	_	_
49	B_hs5	_	Bootstrap pin high-side MOSFET	_	_
50	G_hs5	Out	Gate pin high-side MOSFET HP	_	Output: low
51	S_hs5	In	Source pin high side MOSFET	_	_
52	B_hs4	_	Bootstrap pin Boost MOSFET	_	_
53	G_hs4	Out	Gate pin Boost MOSFET	_	Output: low
54	S_hs4	In	Source pin Boost MOSFET	_	_
55	B_hs3	_	Bootstrap pin high-side MOSFET	_	_
56	G_hs3	Out	Gate pin high-side MOSFET	_	Output: low
57	S_hs3	In	Source pin high-side MOSFET	_	_
58	B_hs2	_	Bootstrap pin Boost MOSFET	_	_
59	G_hs2	Out	Gate pin Boost MOSFET	_	Output: low
60	S_hs2	In	Source pin Boost MOSFET	_	_
61	B_hs1	_	Bootstrap pin high-side MOSFET —		_
62	G_hs1	Out	Gate pin high-side MOSFET	_	Output: low
63	S_hs1	In	Source pin high-side MOSFET —		_
64	IrqB	In/Out	Interrupt (output) / Flag_bus(9) Weak PD		Input
ePAD	Pgnd	_	Power ground		

- External 7.0 V is required in case the typical battery voltage is 24 V. Except for supply and ground, it is guaranteed by design unused pins can be kept open without any impact on the device. Unused VSENSEPx and VSENSENx pins can both be connected to GND. Weak pull-up to VCCIO (nominal value: 480 k Ω) Weak pull-down to AGND (nominal value: 480 k Ω) PU: Pull-up to VCCIO (nominal value: 120 k Ω) PD: Pull-down to AGND (nominal value: 120 k Ω) [2] [3] [4] [5] [6] [7]

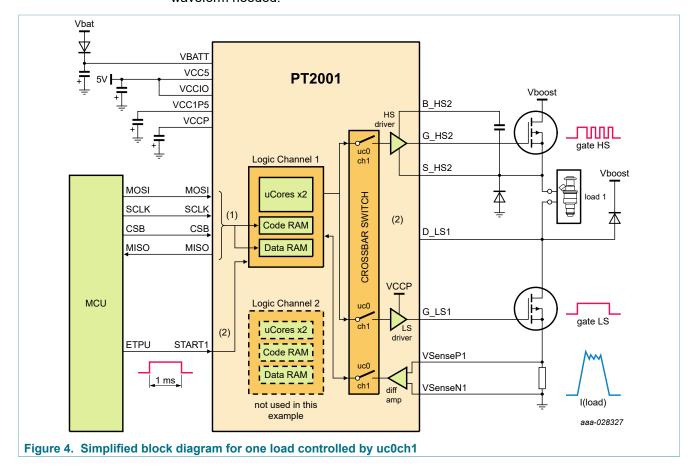
8 Functional description

8.1 Introduction

The PT2001 is a mixed signal IC for any solenoid control but more particularly to engine injector and electrical valve control. It provides a cost effective, flexible, and smart, high-side and low-side MOSFET gate driver. The device includes both individual charge pump outputs for each high-side predriver and high voltage DC/DC converter predriver. Gate drive, diagnostics, and protection against external faults, are managed through four independent and concurrent digital microcores. Each of the two logic channels including two microcores and their own code RAM and data RAM.

The internal microcode is protected against theft via encryption and corruption via check sums. Those microcores are optimized to control power MOSFET with a small latency time, they also allow to move the computation from MCU to PT2001 and use the MCU for other critical tasks. The PT2001 can control two banks of two/three injectors each.

- 1. At power up, MCU programs CRAM in PT2001 using SPI, this will define a particular state machine inside the core to generate a specific current shape. Once done PT2001 can control solenoid current by itself.
- 2. The solenoid turn ON/OFF is still controlled by the MCU most of the time from eTPU or GTM but also from a GPIO, which simply sends a pulse to the STARTx pin of PT2001. Then PT2001 controls gate HS and gate LS according to the current waveform needed.



8.2 Features

High-side and low-side predrivers

- Five high-side predrivers for logic level N-channel MOSFETs using four programmable slew rates
- Six low-side predrivers for logic level N-channel MOSFETs using four programmable slew rates
- · Integrated bootstrap circuitry for each high-side predriver
- Integrated charge pump circuitry for each high-side predriver with 100 % duty cycle capability
- · Configurable automatic freewheeling capability between high-side and low-side

DC/DC converter

- One low-side predriver, for a logic level N-channel MOSFET, can be optionally dedicated to providing a boost DC-DC converter with four programmable slew rates
- Two different control modes to reduce power dissipation (manual, hysteretic)

Current measurement

- Three independent current measurement blocks
- One current measurement (channel 4) is optionally configurable to support DC/DC converter

Diagnostics and monitoring

- V_{DS} and V_{SRC} monitoring (programmable values) for fault protection and diagnostics
- V_{BOOST} monitoring
- V_{BAT} monitoring
- · Temperature monitoring

Integrated end of injection detection

 Accurate detection of end of injection for each high-side source and low-side drain without any external component needed

Power supplies

- Integrated 7.0 V linear regulator (VCCP) for the HS/LS gate power supply
- Integrated 1.5 V linear regulator (VCC1P5) for the digital core supply based on the VCC5 input supply
- External 5.0 V supply (VCC5)
- Selectable VCCIO external supply (5.0 V or 3.3 V) for digital I/O

Digital block

- Four digital microcores, each with their own ALU, and full access to the system crossbar switch
- Two memory banks: 1024 x 16-bit of code RAM with built-in error detection and 64 x 16-bit of data RAM
- Memory BIST activated by the SPI, with pass/fail status
- · Control interface

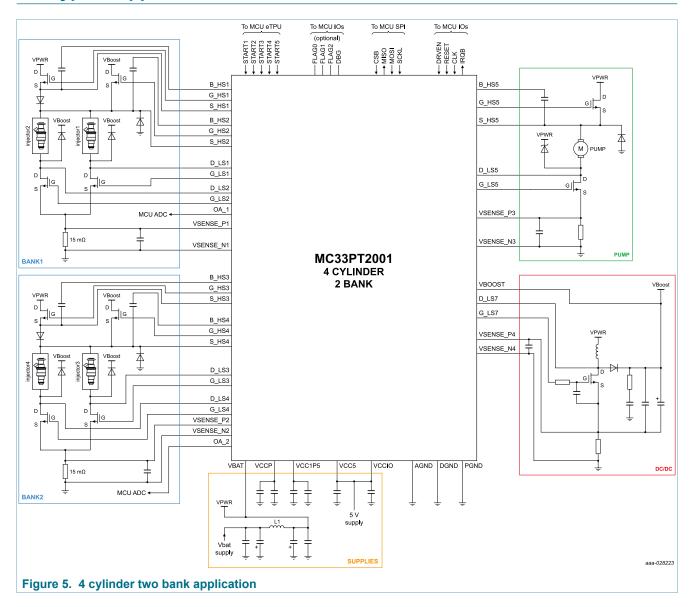
Control interface

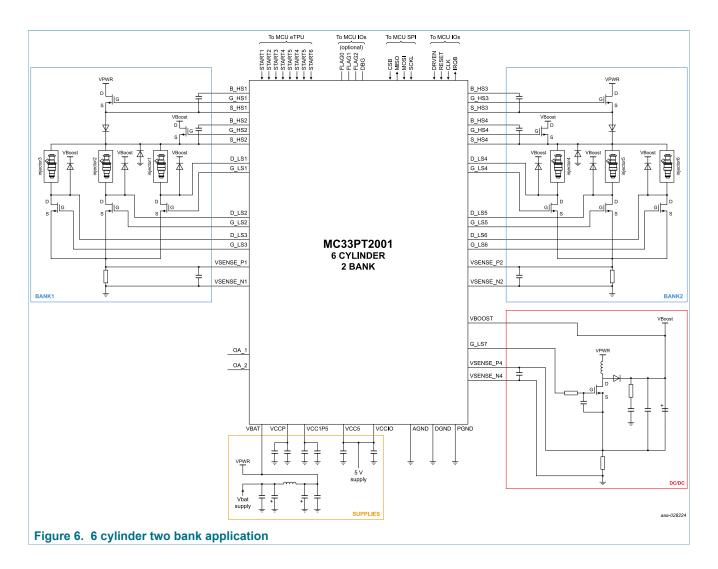
- 16-bit slave SPI up to 10 MHz two protocols programmable slew rate
- 16 general purpose digital IOs able to sustain up to 36 V
- Independent direct predriver inhibition input for safety purposes

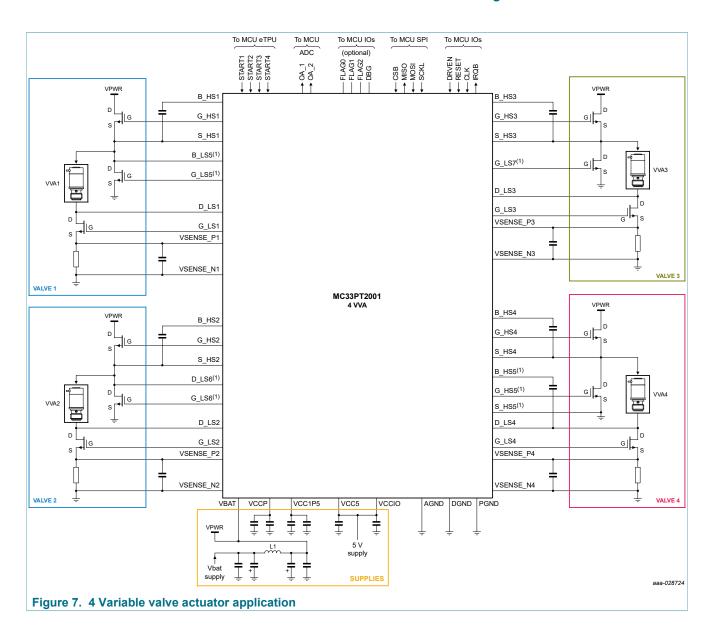
MC33PT2001_SDS

All information provided in this document is subject to legal disclaimers.

9 Typical application







10 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
Electrical ratings							
V _{BOOST}	DC voltage at VBOOST	_	0	_	72	V	
V _{BATT}	DC voltage at VBATT	_	-0.3	_	72	V	
V _{CC5}	DC voltage at VCC5	_	-0.3	_	36	V	
V _{CCIO}	DC voltage at VCCIO	_	-0.3	_	36	V	
V _{CC1P5}	DC voltage at VCC1P5	_	-0.3	_	2.0	V	

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DIG}	DC voltage at CLK, MISO, MOSI, SCLK, CSB, IRQB, RESETB	_	-0.3	_	36	V
V _{DRV_EN}	DC voltage at DRVEN	_	-0.3	_	36	V
V _{STARTX}	DC voltage at STARTx	_	-0.3	_	36	V
V_{FLAGX}	DC voltage at FLAGx	_	-0.3	_	36	V
V_{DBG}	DC voltage at DBG	_	-0.3	_	36	V
V _{OA_OUTX}	DC voltage at OA_1, OA_2	_	-0.3	_	36	٧
V_{DGND}	DC voltage at DGND	_	-0.3	_	0.3	V
V_{AGND}	DC voltage at AGND	_	-0.3	_	0.3	٧
V _{CCP}	DC voltage at VCCP	_	-0.3	_	9.0	V
V _{S_HSX}	S_HSx	DC voltage	-3.0	_	$V_{BOOSTMAX}$	٧
		Transients t < 800 ns	-6.0	_	V _{BOOSTMAX}	
		Transients t < 400 ns	-8.0	_	V _{BOOSTMAX}	
V _{B_HSX}	B_HSx	DC voltage	-0.3	_	V _{S HSX} +	V
_		Transients t < 800 ns	-2.0	_	V _{BS_HSX_CL}	
		Transients t < 400 ns	-4.0	_		
$V_{G_{-HSX}}$	DC voltage at G_HSx	_	VS_HSx-0.3	_	V _{B HSx} +0.3	V
V _{G_LSX}	G_LSx	DC voltage	-0.3	_	V _{CCP} +0.3	V
-		• Transients t < 5.0 µs;V = 8.0 V; energy of pulses < 0 V or > V is limited to 2.0 µJ due to capacitive coupling	-1.5		V _{CCP} + 1.5	
V_{D_LSX}	D_LSx	DC voltage	-3.0	_	75	V
		Transients t < 400 ns	-8.0	_	75	
V _{VSENSEN1/2/3}	DC voltage at VSENSEN1/2/3	Static at VCC5 < 10 V	-1.0	_	1.0	V
		• Dynamic for max 5.0 µs,1.0 kHz repetition rate at VCC5, 5.25 V	- 5.0	_	5.0	
		• Dynamic for max 1.0 µsat VCC5 < 5.25 V	–15	_	15	
V _{VSENSEP1/2/3}	DC voltage at VSENSEP1/2/3	DC voltage at VCC5 < 10 V	-2.5	_	2.5	V
		• Dynamic for max 5.0 μs,1.0 kHz repetition rate at VCC5 < 5.25 V	-5.0	_	5.0	
		• Dynamic for max 1.0 µsat VCC5 < 5.25 V	–15	_	15	
V _{VSENSEN4}	DC voltage at VSENSEN4	DC voltage at VCC5 < 10 V	-3.0	_	1.0	V
		Dynamic for max 5.0 μs,1.0 kHz repetition rate at VCC5 < 5.25 V Dynamic for max 1.0 μsat VCC5 < 5.25 V	-5.0	_	5.0	
		• Dynamic for max 1.0 µsat VCC5 < 5.25 V	–15	_	15	

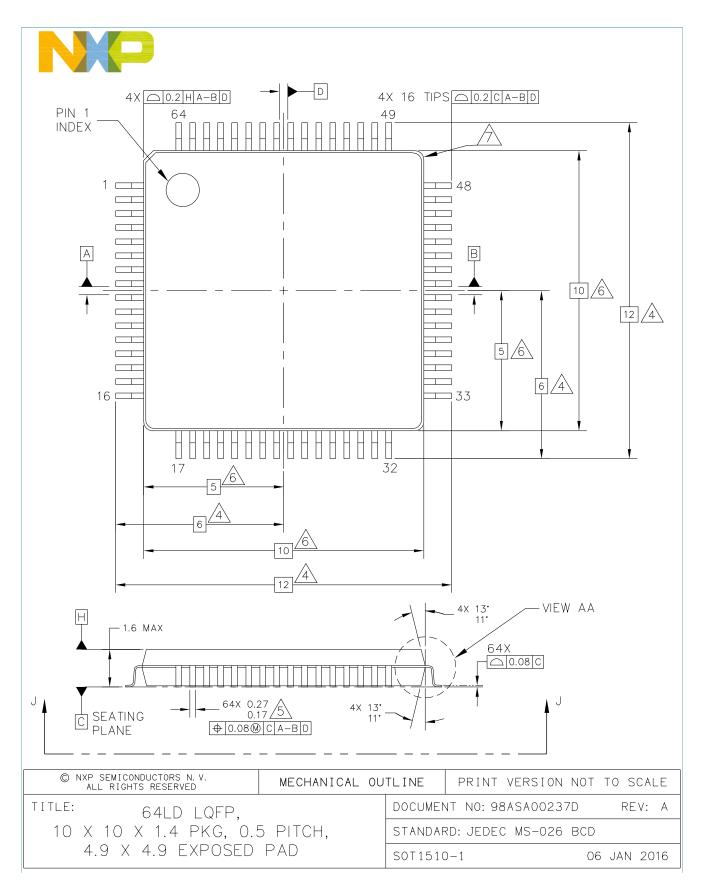
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{VSENSEP4}	DC voltage at VSENSEP4	DC voltage at VCC5 < 10 V	-4.2	_	2.5	V
		 Dynamic for max 5.0 μs,1.0 kHz repetition rate at VCC5 5.25 V 	-5.0	_	5.0	
		 Dynamic for max 1.0 μsat VCC5 < 5.25 V 	-15	_	15	
ESD voltage						'
	Human body model (HBM)					V
V _{ESD-HBM1}	VBOOST, VBATT, S_HSx	_	-4000	_	4000	
V _{ESD-HBM2}	• D_LSx	_	-8000	_	8000	
V _{ESD-HBM3}	All other pins	_	-2000	_	2000	
	Machine model					
V _{ESD-CDM1}	Corner pins	_	-750	_	750	
V _{ESD-CDM2}	All other pins	_	-500	_	500	
Thermal ratings						
	Operating temperature					°C
T _A	Ambient	_	-40	_	125	
T _J	Junction	_	-40	_	150	
T _{THRESHOLD}	Temperature monitoring threshold	_	167	_	187	°C
T _{STG}	Storage ambient temperature	_	-55	_	150	°C
Thermal resista	nce					'
$R_{\theta JA}$	Thermal resistance junction to ambient	_	_	_	25.3	°C/W
$R_{\theta JCTOP}$	Thermal resistance junction to case top	_	_	_	13.2	°C/W
R _θ ЈСВОТТОМ	Thermal resistance junction to case bottom	_	_	_	0.8	°C/W

MC33PT2001

Programmable solenoid controller

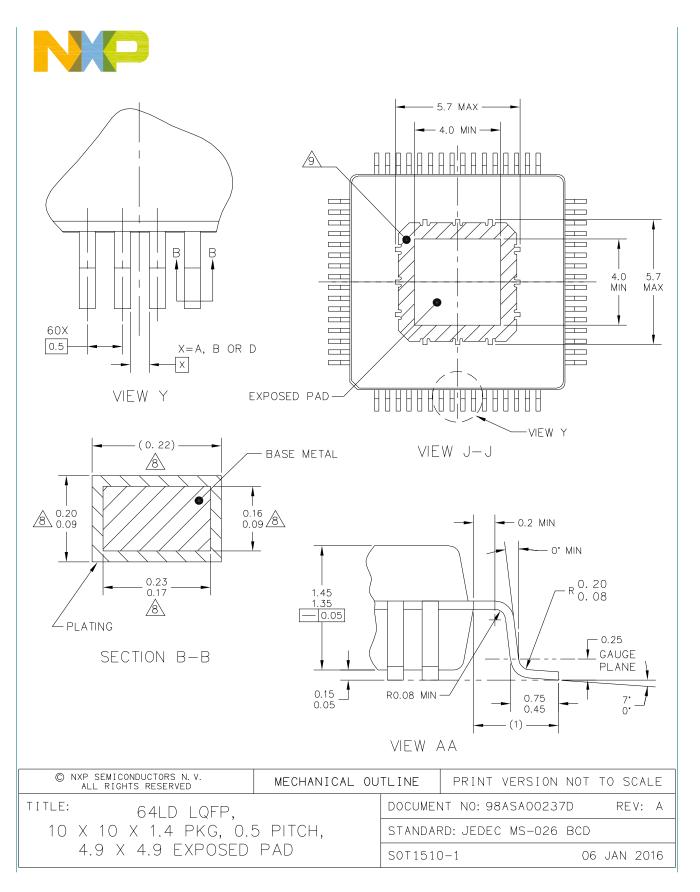
11 Package dimensions

For the most current package revision, visit www.nxp.com and perform a keyword search using the 98ASA00237D listed.



MC33PT2001_SDS

All information provided in this document is subject to legal disclaimers.



MC33PT2001_SDS

All information provided in this document is subject to legal disclaimers.



NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
- $\stackrel{\frown}{4}$ dimension to be determined at seating plane c.
- THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
- THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
- A EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- ATTHESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.
- ATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE		PRINT	VERSION NO	T TO SCALE
64LU LQFP,		DOCUMEN	NT NO: 98	3ASA00237D	REV: A
		STANDAF	RD: JEDE(C MS-026 BC	
4.9 X 4.9 EXPOSED	PAD	S0T1510)-1	(06 JAN 2016

Figure 8. Package outline

MC33PT2001_SDS All information provided in this document is subject to legal disclaimers.

12 Revision history

Table 4. Revision history

Document ID	Release date	Data sheet status	Change notice	Supercedes	
MC33PT2001_SDS v.3.0	20181130	Objective	_	MC33PT2001_SDS v.2.2	
Modifications	Changed revision number	Changed revision number to match data sheet			
MC33PT2001_SDS v.2.2	20180807	Objective	_	MC33PT2001_SDS v.2.1	
MC33PT2001_SDS v.2.1	20180622	Objective	_	_	

13 Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

13.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

 $\ensuremath{\mathbf{Applications}}$ — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected

MC33PT2001 SDS

All information provided in this document is subject to legal disclaimers.

to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

SMARTMOS — is a trademark of NXP B.V.

NXP Semiconductors

MC33PT2001

Programmable solenoid controller

Tables

Tab. 1. Tab. 2.	Orderable parts			
Figur	res			
Fig. 1. Fig. 2. Fig. 3. Fig. 4.	Simplified application diagram	Fig. 6. Fig. 7. Fig. 8.	4 cylinder two bank application	11 12

MC33PT2001

Programmable solenoid controller

Contents

1	General description	1
2	Features and benefits	
3	Simplified application diagram	2
4	Applications	
5	Ordering information	
6	Internal block diagram	
7	Pinning information	5
7.1	Pinning	
7.2	Pin description	
8	Functional description	
8.1	Introduction	8
8.2	Features	
9	Typical application	10
10	Maximum ratings	
11	Package dimensions	
12	Revision history	
13	Legal information	

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.