Advance Information

Switch Monitor Interface

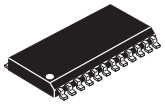
MC33884

The MC33884 Switch Monitor Interface is a monolithic silicon integrated circuit (IC) that performs switch monitoring functions. The device provides efficient interface between electrical switches and low voltage microprocessors. The MC33884 supplies switch contact pull–up and pull–down current while monitoring the input voltage level. All inputs are protected for transients when implemented with an appropriate static discharge capacitor used on the inputs.

There are four modes of operation – Sleep, Normal, Polling, and Polling + INT Timer. Sleep mode reduces the current drain to a quiescent current level of 10 μA and disables the IC. Normal mode interrupts the microprocessor whenever any external switch changes it's OPEN or CLOSED state. Polling mode reads a switch status periodically and interrupts the microprocessor only when an external switch is sensed as being CLOSED. The Polling + INT Timer mode is similar to the Polling mode, with the addition of an interrupt being sent to the microprocessor if a switch is sensed CLOSED or upon the internal interrupt timer "timing out". An interrupt is always ultimately sent to the microprocessor in this mode. All modes of operation are easily programmed via the Serial Peripheral Interface (SPI) control.

The MC33884 has the following features:

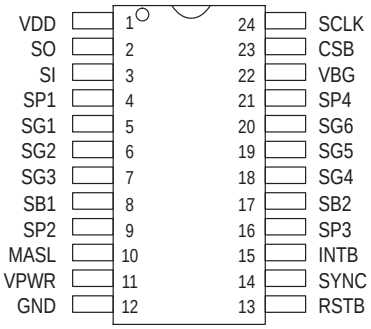
- Full Operation with 7.0 V ≤ V_{PWR} ≤ 26 V, Limited Operation with 5.5 V ≤ V_{PWR} ≤ 7.0 V
- Input Voltage Range: –14 V to 40 V
- Interfaces Directly to Microprocessors Using SPI Protocol
- 24–Lead Wide Body SOIC Package
- Wake–up on Change of Monitored Switch Status
- Programmable Wetting Current
- 4 Programmable Inputs to Monitor 4 Switch–to–Battery or 4 Switch–to–Ground Switches
- 6 (fixed function) Inputs to Monitor 6 Switch–to–Ground Switches
- 2 (fixed function) Inputs to Monitor 2 Switch–to–Battery Switches
- Standby Current During Normal Mode = 100 μA
- Quiescent Current in Sleep Mode < 10 μA
- Reset (RST) Input Defaults the Device to Sleep Mode
- Active Interrupt (INT) on Change of Switch State in Normal Mode
- 4 Modes of Operation (Sleep, Normal, Polling, Polling + INT Timer)
- Designed to Operate –40°C ≤ T_A ≤ 105°C



SCALE 1:1

DW Suffix
24 Lead SOIC
CASE 751E

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33884DW	T_A = – 40 to 105°C	SO–24
MC33884DWR2	T_A = – 40 to 105°C	SO–24

This document contains information on a new product. Specifications and information herein are subject to change without notice.

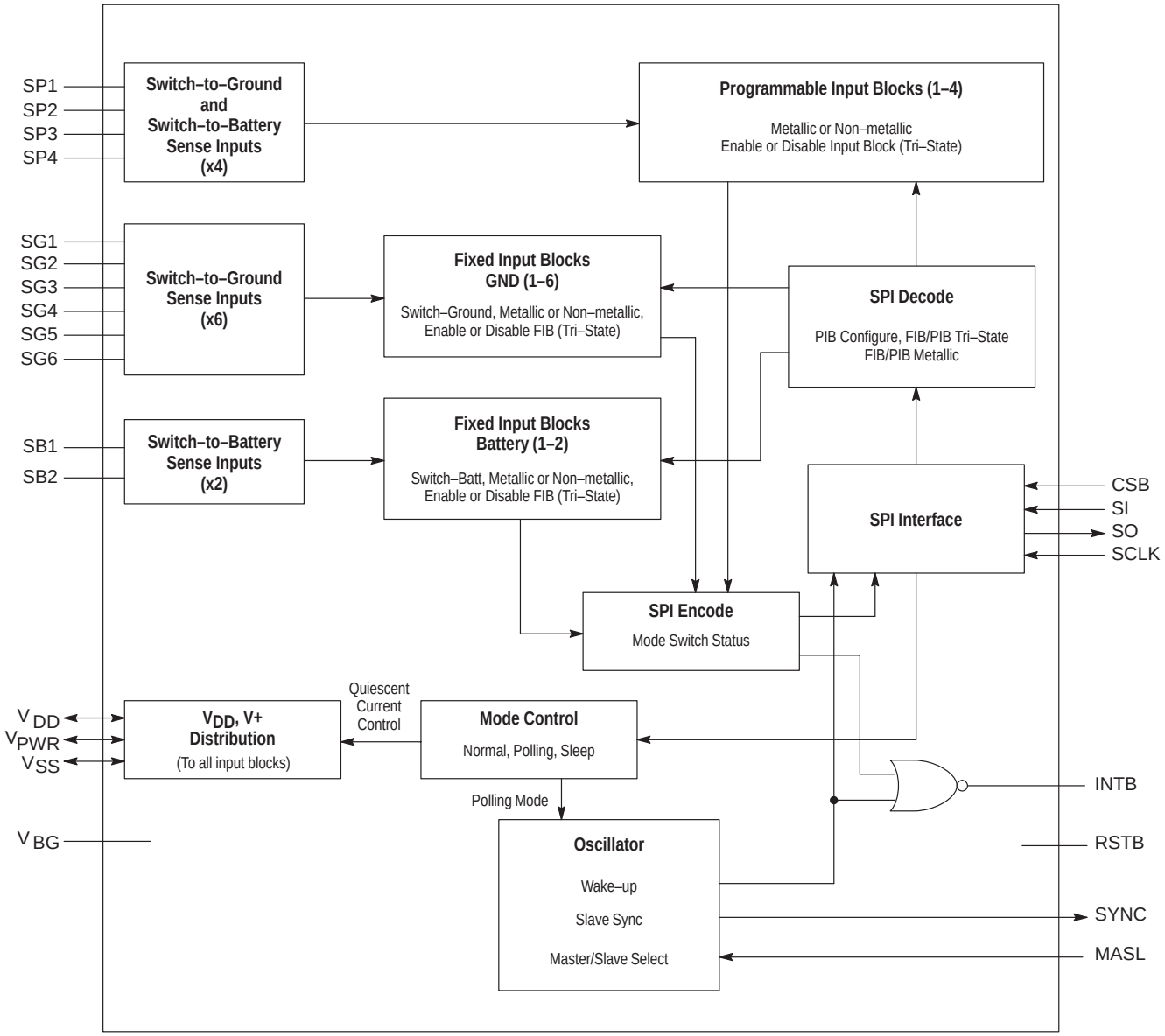


Figure 1. Internal Block Diagram

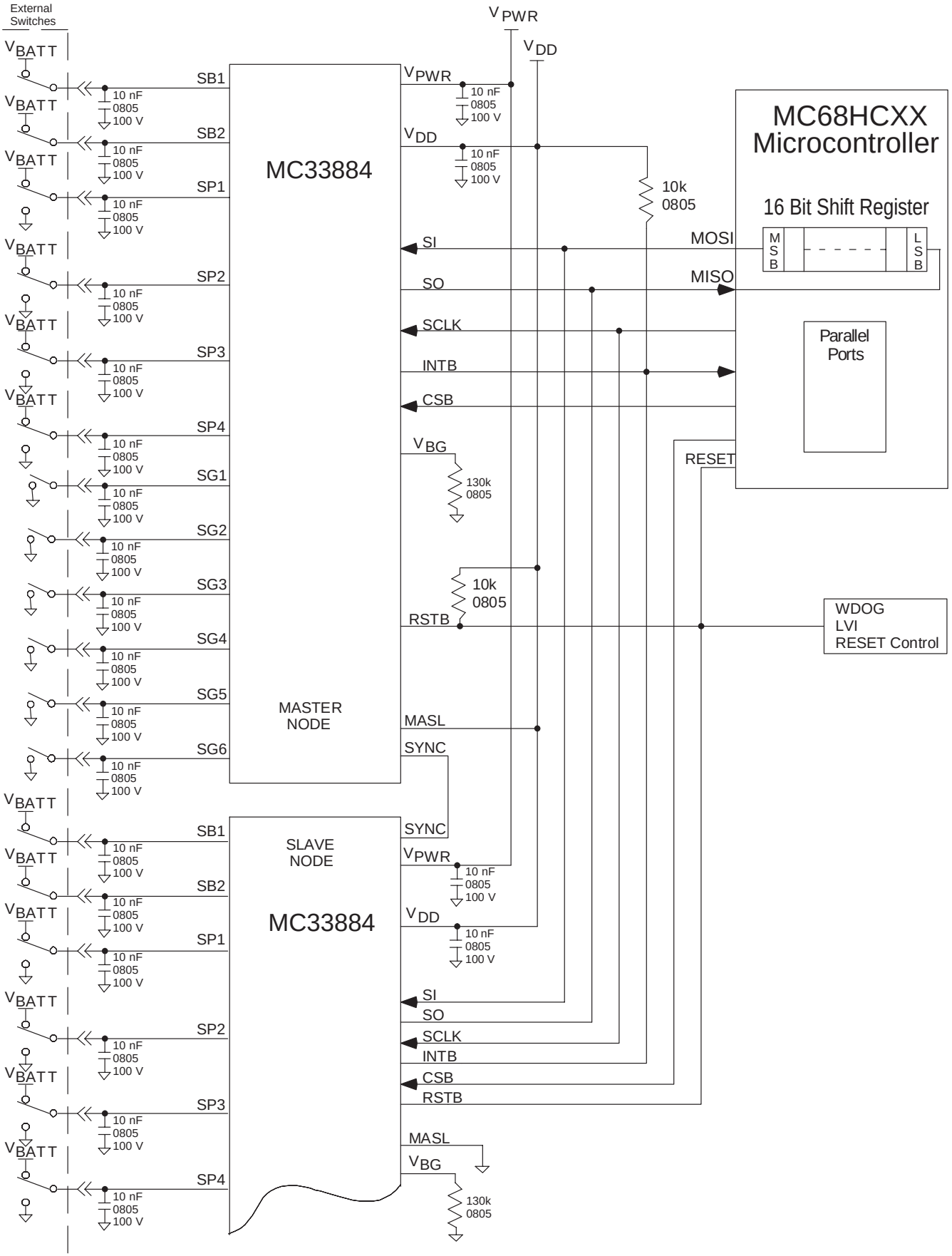


Figure 2. Typical Master / Slave Application

Pin Function Description

Pin	Name	Description
1	V_{DD}	5.0 V Logic Supply
2	SO	SPI Data Out Pin
3	SI	SPI Data In Pin
4	SP1	Programmable – Switch–to–Battery or Switch–to–Ground Input 1 (Source or Sink Output)
5	SG1	Switch–to–Ground Input 1 (Source Output)
6	SG2	Switch–to–Ground Input 2 (Source Output)
7	SG3	Switch–to–Ground Input 3 (Source Output)
8	SB1	Switch–to–Battery Input 1 (Sink Output)
9	SP2	Programmable – Switch–to–Battery or Switch–to–Ground Input 2 (Source or SInk Output)
10	MASL	Master or Slave Select Pin – Used when multiple MC33884 devices are required in Module
11	V_{PWR}	Conditioned Battery Supply Voltage
12	V_{SS}	Ground
13	RSTB	Reset Input
14	SYNC	Synchronization Output – Used when multiple MC33884 devices are required in Module. Provide synchronized wake–up of multiple MC33884 devices.
15	INTB	Interrupt – Open Drain Output
16	SP3	Programmable – Switch–to–Battery or Switch–to–Ground Input 3 (Source or Sink Output)
17	SB2	Switch–to–Battery Input 2 (Sink Output)
18	SG4	Switch–to–Ground Input 4 (Source Output)
19	SG5	Switch–to–Ground Input 5 (Source Output)
20	SG6	Switch–to–Ground Input 6 (Source Output)
21	SP4	Programmable – Switch–to–Battery or Switch–to–Ground Input 4 (Source or Sink Output)
22	V_{BG}	Bandgap Voltage. A bandgap reference is used to set up the reference and bias currents for the device. A resistor must be connected from this pin to ground.
23	CSB	Chip Select Input. Input with internal active pull–up. Requires 5.0 V CMOS logic levels. Communication with the device using SPI is enabled when the CSB pin is a logic 0.
24	SCLK	Serial Clock. SCLK is used to shift data into and out of the device. It transitions 1 time per bit with an operation frequency, f_{SCLK}, with a 50% duty cycle. SCLK is idle between commands and should be commanded low.

MAXIMUM RATINGS (All voltages are with respect to ground, unless otherwise noted)

Rating	Symbol	Value	Unit
V_{DD} Supply Voltage	–	–0.3 to 7.0	VDC
CSB, SI, SO, SCLK, RSTB, MASL, SYNC, INTB (Note 1)	–	–0.3 to 7.0	VDC
V_{PWR} Supply Voltage (Note 1)	–	–16 to 50	VDC
Switch Input Voltage Range	–	–14 to 40	VDC
Recommended Frequency of SPI Operation	–	3.0	MHz
ESD Voltage (Note 2) Human Body Model (Notes 3, 4, 5) Machine Model (Note 6)	 V_{ESD1} V_{ESD2}	 4000 200	V
Storage Temperature	T_{stg}	–55 to 150	°C
Operating Case Temperature	T_C	–40 to 105	°C
Operating Junction Temperature	T_J	–40 to 150	°C
Lead Soldering Temperature (Note 7)	T_{Solder}	260	°C
Maximum Junction Temperature	–	–40 to 150	°C
Thermal Resistance, Junction–to–Ambient Plastic Package, 24 SOIC, Case 751E:	$P_{\theta JA}$	107	°C/W

NOTES:

1. Exceeding these limits may cause malfunction or permanent damage to the device.
2. ESD data available upon request.
3. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
4. All pins when tested individually.
5. 1 kV on V_{PWR} and V_{DD} when connected together.
6. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 100 pF, R_{ZAP} = 0 Ω).
7. Lead soldering temperature limit is for 10 seconds maximum duration.

STATIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, –40°C ≤ T_C ≤ 105°C, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Units
POWER INPUT					
Supply Voltage Range Quasi–Functional (Note 1) Fully Operational	 $V_{PWR(qf)}$ $V_{PWR(fo)}$	 5.5 7.0	 – –	 7.0 26	V
Supply Current Normal Mode (I_{DD} + I_{PWR}) (All Switches Open)	$I_{PWR(on)}$	–	100	300	μA
Supply Current Sleep State ($I_{DD(SS)}$ + $I_{PWR(on)}$)	$I_{(ss)}$	–	2.0	10	μA
Supply Current Periodic Mode (Polling at 30–50 ms period) (All Switches Open)		–	26	–	μA
Logic Supply Voltage	V_{DD}	4.75	–	5.25	V
Bandgap Voltage Output Pin (Tested with 130 kΩ ± 0.1% resistor)	V_{BG}	1.18	1.26	1.4	V
SWITCH INPUT					
Pulse Wetting Current Switch to Battery	$I_{w(batt)}$	7.5	14	25	mA
Pulse Wetting Current Switch to Ground	$I_{w(gnd)}$	–7.5	–14	–25	mA
Sustain Current Switch to Battery	$I_{s(batt)}$	0.4	0.75	1.25	mA
Sustain Current Switch to Ground	$I_{s(gnd)}$	–0.4	–0.75	–1.25	mA
Tri–State Input Current	$I_{T(swt)}$	–10	–	10	μA
Switch Detection Threshold	I_{th}	3.25	3.75	4.75	V
Switch Input Voltage Range	V_{in}	–14	–	40	V
DIGITAL INTERFACE					
Input Logic Voltage Thresholds (Note 2)	$V_{IN(logic)}$	0.2 * V_{DD}	–	0.7 * V_{DD}	V
SO High State Output Voltage (I_{OH} = 1 mA)	$V_{OH(so)}$	3.5	–	–	V
SO Low State Output Voltage (I_{OL} = 1 mA)	$V_{OL(so)}$	–	–	0.4	V
SO Tri–State Leakage Current (CSB = 0.7 V_{DD}, V_{SO} = 0 to V_{DD})	$I_{T(so)}$	–40	–	40	μA
SI Pull–Down Current (SI = V_{DD})	I_{SI}	5.0	–	35	μA
SCLK Input Current (0 V = V_{DD})	I_{SCLK}	–10	–	10	μA
CSB Pull–Up Current (CSB = 0 V)	I_{CSB}	–25	–	–5.0	μA
RSTB Pull–Down Current (RSTB = 0 V)	I_{RSTB}	5.0	–	35	μA
INTB Low State Output Voltage (I_{OL} = 0.5 mA)	$V_{OL(INTB)}$	–	–	0.4	V
Input Capacitance on SCLK, SI, Tri–State SO, CSB (Note 3)	C_{IN}	–	–	20	pF

NOTES:
1. SPI inputs and outputs are operational; Fault reporting may not be fully operational within this voltage range.
2. Upper and lower logic threshold voltage levels apply to SI, CSB, SCLK, RSTB, SYNC, MASL.
3. This parameter is guaranteed by design, but not production tested

DYNAMIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, –40°C ≤ T_C ≤ 105°C, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.)

Characteristics	Symbol	Min	Typ	Max	Units
SWITCH INPUT					
Pulse Wetting Current Duration	t_{pulse}	30	34	43	ms
Interrupt Delay Time	$t_{INT(delay)}$	2.5	–	13	ms
SCLK Frequency vs. SO Load Capacitance 200 pF 160 pF 120 pF	f_{SCLK}	 3.2 3.5 4.0	–	–	MHz
DIGITAL INTERFACE TIMING					
Falling Edge of CSB to Rising Edge of SCLK (Note 1) (Required Set–up Time)	t_{lead}	–	100	140	ns
Falling Edge of SCLK to Rising Edge of CSB (Required Set–up Time)	t_{lag}	–	–	50	ns
SI to Rising Edge of SCLK (Required Set–up Time)	t_{SU2}	–	25	45	ns
Rising Edge of SCLK to SI (Required Hold Time)	t_{H2}	–	25	45	ns
SO to Rising Edge of SCLK (Required Set–up Time)	t_{SU1}	90	125	–	ns
Rising Edge of SCLK to Falling Edge of SO (Hold Time)	t_{H1}	90	125	–	ns
SO Rise Time, SO Fall Time (C_L = 200 pF)	$t_{r(SO)}$ $t_{f(SO)}$	–	30	50	ns
SI, CSB, SCLK Incoming SIgnal Rise Time (Note 2)	$t_{r(SI)}$	–	–	50	ns
SI, CSB, SCLK Incoming Signal Fall Time (Note 2)	$t_{f(SI)}$	–	–	50	ns
Time from Falling Edge of CSB to SO Low Impedance (Note 3)	$t_{SO(en)}$	–	80	110	ns
Time for Rising Edge of CSB to SO High Impedance (Note 4)	$t_{SO(DIS)}$	–	80	110	ns
Time from Falling Edge of SCLK to SO Data Valid (Note 5)	t_{valid}	–	65	105	ns
Recovery Time for Sequential Transfers	t_{REC}	–	100	120	ns

NOTES:
1. This parameter is guaranteed by design, but not production tested.
2. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
3. Time required for output status data to be available for use at SO pin.
4. Time required for output states data to be terminated at SO pin.
5. Time required to obtain valid data out from SO following the falling edge of SCLK.

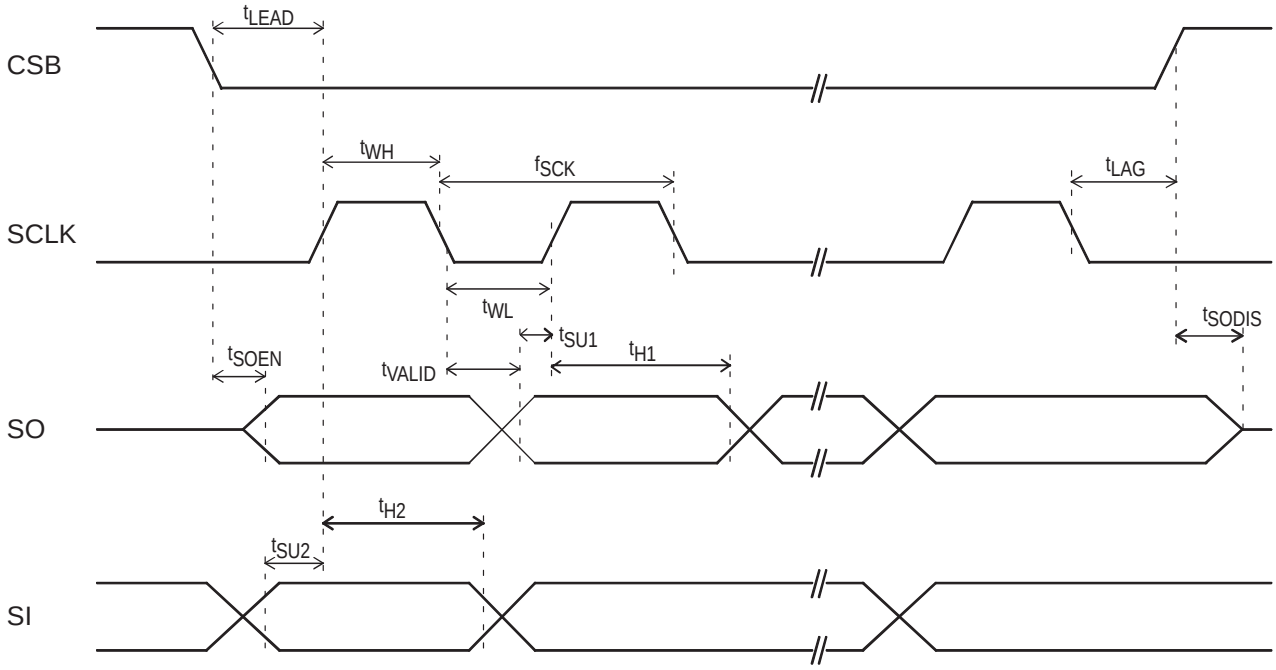


Figure 3. SPI Timing Diagram

CIRCUIT DESCRIPTION

Introduction

The MC33884 is a monolithic integrated circuit designed to interface between external electrical system switches and low voltage microprocessors via a Serial Peripheral Interface (SPI). The MC33884 monitors the OPEN/CLOSED status of multiple external switches used in a system. The MC33884 features 4 programmable Switch–to–Ground or Battery sense inputs, 6 Switch–to–Ground sense inputs, 2 Switch–to–Battery sense inputs, programmable Wake–up Timer, programmable Interrupt Timer, and programmable wetting current settings. All inputs are protected for ESD transients when implemented with the appropriate ESD capacitor.

There are numerous applications for this device in aircraft, aerospace, robotic, process & control, automotive, and security systems. Potential applications exist where switch status verification for safety, fault tolerant operation, or process control function purposes are critical.

The MC33884 has four modes of operation: Sleep, Normal, Polling, and Polling + INT Timer.

The MC33884 is designed to provide a robust interface between system switch contacts and a microprocessor. Each MC33884 input provides the switch contact with high levels of wetting current during switch closure. After the input switch has been closed for 20 ms, the wetting current is reduced, hence reducing power dissipation in the IC. The response to a SPI command will always return Switch Status, Master/Slave, INT Flag, and Mode settings. The following section describes the programming modes and features of the MC33884.

Microprocessor Interface

The MC33884 directly interfaces to 3.3 or 5.0 V MCU. SPI serial clock frequencies in excess of 5.0 MHz may be used for programming and reading switch input status. Figure 4 shows the configuration between an MCU and one MC33884.

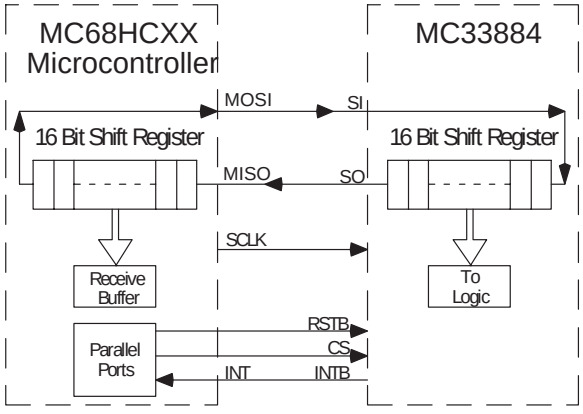


Figure 4. SPI Interface with Microprocessor

The MC33884, though originally designed for automotive use, is very useful in a variety of other applications, i.e., computer, telecommunications, and industrial fields. It is parametrically specified over an input battery/supply voltage of 9.0 to 16.0 V but is designed to operate over a considerably wider range of 5.5 to 26.5 V.

Two or more MC33884 devices may be used in a module system when implemented in a parallel or serial configuration. Figure 5 and Figure 6 show the parallel and serial configurations respectively. When using the Serial configuration, 32 clock cycles are required for a complete transfer of data to the MC33884.

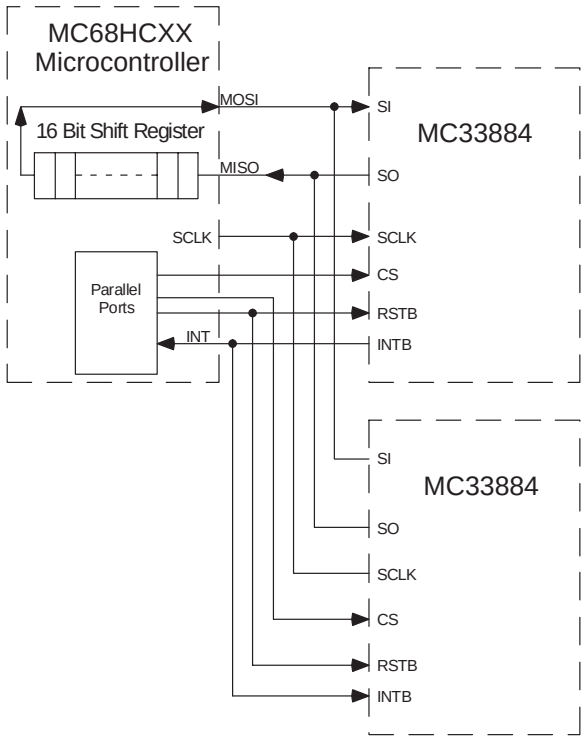


Figure 5. SPI Parallel Interface with Microprocessor

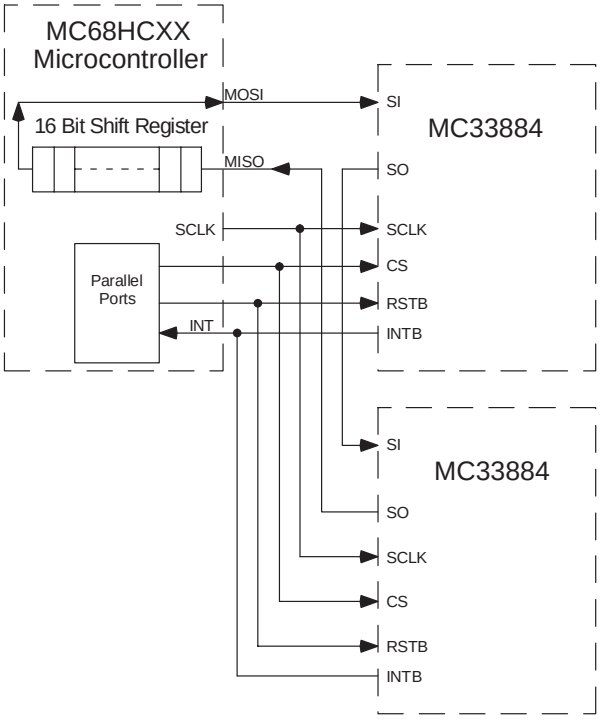


Figure 6. SPI Serial Interface with Microprocessor

PIN FUNCTIONAL DESCRIPTION

CSB Pin

The system MCU selects the MC33884 to be communicated with through the use of the CSB pin. With the CSB in a logic low state, command words may be sent to the MC33884 via SI and switch status can be received by the MCU via SO. Falling edge of CSB enables the SO output, latches the state of the INTB pin, operating mode and the state of the external switch inputs. Rising edge of CSB disables the SO driver, resets the INTB pin to logic [1], activates the received command word, and allows the MC33884 to act upon new data obtained from switch inputs. To avoid any spurious data, it is essential that the high–to–low and low–to–high transition of the CSB signal occur only when SCLK is in a logic low state. Internal to the MC33884 is an active pull up on CSB.

SCLK Pin

The system clock pin (SCLK) clocks the internal 16–bit shift register of the MC33884. The serial input (SI) data is latched into the input shift register on the rising edge of SCLK signal. The serial output pin (SO) shifts the switch status bits out on the falling edge of SCLK. False clocking of the shift register must be avoided to guarantee validity of data. It is essential that the SCLK pin be in a logic low state whenever chip select pin (CSB) makes any transition. For this reason it is recommended, though not necessary, that the SCLK pin be commanded to a low logic state as long as the device is not accessed (CSB in logic high state). When the CSB is in a logic high state, any signal on the SCLK and SI pin will be ignored and the SO pin is Tri–Stated (high impedance).

SI Pin

This pin is used for serial instruction data input. SI information is latched into the input register on the rising edge of SCLK. A logic high state present at SI when SCLK rises, programs a [1] into the command word on rising edge of the CSB signal. To program a complete word, 16 bits of information must be entered into the MC33884. Internal to the IC is an active pull down on the SI pin.

SO Pin

The serial output (SO) pin is the output from the shift register. The SO pin remains Tri–State until the CSB pin transitions to a logic low state. All “open switches” are reported as [0], all ‘closed switches’ are reported as [1]. The negative transition of CSB will make status bit 15 available on SO. Each successive negative clock will make the next status bit available. The SI/SO shifting of the data follows a first–in–first–out protocol with both input and output words transferring the Most Significant Bit (MSB) first.

MASL pin

The MASL pin is required when multiple MC33884 devices are used in one module. The MASL (Master/Slave) identifies which device will be the master and which will be the slave. Master/Slave identification is used during Polling mode. In the Polling mode the Master device has it’s internal oscillator running while the Slave device oscillator is shutdown. When polling the Master device wakes the Slave via the SYNC pin. This feature provides minimal quiescent from V_{PWR} and V_{DD} pins.

SYNC Pin

The SYNC input is used by slave IC during Polling mode. The SYNC allows multiple MC33884 ICs to poll the multiple inputs at the same time. The Master controls the polling period. The Slave is allowed to shut down it’s oscillator to conserve current. When the Slave receives the SYNC signal from the Master, the Slave starts the internal oscillator and reads the switch inputs.

INTB Pin

The INTB pin is an interrupt output from the MC33884. The INTB pin is an open drain output with an internal pull up. In normal mode a switch state change will trigger the INTB pin. The INTB pin and INT bit (flag) is latched on falling edge of CSB. This permits the MCU to determine the origin of the interrupt. The flag INT bit in the SPI word is the inverse of the INTB pin. The INTB pin is cleared on rising edge of CSB. In Polling mode the INTB pin is active only during the ON time (when sink and source currents are active).

RSTB Pin

The RSTB pin is active low reset input to the MC33884. When asserted, the MC33884 will reset all internal registers, timers, and enter a sleep mode (with all switch inputs in a Tri–State condition). Only an MCU SPI command word will wake the MC33884 from a sleep state. The RSTB pin may be controlled directly from a general purpose I/O pin or from a system/MCU reset.

V_{BG} Pin

The V_{BG} pin requires a 130 kΩ to ground for standard wetting and sustain currents. The device is tested with a 0.1% value, but a standard 1.0% could be used for proper functionality.

V_{PWR} Pin

V_{PWR} pin is battery/supply source pin for the MC33884. The V_{PWR} pin requires external reverse battery/supply and transient protection. Maximum input voltage on V_{PWR} is 40 volts. All wetting currents and sustain currents are derived from V_{PWR}.

SP1 – SP4 Pins

The MC33884 has 4 switch sense inputs that may be programmed to read switch–to–ground or switch–to–battery/ supply contacts. Transient battery/supply voltages greater than 40 volts must be clamped by an external device. Surface mount 0805 MOVs and transient voltage suppressors (TVS) are available in SOT–23 packages. The sensed input is compared with an internal 4.0 volt reference. When programmed to sense switch–to–battery, sensed voltages greater than 4.0 volts are interpreted as a CLOSED switch. Sensed voltages less than 4.0 V are interpreted as an OPEN switch. The opposite holds true when inputs are programmed to sense switch–to–ground. Further programming can set the wetting currents or make the inputs Tri–State. Programming methods are provided in the following section.

PIN FUNCTIONAL DESCRIPTION (continued)

SB1, SB2 Pins

The SB pins are switch–to–battery sensing inputs only. Transient battery/supply voltages greater than 40 volts must be clamped by external device. Surface mount 0805 MOVs and transient voltage suppressors (TVS) are available in SOT–23 packages. The sensed input is compared with an internal 4.0 volts reference. Voltages greater than 4.0 volts are interpreted as a CLOSED switch. Sensed voltages less than 4.0 V are interpreted as an OPEN switch. Programming can set wetting currents or Tri–State the input. Programming methods are provided in the following section.

SG1 – SG6 Pins

The SG pins are switch–to–ground inputs only. The input is compared with the internal 4.0 volt reference. Voltages greater than 4.0 volts are interpreted as an OPEN switch. Voltages less than 4.0 V are interpreted as a CLOSED switch. Programming can set the wetting currents or Tri–State the input. Programming methods are provided in the following section.

FUNCTIONAL DESCRIPTION

POWER UP

On initial power up, all MC33884 registers will be cleared and the device will enter the Sleep mode. To exit Sleep mode a valid command word is required to be received from the microprocessor.

Sleep Command

Sleep mode can be entered by a SPI Sleep command or asserting the RSTB pin. In Sleep mode all inputs are Tri–State and all internal active pull up and pull down currents are disabled. Sleep mode reduces the current drain to a quiescent current level of 10 μA and disables the IC. Sleep mode provides lowest quiescent current for the IC. Exit from sleep mode requires a valid SPI RUN, TRI–STATE, or METALLIC command.

RUN Command

Run command places the IC in one of three operating modes; Normal, Polling, and Polling + INT Timer. The command also programs the SP1 to SP4 sense inputs (switch–to–battery [1] or switch–to–ground [0]). See Table 1.

Normal mode is the normal operating mode of the MC33884. In Normal Mode the status of the input switches are latched on falling edge of CSB and data is sent back to MCU via SPI. All programmed combinations of source and sink currents, used for sensing purposes, are always active in this mode. In normal mode an interrupt is generated and sent to the microprocessor whenever an external switch changes its OPEN or CLOSED state. Prior to a switch closing, the MC33884 sources 0.75 mA of sustain current. When the voltage at the input crosses the comparator threshold, 14 mA of current is allowed to flow. The 14 mA wetting current shuts off after a 20 ms timer expires.

Polling mode reads a switch status periodically and interrupts the microprocessor only when an external switch is sensed as being CLOSED. If the MC33884 senses all external switches to be OPEN, the Polling mode of operation continues. If a switch is sensed CLOSED, an interrupt is sent to the microprocessor and the MC33884 transfers it's operational mode to the Normal mode. The Polling mode provides a reduction in quiescent current by turning OFF all source and sink currents during sensed switch OFF periods. The Polling mode allows the user to reduce quiescent current by disabling sink and source currents during swtich "OFF" periods.

Polling + INT Timer mode of operation is similar to the Polling mode above, with the addition of an interrupt being sent to the microprocessor if a switch is sensed CLOSED or upon the internal interrupt timer "timing out". An interrupt is always ultimately sent to the microprocessor in this mode. The microprocessor can be programmed to read (or ignore) the MC33884's reported switch status upon receiving the interrupt. If a switch is sensed CLOSED, operation reverts automatically to the Normal mode. If all switches are sensed OPEN, and the wake–up timer (INT Timer) times out, the MC33884 continues to operate in the Polling + INT Timer mode. The wake–up timer duration may be set much longer than the Polling time.

TRI–STATE Command

TRI–STATE command places all switch inputs into Tri–State. All comparators on inputs are disabled in this mode. The device will return [0] for the switch status.

SPI PROGRAMMING

The MC33884 uses the SPI in full duplex synchronous slave mode for communication with the microprocessor. The MC33884 is programmed via a 16 bit word command from the MCU. The word is sent to the device with the MSB first. The command word sent to the MC33884 sets the mode of operation in the device. Data received back from the MC33884 is the status of the sensed input switch on falling edge of CSB. Sixteen clock periods are required for each transmission to be valid. After the 16 clocks, CSB is returned to the inactive state (logic [1]), command words are no longer accepted into SI, and the SO pin is Tri–Stated. The response to a SPI command returns status based on previous command word. This previous command could be a hardware reset as well as any of the other commands discussed in this section.

PROGRAMMING AND CONFIGURATION DESCRIPTION

SPI Commands from Microcontroller

Command Protocol (Data into SI)

Table 1: SPI Command Protocol

Command	MSB Bit 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	LSB Bit 1
Sleep [DEFAULT]	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
Run	0	0	0	1	MOD2	MOD1	ST3	ST2	ST1	–	WT2	WT1	CP4	CP3	CP2	CP1
Tri–State	0	0	1	1	TG6	TG5	TG4	TG3	TG2	TG1	TP4	TP3	TP2	TP1	TB2	TB1
Metallic	0	1	0	1	MG6	MG5	MG4	MG3	MG2	MG1	MP4	MP3	MP2	MP1	MB2	MB1
IC Test Mode	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
RESET VALUES:																
Run Register	—	—	—	—	U	U	U	U	U	U	U	U	U	U	U	U
Tri–State Register	—	—	—	—	0	0	0	0	0	0	0	0	0	0	0	0
Metallic Register	—	—	—	—	U	U	U	U	U	U	U	U	U	U	U	U

U: Unknown value coming out of Sleep mode; must configure with Run and Metallic commands.
NOTE: the remaining combinations of Bits [16:13] are NON–FUNCTIONAL (0010, 0100, 0110, 0111)

LABEL DEFINITIONS			
MOD[2:1]	Operating Mode	ST[3:1]	Sample OFF Time
CP[4:1]	Configure Programmable Switch	WT[3:1]	Wake–Up Time
TG[6:1]	Tri–State Switch–to–Ground	MG[6:1]	Metallic Switch–to–Ground
TB[2:1]	Tri–State Switch–to–Battery	MB[2:1]	Metallic Switch–to–Battery
TP[4:1]	Tri–State Programmable Switch	MP[4:1]	Metallic Programmable Switch

Sleep Command

The Sleep command places the IC in Sleep mode and essentially turns off the part. By definition, a hardware reset sends/keeps the IC in Sleep mode. All inputs are Tri–Stated, disabling all input blocks and all internal pull–ups/pull–downs. Only a SPI command can take the IC out of Sleep mode. Exiting this mode requires a valid Run, Tri–State, or Metallic command.

Command	MSB Bit 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	LSB Bit 1
Sleep [DEFAULT]	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X

DESCRIPTION (Continued)

Run Command

The Run command gives access to all of the operating modes: Normal, Polling, and Polling + INT Timer. It allows selection of t_{WAIT} and t_{WAKE}, and configures the programmable input blocks. Bit 7 is currently unused. Note that the Run register values are unknown after exiting the Sleep mode.

	MSB Bit															LSB Bit
Command	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
Run	0	0	0	1	MOD2	MOD1	ST3	ST2	ST1	–	WT2	WT1	CP4	CP3	CP2	CP1
RESET VALUES:																
Run Register	—	—	—	—	U	U	U	U	U	U	U	U	U	U	U	U

U: Unknown value coming out of Sleep mode; must configure with Run command.

MOD[2:1] — Operating Mode

In the Run command, the two MOD bits place the device in one of three operating modes: Normal, Polling, and Polling + INT Timer.

Bit Definitions for Run Command
COMMAND: Run (0001), with bits[12:1] as follows

MODE	MOD2	MOD1	ST[3:1]	WT[2:1]	CP[4:1]
Undefined	0	0	XXX	XX	XXXX
Normal	0	1	XXX	XX	CP[4:1]
Polling	1	0	ST[3:1]	XX	CP[4:1]
Polling + INT Timer	1	1	ST[3:1]	WT[2:1]	CP[4:1]

ST[3:1] — OFF Time between Samples (t_{WAIT})

During both Polling modes (with and without INT Timer 'Wake–Up', MOD2=[1]), these bits select the interval of time (t_{WAIT}) that the Input Blocks are turned OFF; switch transitions are not detected during the OFF interval.

Sample OFF Time Prescales

ST[3:1]	Multiplier Selected	OFF Time, t_{WAIT} (ms) [t_{DETECT} (4.8ms typ.) * Multiplier]	ON Time (ms)
000	5	15 – 25	5.1 – 6.3
001	9	30 – 55	5.1 – 6.3
010	17	60 – 90	5.1 – 6.3
011	25	100 – 140	5.1 – 6.3
100	33	145 – 185	5.1 – 6.3
101	41	195 – 215	5.1 – 6.3
110	49	220 – 245	5.1 – 6.3
111	57	250 – 320	5.1 – 6.3

DESCRIPTION (Continued)

WT[2:1] — Wake–Up Time

These bits let the device assert an external interrupt (INTB) at the following intervals during Polling mode (MOD2=MOD1=1).

Wake–Up Delay Prescales

WT[2:1]	Multiplier Selected	Wake–Up Interrupt, t_{WAKE} (ms) [t_{DETECT} (2.8ms typ.) * Multiplier]
00	512+1	2400 – 3200
01	256+1	1200 – 1600
10	128+1	600 – 750
11	64+1	290 – 360

CP[4:1] — Configure Programmable Switch

Configure the programmable inputs SP[4:1] to detect either an external switch–to–ground (internal current source) or an external switch–to–battery (internal current sink). Note that this configuration may be entered in any of the three valid Operating Modes (see MOD[2:1]) within the Run command.

Programmable Switch Bit Definition

CPx	External Switch to:
0	Ground
1	Battery

Tri–State Command

This command places an external switch into a “Tri–State” condition, essentially disconnecting the wetting current (if the switch is metallic) and the sustain current. The internal input–threshold comparator is still internally connected to its external pin. This command does not change the mode of operation (e.g., a Tri–State command received while in Polling mode leaves the part in that mode). Note that the Tri–State register clears all bits to [0] (all inputs in Tri–State) in response to a hardware reset; all inputs also remain in Tri–State after exiting the Sleep mode.

	MSB Bit															LSB Bit
Command	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Tri–State	0	0	1	1	TG6	TG5	TG4	TG3	TG2	TG1	TP4	TP3	TP2	TP1	TB2	TB1
RESET VALUES:																
Tri–State Register	—	—	—	—	0	0	0	0	0	0	0	0	0	0	0	0

TG[6:1] — Tri–State Switch–to–Ground
TB[2:1] — Tri–State Switch–to–Battery
TP[4:1] — Tri–State Programmable Switch

Tri–State Bit Definition

TGx, TBx, TPx	Input Configured to:
0	Input Disabled [DEFAULT]
1	Input Enabled

DESCRIPTION (Continued)

Metallic Command

This command enables the pulsed wetting current for an external metallic switch and disables it for an external non–metallic switch. This command does not change the mode of operation (e.g., a Metallic command received while in Polling mode leaves the part in that mode). Note that the Run register values are unknown after exiting the Sleep mode.

	MSB Bit															LSB Bit
Command	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
Metallic	0	1	0	1	MG6	MG5	MG4	MG3	MG2	MG1	MP4	MP3	MP2	MP1	MB2	MB1
RESET VALUES:																
Metallic Register	—	—	—	—	U	U	U	U	U	U	U	U	U	U	U	U

U: Unknown value coming out of Sleep mode; must configure with Metallic command.
MG[6:1] — Metallic Switch–to–Ground
MB[2:1] — Metallic Switch–to–Battery
MP[4:1] — Metallic Programmable Switch

Metallic Switch Bit Definition

MGx, MBx, MPx	Accepted Switch Type:
0	Non–metallic
1	Metallic (enable wetting current pulse)

Test Mode

Bit 16 is reserved for placing the device into a special IC Test mode. It is used to confirm various internal functions.

	MSB Bit															LSB Bit
Command	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
IC Test Mode	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

DESCRIPTION (Continued)

SPI Responses

Response Protocol (Data out of SO)

Table 1: SPI Response Protocol

Mode	MSB Bit 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	LSB Bit 1
Reset/Sleep	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Normal	0	1	MASL	INT	SG6	SG5	SG4	SG3	SG2	SG1	SP4	SP3	SP2	SP1	SB2	SB1
Polling	1	0	MASL	X	SG6	SG5	SG4	SG3	SG2	SG1	SP4	SP3	SP2	SP1	SB2	SB1
Polling + INT Timer	1	1	MASL	INT	SG6	SG5	SG4	SG3	SG2	SG1	SP4	SP3	SP2	SP1	SB2	SB1

LABEL DEFINITIONS			
SG[6:1]	Switch–to–Ground Flag	MASL	Master/Slave Identification Flag
SB[2:1]	Switch–to–Battery Flag	INT	External Interrupt Flag
SP[4:1]	Programmable Switch Flag		

Reset/Sleep

When the Reset (RSTB) input is active (logic [0]), all internal registers are cleared, thereby placing the device in Sleep mode and upon the RSTB input returning to the inactive state (logic [1]) the MC33884 remains in Sleep mode. A SPI command, received from the microprocessor, is necessary to command the device out of Sleep mode.

Mode	MSB Bit 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	LSB Bit 1
Reset/Sleep	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Note: The SPI response given while sending the command to exit Sleep mode should be ignored due to unknown power–up state.

DESCRIPTION (Continued)

Normal and Periodic

Bits [16:15] identify one of the three operating modes: Normal, Polling, and Polling + INT Timer. The remaining bits identify the device as the Master or a Slave, whether the device has an interrupt that has not been cleared, and the state of all the inputs.

Mode	MSB Bit 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	LSB Bit 1
Normal	0	1	MASL	INT	SG6	SG5	SG4	SG3	SG2	SG1	SP4	SP3	SP2	SP1	SB2	SB1
Polling	1	0		X												
Polling + INT Timer	1	1		INT												

MASL — Master/Slave Identification Flag

This flag is the same as the state of the MASL pin. It provides software identification of the configuration of each IC.

MASL Bit Definition

MASL	Device is a
0	Slave
1	Master

INT — External Interrupt Flag

This flag identifies this particular IC as the initiator of an external interrupt. It is the inverse of INTB.

INT Bit Definition

Mode	Bit 16	15	14	13	Type of Interrupt
Normal	0	1	X	0	Nothing has happened
				1	Switch Interrupt
Polling	1	0	X	X	–
Polling + INT Timer	1	1	X	0	Nothing has happened
				1	Wake–Up Interrupt

SG[6:1] — Switch–to–Ground Flag
SB[2:1] — Switch–to–Battery Flag
SP[4:1] — Programmable Switch Flag

These twelve flags indicate the state of all switch inputs:

Switch State Bit Definition

SGx, SBx, SPx	External Switch is:	Mode	Input States Latched:
0	Open	Normal	At the moment CSB transitions to logic 0.
1	Closed	Polling	

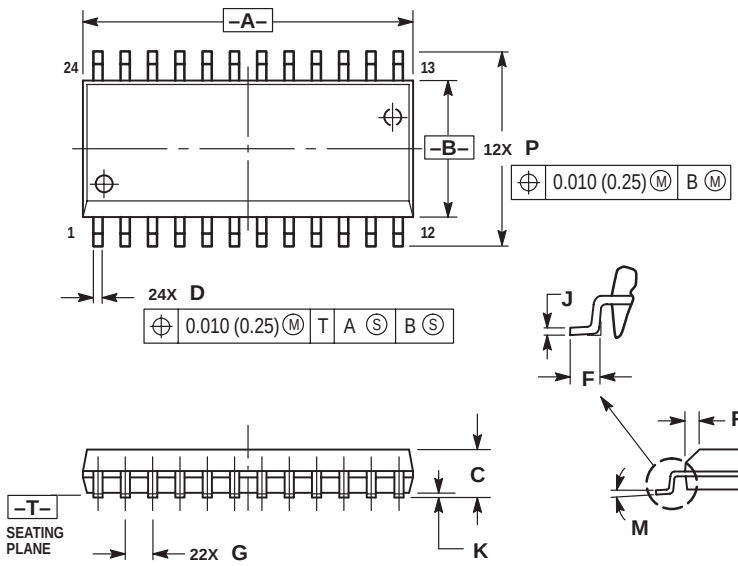
Tri–State

All Tri–State inputs have their wetting and sustain currents disabled. By definition, all disabled inputs return the following value for the switch state whenever SPI data is exchanged:

Tri–State Bit Definition

SGx, SBx, SPx	External Switch is:
0	Tri–State

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

CASE 751E–04
ISSUE E

NOTES

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