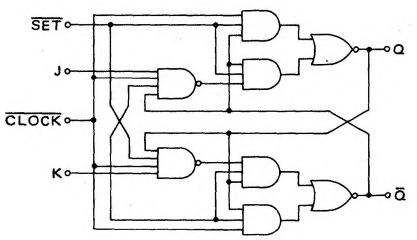
DUAL J-K FLIP-FLOP

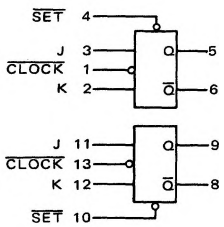
MC3162F • MC3062F
MC3162L • MC3062L,P

This dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct $\overline{SET}$ input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between the Set up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the $\overline{SET}$ input.

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN





Input Loading Factors:
$\overline{CLOCK}$, $\overline{SET}$ = 1.75
J, K, = 0.75

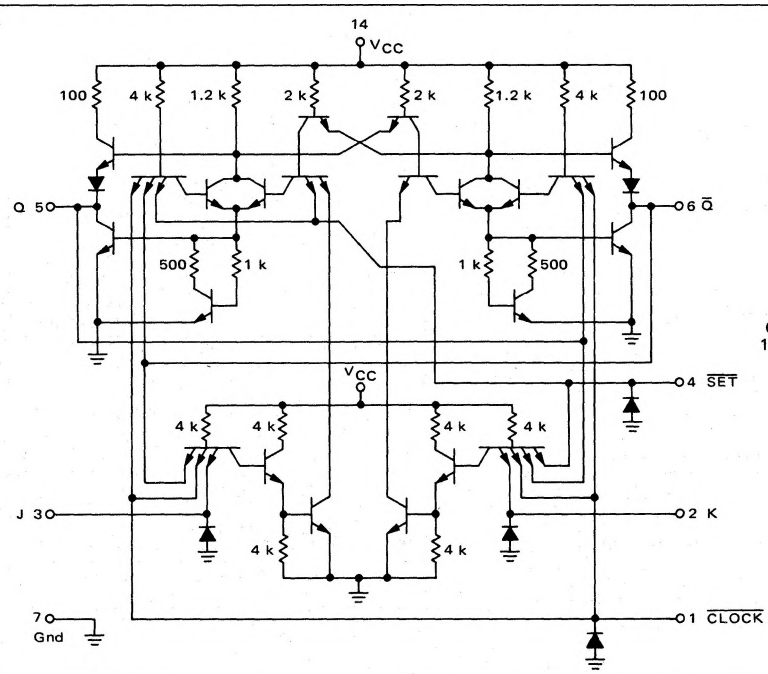
Output Loading Factor = 10

J-K TRUTH TABLE

J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Typical Characteristics:
(V_{CC} = 5.0 V; T_A = 25°C)

Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz typ
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
t_{pd+} = 12 ns
t_{pd-} = 12 ns

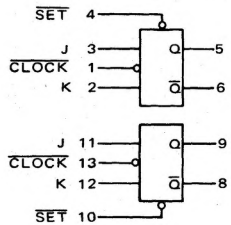


CIRCUIT SCHEMATIC
1/2 OF DEVICE SHOWN

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES										
		mA				Volts						
		I_{OL}	I_{OH}	I_{in}	I_D	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}
MC3162	−55°C	20	-2.0	-	-	0.4	2.4	4.0	-	4.5	5.5
	+25°C	20	-2.0	1.0	-10	0.4	2.4	4.0	7.0	4.5	5.5
	+125°C	20	-2.0	-	-	0.4	2.4	4.0	-	4.5	5.5
MC3062	0°C	20	-2.0	-	-	0.4	2.5	4.0	-	4.75	5.25
	+25°C	20	-2.0	1.0	-10	0.4	2.5	4.0	7.0	4.75	5.25
	+75°C	20	-2.0	-	-	0.4	2.5	4.0	-	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC3162 Test Limits −55°C Min	MC3162 Test Limits −55°C Max	MC3162 Test Limits +25°C Min	MC3162 Test Limits +25°C Max	MC3162 Test Limits +125°C Min	MC3162 Test Limits +125°C Max	MC3062 Test Limits 0°C Min	MC3062 Test Limits 0°C Max	MC3062 Test Limits +25°C Min	MC3062 Test Limits +25°C Max	MC3062 Test Limits +75°C Min	MC3062 Test Limits +75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}	P_1*	Gnd
Input																											
Forward Current	I_F	2	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	2,6	-	1,4	-	-	14	-	3,7,13
		3	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	3,5	-	1,4	-	-	14	-	2,7,13
	$I_{F\overline{S}}$	4	-	-4.7	-	-4.7	-	-4.7	-	-4.7	-	-4.7	-	-4.7	mAdc	-	-	-	-	4,6	-	1,2	-	-	14	-	3,7,13
	$I_{F\overline{C}}$	1	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	1,6	-	2,3	-	-	14	4	7,13
		1	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	1,5	-	2,3,4	-	-	14	-	7,13
Leakage Current	I_R	2	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	2	3	-	-	14	-	1,4,7,13
		3	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	3	2	-	-	14	-	1,4,7,13
	$I_{R\overline{S}}$	4	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	4	3	-	-	14	-	1,2,7,13
	$I_{R\overline{C}}$	1	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	1	-	-	-	14	-	2,3,4,7,13
Breakdown Voltage	BV_{in}	2	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	-	14	-	1,4,7,13
		3	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	3	-	-	-	-	-	-	↓	-	1,4,7,13
		4	-	-		-	-	-	-	-		-	-	-		-	-	4	-	-	-	-	-	-		-	1,2,7,13
		1	-	-		-	-	-	-	-		-	-	-		-	-	1	-	-	-	-	-	-		-	2,3,4,7,13
Clamp Voltage	V_D	2	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	2	-	-	-	-	14	-	-	7,13
		3	-	-	-	↓	-	-	-	-	-	↓	-	-	↓	-	-	-	3	-	-	-	-	↓	-	-	↓
		4	-	-	-		-	-	-	-	-		-	-		-	-	-	4	-	-	-	-		-	-	
		1	-	-	-		-	-	-	-	-		-	-		-	-	-	1	-	-	-	-		-	-	
Output																											
Output Voltage	V_{OL}	5	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	5	-	-	-	-	-	-	-	14	-	5	1,7,13
		6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	4	-	-	-	14	-	4	1,7,13
	V_{OH}	5	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	5	-	-	4	-	-	-	14	-	4	7
		6	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	-	4	-	14	-	5	1,7,13
Short-Circuit Current	I_{SC}	5	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	-	-	-	14	-	4,5,7,13
Power Requirements (Total Device)																											
Maximum Power Supply Current	I_{max}	14	-	-	-	41	-	-	-	-	-	41	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	4,7,10
Power Supply Drain	I_{PD}	14	-	31	-	31	-	31	-	31	-	31	-	31	mAdc	-	-	-	-	-	-	-	-	-	14	-	4,7,10

* Momentarily ground pin prior to taking measurement. (If pin is also in another column the pin must be returned to that voltage or current for measurement.)

OPERATING CHARACTERISTICS

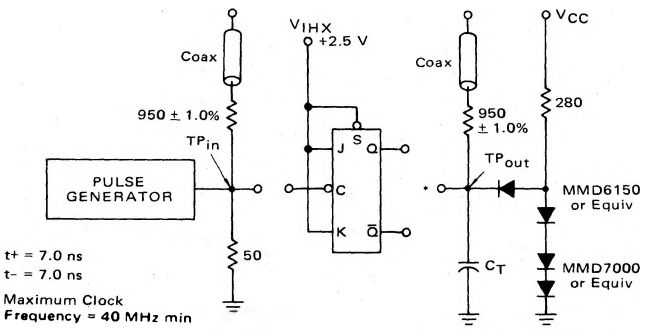
The data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The flip-flop is set to the Q = 1 state by applying a low level to the $\overline{SET}$ input. The direct $\overline{SET}$ inputs may be used at any time without regard to the clock state. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering – The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



t+ = 7.0 ns
t- = 7.0 ns

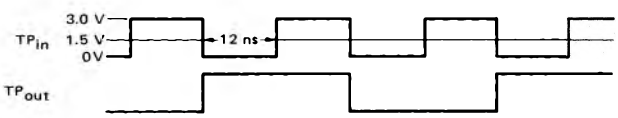
Maximum Clock Frequency = 40 MHz min

*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

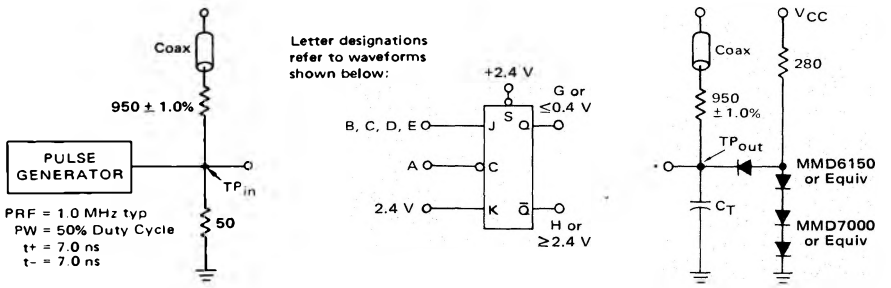
VOLTAGE WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs; to test other inputs, refer to Test Procedures Chart)



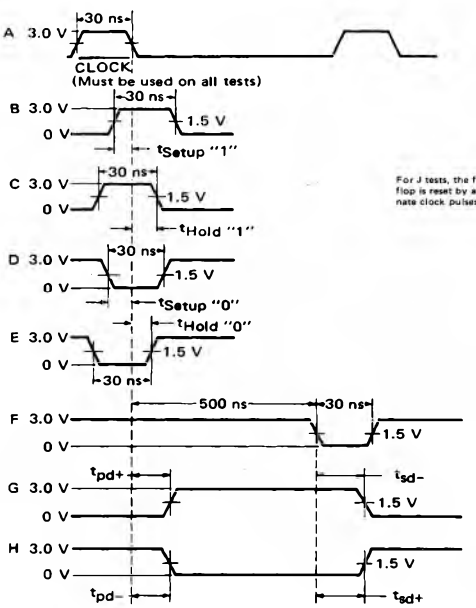
Three pulse generators are required and must be slaved together to provide the waveforms shown.

*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS AND DEFINITIONS



For J tests, the flip-flop is reset by alternate clock pulses

TEST PROCEDURES CHART

TEST	INPUT J*	INPUT $\overline{SET}$*	INPUT K*	INPUT Q*	INPUT $\overline{Q}$*	LIMITS (ns) Max
t_{Setup} "1" J	B	2.4 V	2.4 V	G	H	15
t_{Hold} "1" J	C	2.4 V	2.4 V	G	H	0**
t_{Setup} "0" J	D	2.4 V	2.4 V	≤0.4 V	≥2.4 V	15
t_{Hold} "0" J	E	2.4 V	2.4 V	≤0.4 V	≥2.4 V	0**
t_{Setup} "1" K	Gnd	F	B	H	G	15
t_{Hold} "1" K	Gnd	F	C	H	G	0**
t_{Setup} "0" K	Gnd	F	D	≥2.4 V	≤0.4 V	15
t_{Hold} "0" K	Gnd	F	E	≥2.4 V	≤0.4 V	0**
t_{pd+}	Delay from $\overline{CLOCK}$ to Q during t_{Setup} "1" J test. Delay from $\overline{CLOCK}$ to $\overline{Q}$ during t_{Setup} "1" K test.					18
t_{pd-}	Delay from $\overline{CLOCK}$ to $\overline{Q}$ during t_{Setup} "1" J test. Delay from $\overline{CLOCK}$ to Q during t_{Setup} "1" K test.					18
t_{sd+}	Delay from $\overline{SET}$ to Q during t_{Setup} "1" K test.					18
t_{sd-}	Delay from $\overline{SET}$ to $\overline{Q}$ during t_{Setup} "1" K test.					18

*Letters shown in test columns refer to waveforms shown at the left.

**t_{Hold} is typically a negative number.