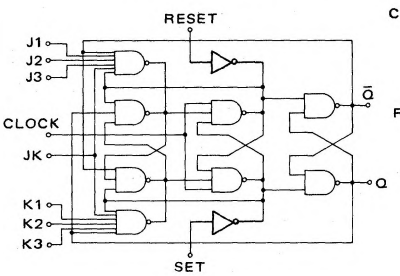
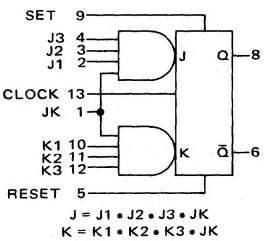
MC3150F • MC3050F
MC3150L • MC3050L,P

This J-K flip-flop triggers on the positive edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct SET and RESET are provided to permit presetting data, such as initial conditions into the flip-flop. The direct SET and RESET fully override the clock; i.e., the direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set up and Hold times. The inputs are inhibited when the clock is high; data is entered into the input steering section of the flip-flop when the clock goes low. The input steering section of the flip-flop continually reflects the input state when the clock is low. Data present during the time interval between the Set up and Hold times is transferred to the bistable section on the positive edge of the clock and the outputs Q and $\bar{Q}$ respond accordingly. The flip-flop can be set or reset directly by applying the high state to the SET or RESET inputs.

LOGIC DIAGRAM





J = J1 • J2 • J3 • JK
K = K1 • K2 • K3 • JK

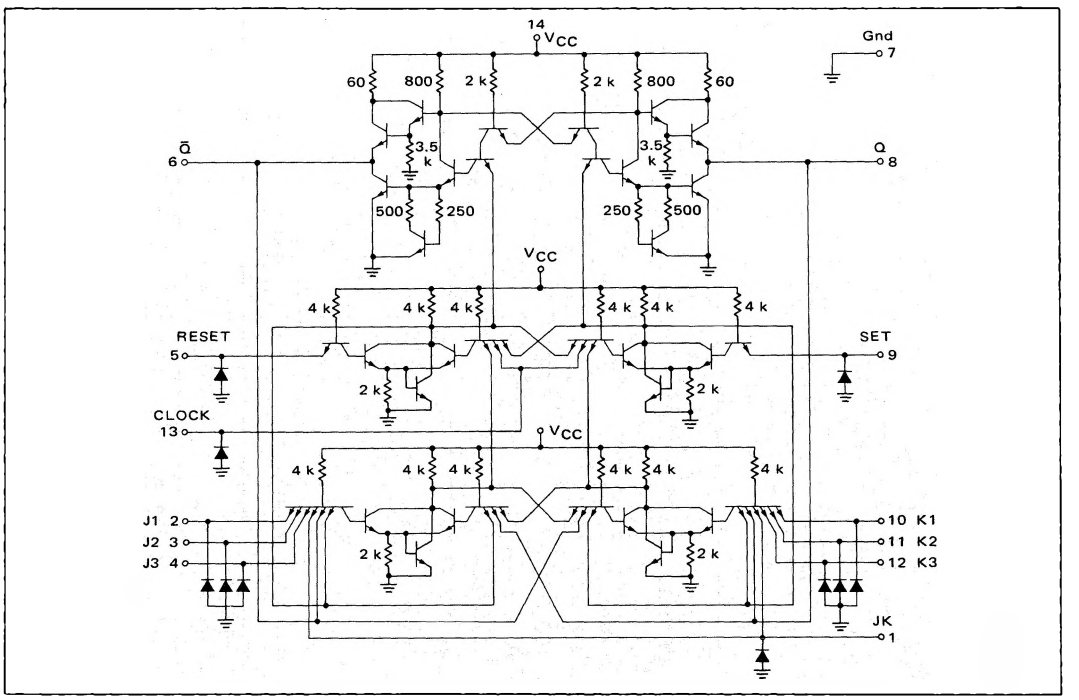
TRUTH TABLE

J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Input Loading Factors:
J, K, SET, RESET = 0.75
CLOCK, JK = 1.5

Output Loading Factor = 10

Typical Characteristics (V_{CC} = 5.0 V, T_A = 25°C)
Total Power Dissipation = 80 mW/pkg
Toggle Frequency = 40 MHz
Logical "1" Setup Time = 10 ns
Logical "0" Setup Time = 5.0 ns
Logical "1" and "0" Hold Time = 5.0 ns
t_{pd-} = 12 ns
t_{pd+} = 14 ns



See General Information section for packaging.

FIGURE 1 – I_{EX} TEST CIRCUIT

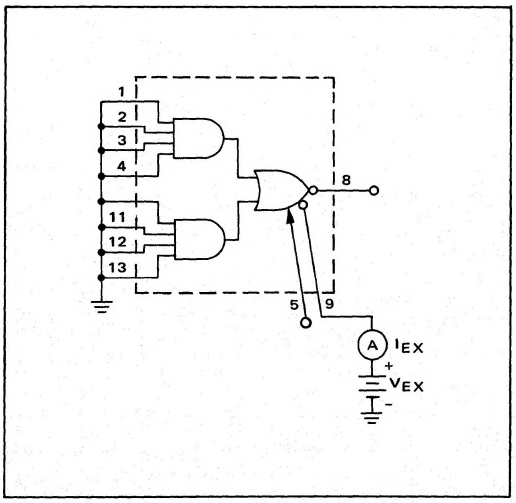


FIGURE 2 – V_{BE} TEST CIRCUIT

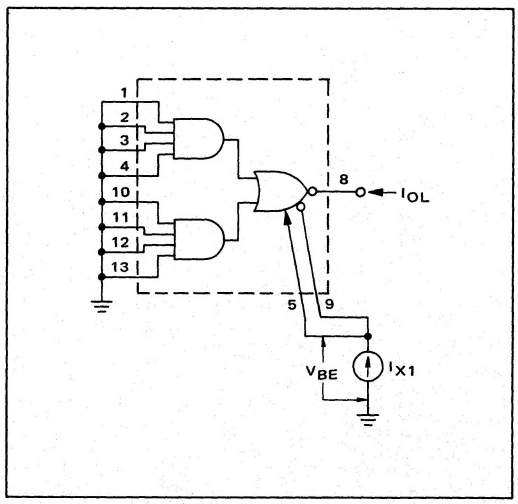
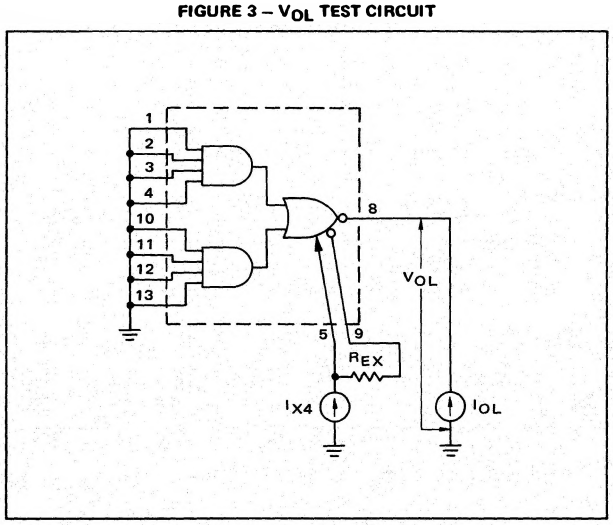
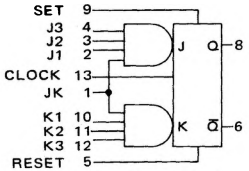


FIGURE 3 – V_{OL} TEST CIRCUIT



ELECTRICAL CHARACTERISTICS



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}
MC3150	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	4.5	5.5
	+25°C	20	-2.0	1.0	10	1.1	1.8	0.4	2.4	4.0	7.0	4.5	5.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	4.5	5.5
MC3050	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	4.75	5.25
	+25°C	20	-2.0	1.0	10	1.1	1.8	0.4	2.5	4.0	7.0	4.75	5.25
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC3150 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3050 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}	Gnd
Input																												
Forward Current	I_{FJ}	2	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	2	-	1,3,4,5	-	-	14	7,9,13
		3	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	3	-	1,2,4,5	-	-	↓	↓
		4	-		-		-		-		-		-			-	-	-	-	-	-	4	-	1,2,3,5	-	-		
	I_{FK}	10	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	10	-	1,9,11,12	-	-	14	5,7,13
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	11	-	1,9,10,12	-	-	↓	↓
		12	-		-		-		-		-		-			-	-	-	-	-	-	12	-	1,9,10,11	-	-		
	I_{FC}	13	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	13	-	-	-	-	14	1,5,7,9
	I_{FJK}	1	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	1	-	2,3,4,10,11,12	-	-	14	5,7,9,13
	I_{FS}	9	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	9	-	5	-	-	14	7
	I_{FR}	5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	5	-	9	-	-	14	7
Leakage Current	I_{RJ}	2	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	2	9	-	-	14	1,3,4,5,7
		3	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	3		-	-	↓	1,2,4,5,7
		4	-		-		-		-		-		-			-	-	-	-	-	-	-	4		-	-		1,2,3,5,7
	I_{RK}	10	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	10	5	-	-	14	1,7,9,11,12
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	11	↓	-	-	↓	1,7,9,10,12
		12	-		-		-		-		-		-			-	-	-	-	-	-	-	12		-	-		1,7,9,10,11
	I_{RC}	13	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	-	13	1,2,3,4,5,10,11,12	-	-	14	7,9
	I_{RJK}	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	9	-	-	14	2,3,4,5,7,10,11,12
	I_{RS}	9	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	9	-	-	-	14	7
	I_{RR}	5	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	5	-	-	-	14	7
Breakdown Voltage	BV_{in}	2	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	9	-	-	14	1,3,4,5,7
		3	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	3	-	-	-	-	-	↓	-	-		1,2,4,5,7
		4	-	-		-	-	-	-	-		-	-	-		-	-	4	-	-	-	-	-		-	-		1,2,3,5,7
		10	-	-		-	-	-	-	-		-	-	-		-	-	10	-	-	-	-	-	5	-	-		1,7,9,11,12
		11	-	-		-	-	-	-	-		-	-	-		-	-	11	-	-	-	-	-	↓	-	-		1,7,9,10,12
		12	-	-		-	-	-	-	-		-	-	-		-	-	12	-	-	-	-	-		-	-		1,7,9,10,11
		13	-	-		-	-	-	-	-		-	-	-		-	-	13	-	-	-	-	-	1,2,3,4,5,10,11,12	-	-		7,9
		1	-	-		-	-	-	-	-		-	-	-		-	-	1	-	-	-	-	-	9	-	-		2,3,4,5,7,10,11,12
		9	-	-		-	-	-	-	-		-	-	-		-	-	9	-	-	-	-	-	-	-	-		7
		5	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	5	-	-	-	-	-	-	-	-	↓	7
Clamp Voltage	V_D	2	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	2	-	-	-	-	-	-	14	-	7
		3	-	-	-	↓	-	-	-	-	-	↓	-	-	↓	-	-	-	3	-	-	-	-	-	-	↓	-	↓
		4	-	-	-		-	-	-	-	-		-	-		-	-	-	4	-	-	-	-	-	-		-	
		10	-	-	-		-	-	-	-	-		-	-		-	-	-	10	-	-	-	-	-	-		-	
		11	-	-	-		-	-	-	-	-		-	-		-	-	-	11	-	-	-	-	-	-		-	
		12	-	-	-		-	-	-	-	-		-	-		-	-	-	12	-	-	-	-	-	-		-	
		13	-	-	-		-	-	-	-	-		-	-		-	-	-	13	-	-	-	-	-	-		-	
		1	-	-	-		-	-	-	-	-		-	-		-	-	-	1	-	-	-	-	-	-		-	
		9	-	-	-		-	-	-	-	-		-	-		-	-	-	9	-	-	-	-	-	-		-	
		5	-	-	-	↓	-	-	-	-	-	↓	-	-	↓	-	-	-	5	-	-	-	-	-	-	↓	-	↓
Output																												
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	5	9	-	-	-	-	-	14	7,13
		8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	9	5	-	-	-	-	-	14	7,13
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	9	5	-	-	-	-	14	-	7,13
		8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	5	9	-	-	-	-	14	-	7,13
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	5	-	-	14	6,7,9
		8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	9	-	-	14	5,7,8
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	35	-	-	-	-	-	35	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	1,5,7,13
Power Supply Drain	I_{PD}	14	-	27.6	-	27.6	-	27.6	-	27.6	-	27.6	-	27.6	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,5,7,13

OPERATING CHARACTERISTICS

High state data must be present 17 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

Positive edge triggering: When the clock goes from the low state to the high state, the information in the input steering section is transferred to the bistable section.

The direct SET and RESET inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED TO GROUND.

Unused Inputs:

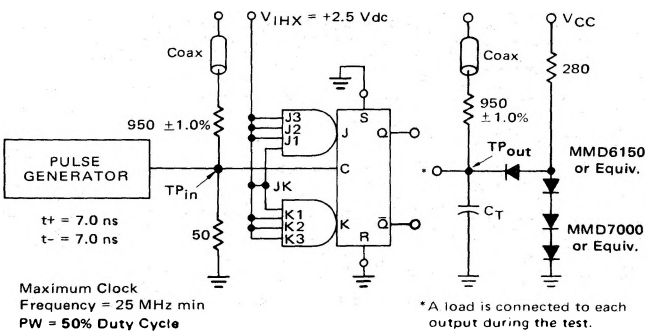
JK input MUST be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and 5.5 Vdc.

Unused J inputs should be tied to used J inputs, the used JK input, $\overline{Q}$, or a voltage between 2.0 and 5.5 Vdc.

Unused K inputs should be tied to used K inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.

Unused SET and RESET inputs MUST be tied to ground.

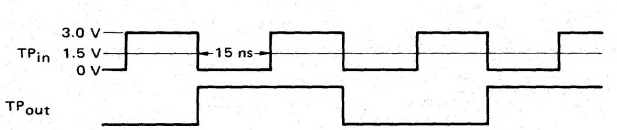
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

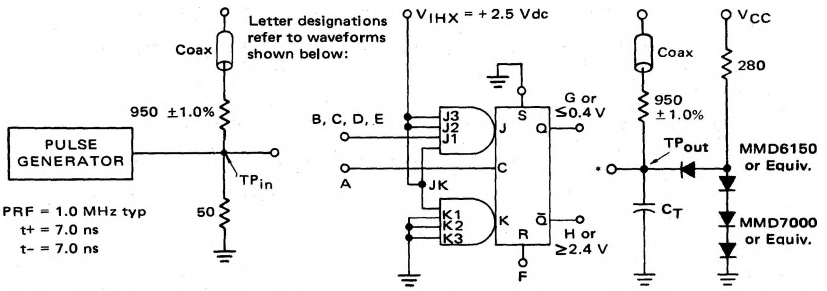
WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)



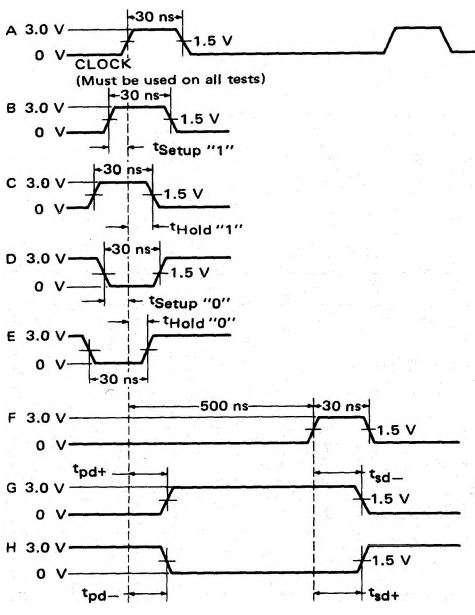
Three pulse generators are required and must be slaved together to provide the waveforms shown.

*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT J**	SET**	RESET**	K**	Q*	Q̄*	LIMITS (ns) Min	Max
t_{Setup} "1" J	B	Gnd	F	Gnd	G	H	-	17
t_{Hold} "1" J	C	Gnd	F	Gnd	G	H	-	01
t_{Setup} "0" J	D	Gnd	F	Gnd	≤0.4 V	≥2.4 V	-	5.0
t_{Hold} "0" J	E	Gnd	F	Gnd	≤0.4 V	≥2.4 V	-	01
t_{Setup} "1" K	Gnd	F	Gnd	B	H	G	-	17
t_{Hold} "1" K	Gnd	F	Gnd	C	H	G	-	01
t_{Setup} "0" K	Gnd	F	Gnd	D	≥2.4 V	≤0.4 V	-	5.0
t_{Hold} "0" K	Gnd	F	Gnd	E	≥2.4 V	≤0.4 V	-	01
t_{pd+}	Delay from clock to Q during t_{Setup} "1" J test. Delay from clock to Q̄ during t_{Setup} "1" K test.						8.0	30
t_{pd-}	Delay from clock to Q̄ during t_{Setup} "1" J test. Delay from clock to Q during t_{Setup} "1" K test.						8.0	30
t_{sd+}	Delay from SET to Q during t_{Setup} "1" K test. Delay from RESET to Q̄ during t_{Setup} "1" J test.						7.0	23
t_{sd-}	Delay from SET to Q̄ during t_{Setup} "1" K test. Delay from RESET to Q during t_{Setup} "1" J test.						7.0	23

** Letters shown in these columns refer to waveforms at the left.

†† t_{Hold} is typically a negative number.