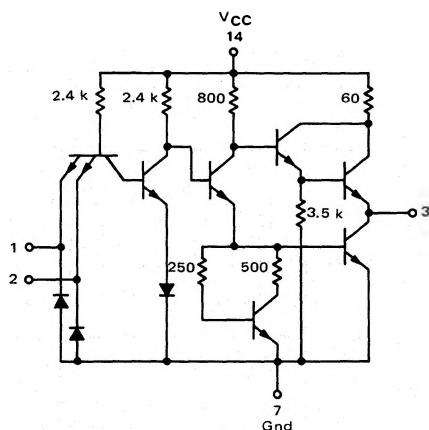


QUAD 2-INPUT "AND" GATE

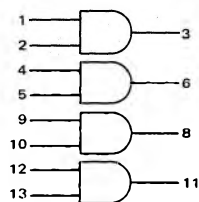
MC3100/MC3000 series

MC3101F • MC3001F
MC3101L • MC3001L,P
 (54H08J) (74H08J,N)

CIRCUIT SCHEMATIC
 1/4 OF CIRCUIT SHOWN



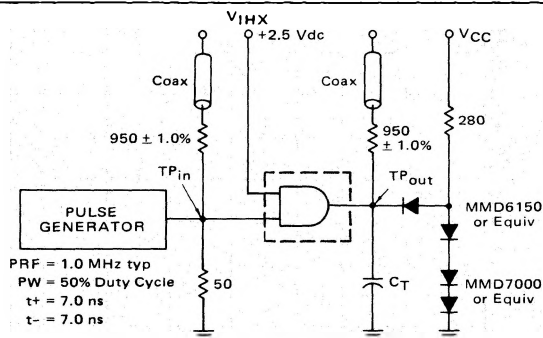
This device consists of four 2-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.



Positive Logic: $3 = 1 \cdot 2$
 Negative Logic: $3 = 1 + 2$

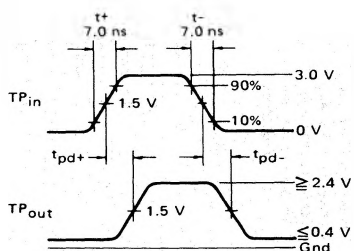
Input Loading Factor = 1
 Output Loading Factor = 10
 Total Power Dissipation = 112 mW typ/pkg
 Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

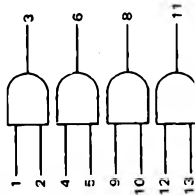
The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



MC3101, MC3001 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic		Pin Under Test	MC3101 Test Limits						MC3001 Test Limits						TEST CURRENT / VOLTAGE VALUES																					
			-55°C			+25°C			+125°C			0°C			+25°C			+75°C			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															
			Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit																			
Input																																				
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc																			
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	-	50	μ Adc																			
Breakdown Voltage	BV_{in}	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Vdc																			
Clamp Voltage	V_D	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Vdc																			
Output																																				
Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc																			
	V_{OH}	3	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	2.5	-	Vdc																			
Short-Circuit Current	I_{SC}	3	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc																			
Power Requirements (Total Device)																																				
Maximum Power Supply Current	I_{max}	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	mAdc																			
Power Supply Drain	I_{PDH}	14	-	24	-	24	-	24	-	24	-	24	-	24	-	24	mAdc																			
	I_{PDL}	14	-	48	-	48	-	48	-	48	-	48	-	48	-	48	mAdc																			
Switching Parameters																																				
Turn-On Delay	t_{pd}	1,3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ns																			
Turn-Off Delay	t_{pd}	1,3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ns																			

③ Test Temperature

Volts

mA

I_{OL}	I_{OH}	I_{in}	I_{D}	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCN}	V_{IHx}
20	-2.0	-	-	-1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:

I_{OL}	I_{OH}	I_{in}	I_{D}	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCN}	V_{IHx}
-	-	-	-	-	-	1	-	2*	-	-	14	-	-
-	-	-	-	-	-	-	1	*	-	-	-	14	-
-	-	1	-	-	-	-	-	*	-	-	-	14	-
-	-	-	1	-	-	-	-	*	-	-	14	-	-
-	-	-	-	1	-	-	-	2*	-	-	-	-	-
-	-	-	-	-	1	-	-	2*	-	-	14	-	-
-	-	-	-	-	-	-	-	1,2*	-	-	-	14	-
-	-	-	-	-	-	-	-	1,2,4,5,9,10,12,13	14	-	-	-	-
-	-	-	-	-	-	-	-	1,2,4,5,9,10,12,13	-	-	-	14	-
-	-	-	-	-	-	-	-	-	-	-	-	14	-
-	-	-	-	-	-	-	-	-	-	-	-	-	1,2,4,5,7,9,10,12,13
-	-	-	-	-	-	-	-	*	-	14	-	-	2
-	-	-	-	-	-	-	-	*	-	14	-	-	2

*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{IH} .