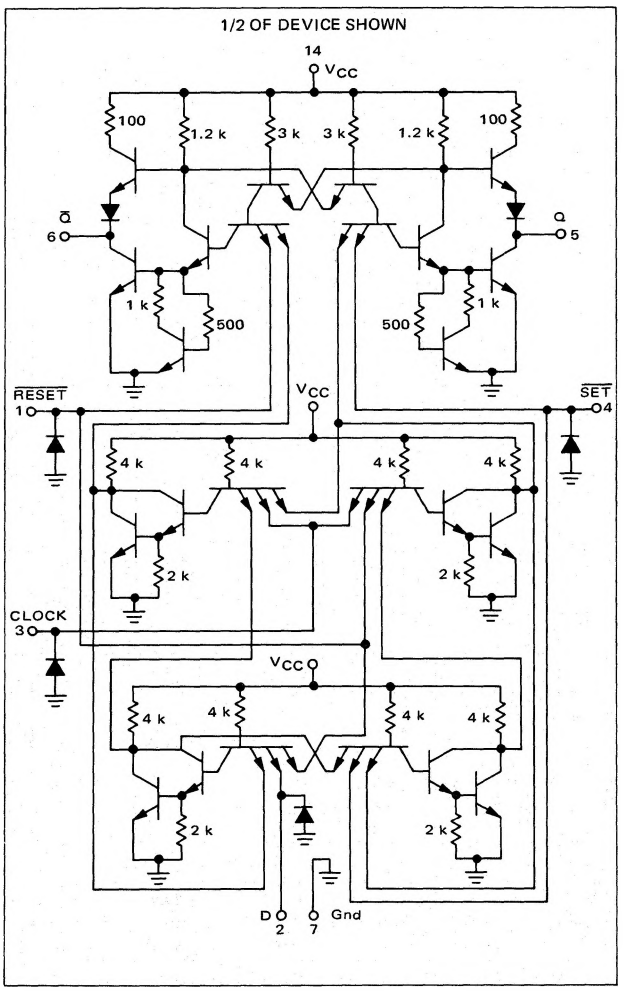
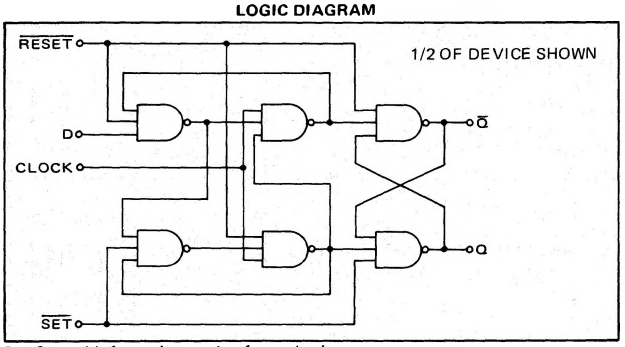
MC3160F • MC3060F
MC3160L • MC3060L,P



LOGIC DIAGRAM

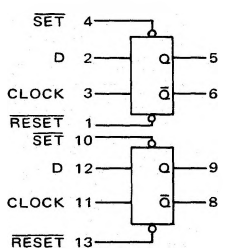


See General Information section for packaging

This dual flip-flop triggers on the positive edge of the clock and performs the Type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct $\overline{SET}$ and $\overline{RESET}$ inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the Setup and Hold times. The clocked inputs are inhibited when the clock is high and data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Setup and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Q and $\bar{Q}$ respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs.



TRUTH TABLE

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$Q^{n+1} = D^n$

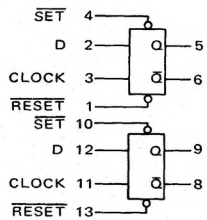
Input Loading Factors:
- $\overline{SET}$ = 1.15
- $\overline{RESET}$ = 1.7
- CLOCK= 1.5
- D = 0.75

Output Loading Factor = 10

Typical Characteristics: (V_{CC} = 5.0 V, T_A = 25°C)
- Total Power Dissipation = 120 mW/pkg
- Toggle Frequency = 30 MHz
- Logical "1" Setup Time = 10 ns
- Logical "0" Setup Time = 5.0 ns
- Logical "1" and "0" Hold Times = 5.0 ns
- t_{pd-} = 17 ns
- t_{pd+} = 15 ns

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}
MC3160	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	4.5	5.5
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	4.5	5.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	4.5	5.5
MC3060	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	4.75	5.75
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	4.75	5.75
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	4.75	5.75

Characteristic	Symbol	Pin Under Test	MC3160 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3060 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}	P_1*	Gnd
Input																													
Forward Current	I_{FC}	3	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	3	-	1	-	-	14	-	2,4,7,11
	$I_{F\bar{D}}$	2	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	2	-	1,4	-	-	14	-	3,7,11
	$I_{F\bar{S}}$	4	-	-2.3	-	-2.3	-	-2.3	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	4	-	1	-	-	14	-	2,3,7,11
	$I_{F\bar{R}}$	1	-	-3.4	-	-3.4	-	-3.4	-	-3.4	-	-3.4	-	-3.4	mAdc	-	-	-	-	-	-	1	-	2,4	-	-	14	-	3,7,11
Leakage Current	I_{RC}	3	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	3	4	-	-	14	-	1,2,7,11
	I_{RD}	2	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	2	3,4	-	-	14	-	1,7,11
	$I_{R\bar{S}}$	4	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	4	1,2	-	-	14	3	7,11
	$I_{R\bar{R}}$	1	-	140	-	140	-	140	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	1	4	-	-	14	3	2,7,11
Breakdown Voltage	BV_{in}	3	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	3	-	-	-	-	-	4	-	-	14	-	1,2,7,11
		2	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	2	-	-	-	-	-	3,4	-	-	↓	-	1,7,11
		4	-	-		-	-	-	-	-		-	-	-		-	-	4	-	-	-	-	-	1,2	-	-		3	7,11
		1	-	-		-	-	-	-	-		-	-	-		-	-	1	-	-	-	-	-	4	-	-		3	2,7,11
Clamp Voltage	V_D	3	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	3	-	-	-	-	-	-	14	-	-	7,11
		2	-	-	-	↓	-	-	-	-	-	↓	-	-	↓	-	-	-	2	-	-	-	-	-	-	↓	-	-	↓
		4	-	-	-		-	-	-	-	-		-	-		-	-	-	4	-	-	-	-	-	-		-	-	
		1	-	-	-		-	-	-	-	-		-	-		-	-	-	1	-	-	-	-	-	-		-	-	
Output																													
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	4	1	-	-	-	-	14	-	-	2,3,7,11
		5	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	5	-	-	-	1	4	-	-	-	-	14	-	-	2,3,7,11
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	1	4	-	-	-	-	14	-	-	2,3,7,11
		5	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	5	-	-	4	1	-	-	-	-	14	-	-	2,3,7,11
Short-Circuit Current	I_{SC}	6	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	4	1	-	-	-	-	14	-	6,7,11
		5	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	1	4	-	-	-	-	14	-	5,7,11
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	42	-	-	-	-	-	42	-	-	mAdc	-	-	-	-	-	-	-	-	1,13	14	-	-	-	3,4,7,10,11
Power Supply Drain	I_{PD}	14	-	31	-	31	-	31	-	31	-	31	-	31	mAdc	-	-	-	-	-	-	-	-	4,10	-	-	14	-	1,3,7,11,13

* Pulse is used to set flip-flop in desired state. P_1 = 4.0 V (V_{RH}), 0 V. If pin is also in another column, the pin must be returned to that voltage or current for measurement.

OPERATING CHARACTERISTICS

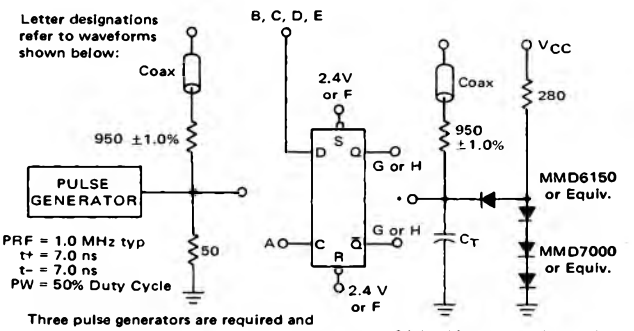
Data must be present 15 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

The direct $\overline{SET}$ and $\overline{RESET}$ inputs may be used at any time as they completely override the clock.

Positive edge triggering: When the clock goes from the low to the high state, the information in the input steering section is transferred to the bistable section.

Unused inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

SWITCHING TIME TEST CIRCUIT



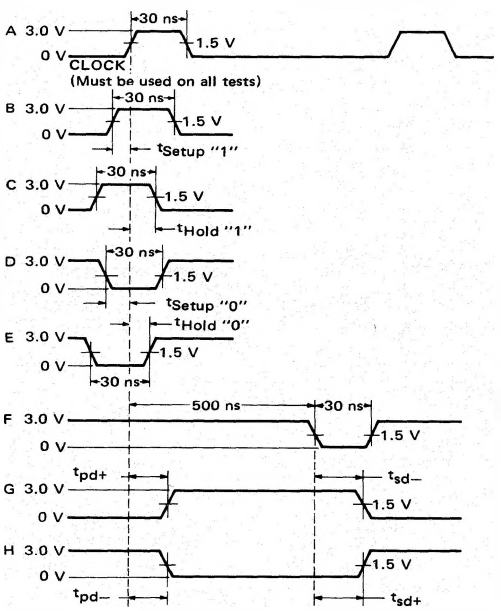
Three pulse generators are required and must be slaved together to provide the waveforms shown.

*A load is connected to each output during the test.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT D*	INPUT $\overline{SET}$*	INPUT $\overline{RESET}$*	Q*	$\overline{Q}$*	LIMITS (ns) Min	LIMITS (ns) Max
t_{Setup} "1" D	B	2.4 V	F	G	H	–	15
t_{Hold} "1" D	C	2.4 V	F	G	H	–	5.0
t_{Setup} "0" D	D	F	2.4 V	H	G	–	15
t_{Hold} "0" D	E	F	2.4 V	H	G	–	5.0
t_{pd+}	Delay from clock to Q during t_{Setup} "1" D test. Delay from clock to $\overline{Q}$ during t_{Setup} "0" D test.					10	25
t_{pd-}	Delay from clock to Q during t_{Setup} "0" D test. Delay from clock to $\overline{Q}$ during t_{Setup} "1" D test.					10	25
t_{sd+}	Delay from $\overline{SET}$ to Q during t_{Setup} "0" D test. Delay from $\overline{RESET}$ to $\overline{Q}$ during t_{Setup} "1" D test.					5.0	20
t_{sd-}	Delay from $\overline{SET}$ to $\overline{Q}$ during t_{Setup} "0" D test. Delay from $\overline{RESET}$ to Q during t_{Setup} "1" D test.					5.0	20

*Letters shown in these columns refer to waveforms at left.