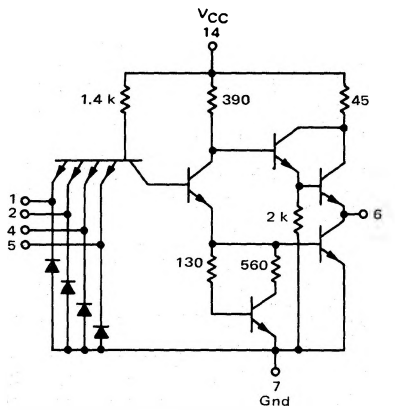
DUAL 4-INPUT "NAND" BUFFER GATE

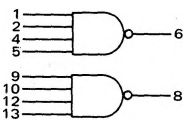
MC3124F • MC3024F
MC3124L • MC3024L,P

(54H40J) (74H40J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (30).



Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

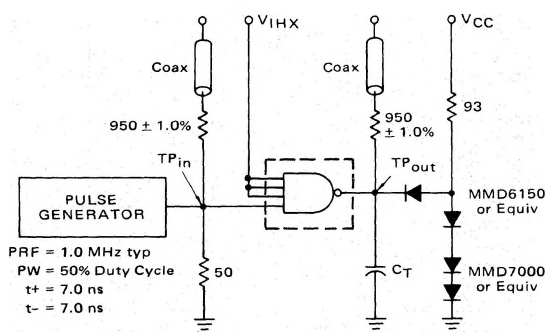
Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

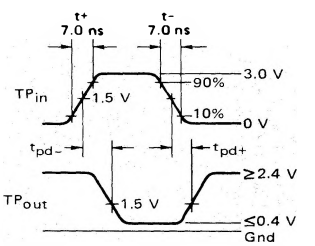
Input Loading Factor = 2
Output Loading Factor = 30
Total Power Dissipation = 90 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

Pin numbers for the 54H40F/74H40F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3124F,L/3024F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H40F/74H40F	1	12	3	13	14	2	11	10	6	7	5	8	9	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





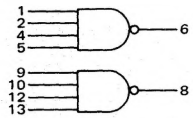
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
	mA				Volts									
	I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3124 −55°C	60	-1.5	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3124 +25°C	60	-1.5	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.4
MC3124 +125°C	60	-1.5	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3024 0°C	60	-1.5	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
MC3024 +25°C	60	-1.5	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
MC3024 +75°C	60	-1.5	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3124 Test Limits −55°C Min	MC3124 Test Limits −55°C Max	MC3124 Test Limits +25°C Min	MC3124 Test Limits +25°C Max	MC3124 Test Limits +125°C Min	MC3124 Test Limits +125°C Max	MC3024 Test Limits 0°C Min	MC3024 Test Limits 0°C Max	MC3024 Test Limits +25°C Min	MC3024 Test Limits +25°C Max	MC3024 Test Limits +75°C Min	MC3024 Test Limits +75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0	mAdc	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 4, 5, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	1.2,4,5	-	-	-	-	-	14	-	-	7*
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	1	-	-	-	2, 4, 5	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-	-	-40	-135	-	-	-	-	-40	-125	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,4,5,6,7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	22	-	-	-	-	-	22	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	40	-	40	-	40	-	40	-	40	-	40	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	16	-	16	-	16	-	16	-	16	-	16	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7 9, 10, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1,6	-	-	-	12	-	-	-	-	-	12	-	-	ns	Pulse In 1	Pulse Out 6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*
Turn-Off Delay	t_{pd+}	1,6	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.