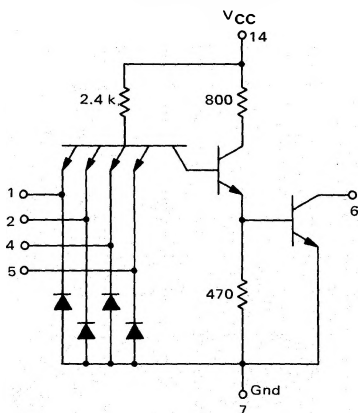


**DUAL 4-INPUT "NAND" GATE
(Open Collector)**

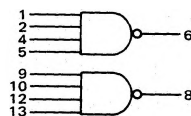
MC3100/MC3000 series

MC3112F • MC3012F
MC3112L • MC3012L,P
(54H22J) (74H22J,N)

**CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN**



This device consists of two 4-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR function is required or for driving discrete components.



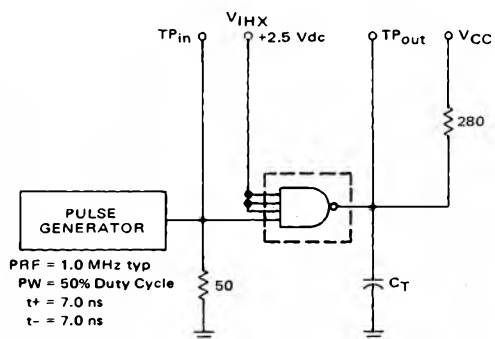
Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$
Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

Pin numbers for the 54H22F/74H22F device are shown in the chart. These devices are available on special request.

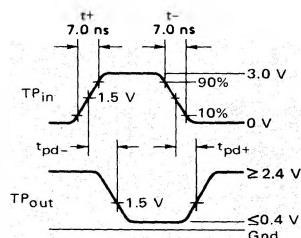
DEVICE	PIN NUMBERS													
MC3112F,L/3012F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H22F/74H22F	1	12	3	13	14	2	11	10	6	7	14	8	9	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PULSE GENERATOR
PRF = 1.0 MHz typ
PW = 50% Duty Cycle
 $t^+ = 7.0$ ns
 $t^- = 7.0$ ns

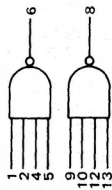
$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic		Pin Under Test	MC3112 Test Limits						MC3012 Test Limits						TEST CURRENT / VOLTAGE VALUES																					
			-55°C			+25°C			+125°C			0°C			+25°C			+75°C			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW :															
			Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit																			
Input		Symbol																Volts																		
			I _{OL}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{BH}	V _{CEX}	V _{max}	V _{CC}	V _{CCL}	V _{CH}	V _{HH}																				
			20	-	-	1.1	2.0	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-																				
			20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	2.5																				
			20	-	-	0.8	1.8	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-																				
			20	-	-	1.1	2.0	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-																				
			20	1.0	-10	1.1	1.8	0.4	2.5	4.0	5.5	7.0	5.0	4.75	5.25	2.5																				
			20	-	-	0.9	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-																				
			I _{OL}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{BH}	V _{CEX}	V _{max}	V _{CC}	V _{CCL}	V _{CH}	V _{HH}																				
			7*	-	-	1	-	-	2, 4, 5	-	-	-	14	-	-	-																				
			2, 4, 5, 7*	-	-	1	-	-	-	-	-	-	-	-	14	-																				
			2, 4, 5, 7*	-	-	-	-	-	-	-	-	-	-	-	-	-																				
			7	-	-	1	-	-	-	-	-	-	-	14	-	-																				
			7*	-	-	1	-	-	2, 4, 5	-	-	-	-	14	-	-																				
			7*	-	-	1	2, 4, 5	-	-	-	6	-	-	14	-	-																				
			1, 2, 4, 5, 7, 9, 10, 12, 13	-	-	-	-	-	-	-	-	-	14	-	-	-																				
			7	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	-	-	14	-																				
			1, 2, 4, 5, 7, 9, 10, 12, 13	-	-	-	-	-	-	-	-	-	-	-	-	-																				
Switching Parameters			Pulse In	Pulse Out																																
			1	6																																
			ns	ns																																
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*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.