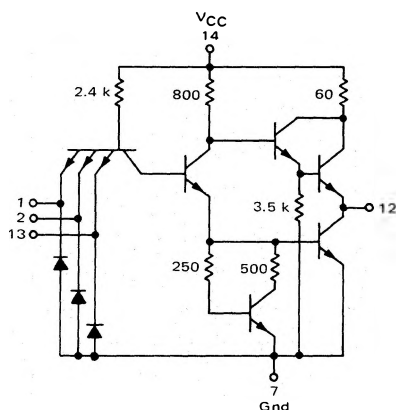


TRIPLE
3-INPUT "NAND" GATE

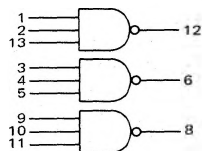
MC3100/MC3000 series

MC3105F • MC3005F
MC3105L • MC3005L,P
(54H10J) (74H10J,N)

CIRCUIT SCHEMATIC
1/3 OF CIRCUIT SHOWN



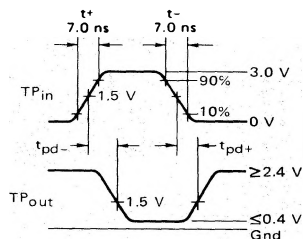
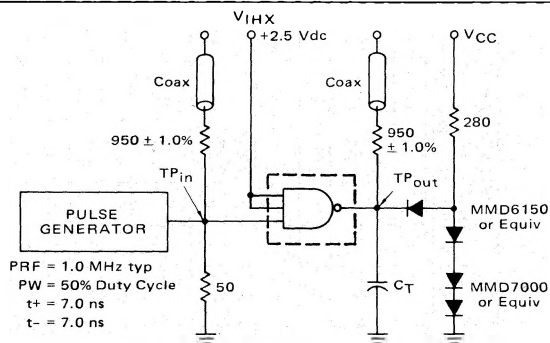
This package consists of three 3-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



Positive Logic: $12 = \overline{1 \cdot 2 \cdot 13}$
Negative Logic: $12 = \overline{1 + 2 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



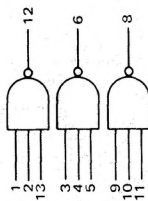
$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

MC3105, MC3005 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



										TEST CURRENT / VOLTAGE VALUES									
										Volts									
										mA									
										TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:									
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* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.