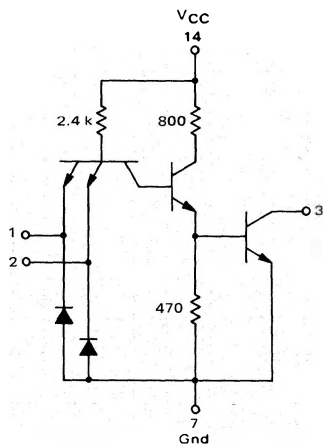


QUAD 2-INPUT "NAND" GATE
(Open Collector)

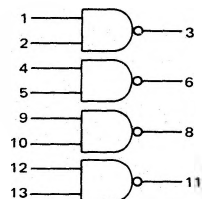
MC3100/MC3000 series

MC3104F • MC3004F
MC3104L • MC3004L,P
(54H01J) (74H01J,N)

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR-function is required or for driving discrete components.



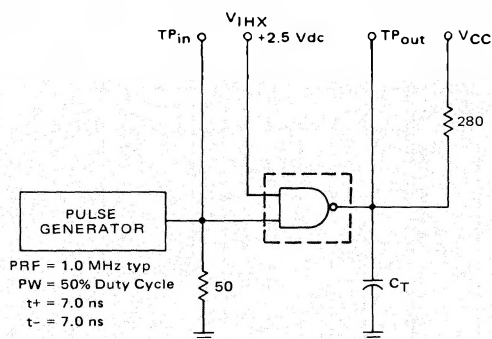
Positive Logic: $3 = \overline{1 \cdot 2}$
Negative Logic: $3 = \overline{1 + 2}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 88 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

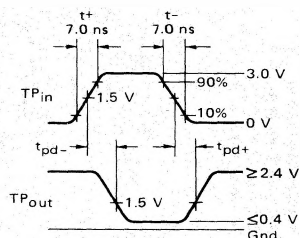
Pin numbers for the 54H01F/74H01F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3104F,L/3004F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H01F/74H01F	1	2	3	6	7	5	11	8	9	10	14	12	13	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PULSE GENERATOR
PRF = 1.0 MHz typ
PW = 50% Duty Cycle
 $t_+ = 7.0$ ns
 $t_- = 7.0$ ns

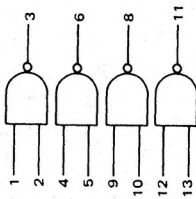


$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

MC3104, MC3004 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



		Pin Under Test		MC3104 Test Limits												MC3004 Test Limits												TEST CURRENT / VOLTAGE VALUES														Gnd																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																										
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* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.