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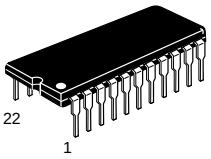
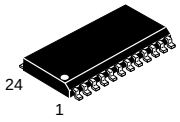
by MC145422/D

MC145422
MC145426

Universal Digital-Loop Transceivers (UDLT)



P SUFFIX
PLASTIC DIP
CASE 708



DW SUFFIX
SOG PACKAGE
CASE 751E

ORDERING INFORMATION

MC145422P	Plastic DIP
MC145426P	Plastic DIP
MC145422DW	SOG Package
MC145426DW	SOG Package

The MC145422 and MC145426 UDLTs are high–speed data transceivers that provide 80 kbps full–duplex data communication over 26 AWG and larger twisted–pair cable up to two kilometers in distance. Intended primarily for use in digital subscriber voice/data telephone systems, these devices can also be used in remote data acquisition and control systems. These devices utilize a 256 kilobaud modified differential phase shift keying burst modulation technique for transmission to minimize RFI/EMI and crosstalk. Simultaneous power distribution and duplex data communication can be obtained using a single twisted–pair wire.

These devices are designed for compatibility with existing, as well as evolving, telephone switching hardware and software architectures.

The UDLT chip–set consists of the MC145422 Master UDLT for use at the telephone switch linecard and the MC145426 Slave UDLT for use at the remote digital telset and/or data terminal.

The devices employ CMOS technology in order to take advantage of their reliable low–power operation and proven capability for complex analog/digital LSI functions.

- Provides Full–Duplex Synchronous 64 kpbs Voice/Data Channel and Two 8 kbps Signaling Data Channels Over One 26 AWG Wire Pair Up to Two Kilometers
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single 5 V Power Supply
- 22–Pin PDIP, 24–Pin SOG Packages
- Application Notes AN943, AN949, AN968, AN946, and AN948

MC145422 Master UDLT

- Pin Controlled Power–Down and Loopback Features
- Signaling and Control I/O Capable of Sharing Common Bus Wiring with Other UDLTs
- Variable Data Clock — 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 kbps Channel into LSB of 64 kbps Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145426 Slave UDLT

- Compatible with MC145500 Series PCM Codec–Filters
- Pin Controlled Loopback Feature
- Automatic Power–Up/Power–Down Feature
- On–Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

REV 2
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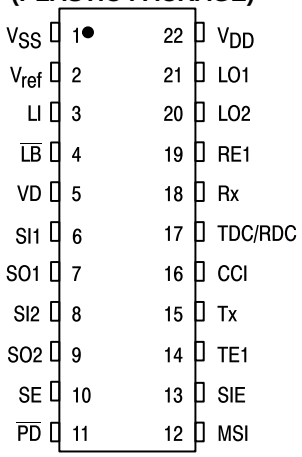
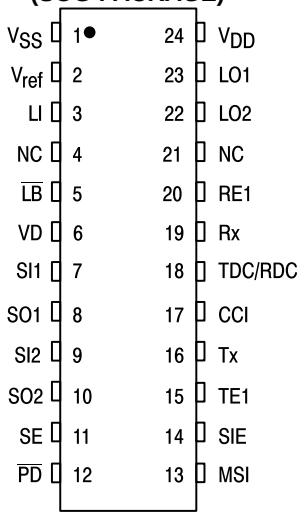
PIN ASSIGNMENTS

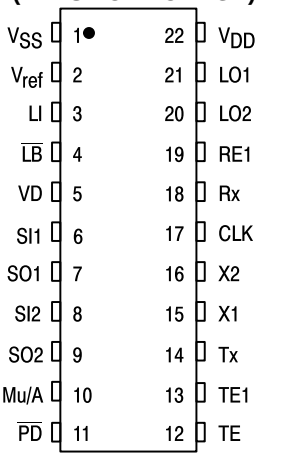
MC145422 — MASTER (PLASTIC PACKAGE)



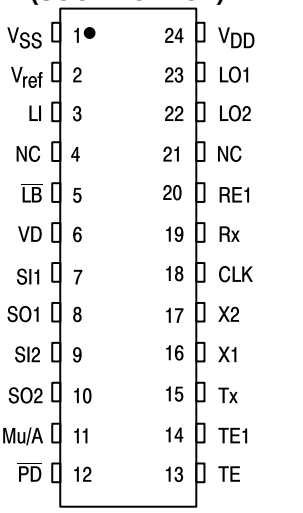
MC145422 — MASTER (SOG PACKAGE)



MC145426 — SLAVE (PLASTIC PACKAGE)

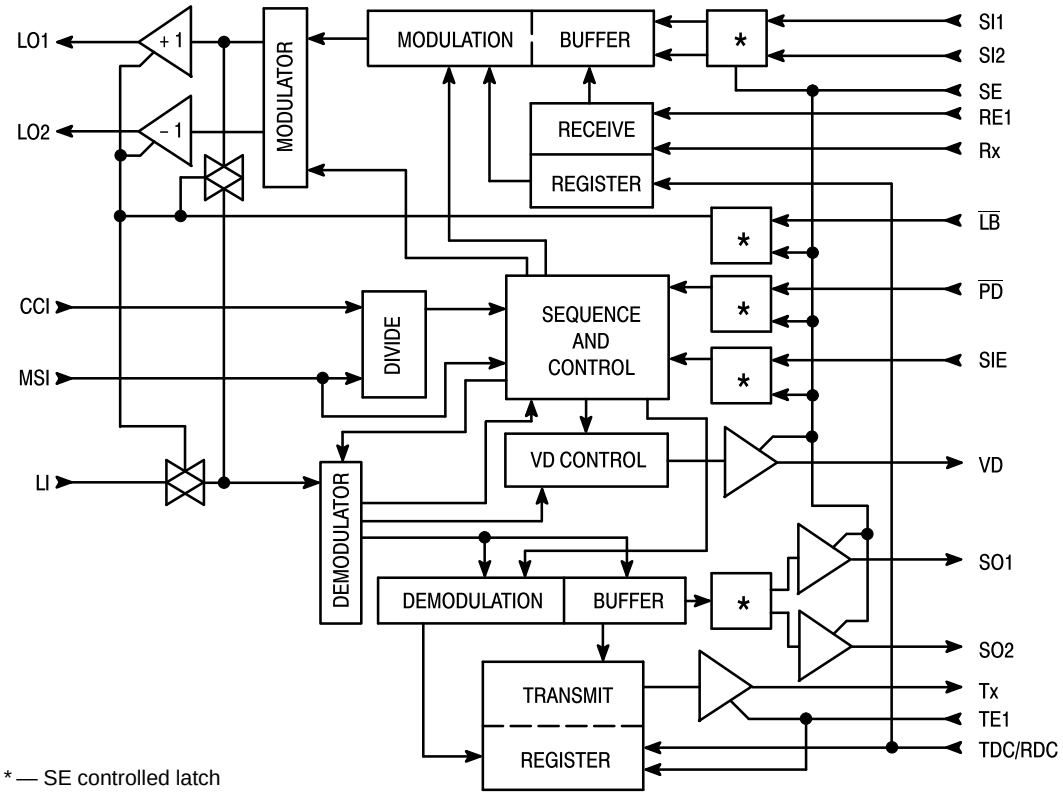


MC145426 — SLAVE (SOG PACKAGE)



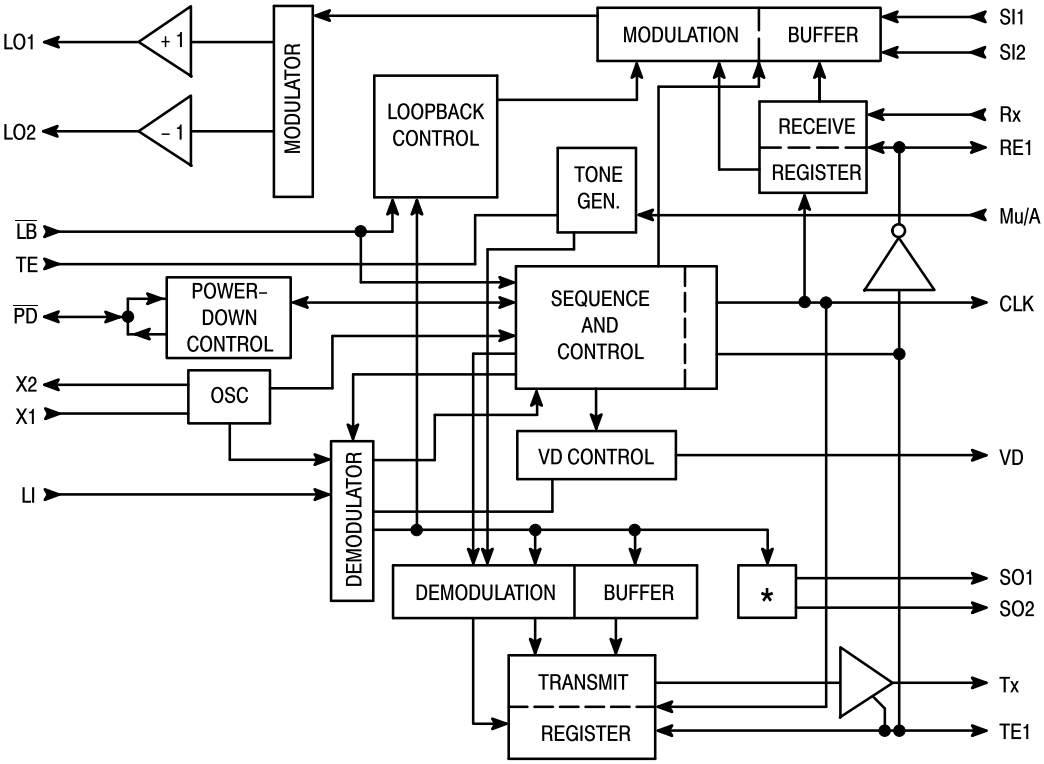
NC = NO CONNECTION

MC145422 MASTER UDLT BLOCK DIAGRAM



* — SE controlled latch

MC145426 SLAVE UDLT BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	– 0.5 to + 9.0	V
Voltage, Any Pin to V_{SS}	V	– 0.5 to V_{DD} + 0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	± 10	mA
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Parameter	Pins	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.5	V
Power Dissipation ($\overline{PD}$ = V_{DD}, V_{DD} = 5 V)	V_{DD}	—	80	mW
Power Dissipation ($\overline{PD}$ = V_{SS}, TE = V_{SS})	V_{DD}	—	75	mW
MC145422 Frame Rate	MSI	7.9	8.1	kHz
MC145422 — MC145426 Frame Rate Slip (See Note 1)	—	—	0.25	%
CCI Clock Frequency (MSI = 8 kHz)	CCI	—	2.048	MHz
Data Clock Rate MC145422	TDC, RDC	64	2560	kHz
Modulation Baud Rate (See Note 2)	LO1, LO2	—	256	kHz

NOTES:
1. The MC145426 crystal frequency divided by 512 must equal the MC145422 MSI Frequency ± 0.25% for optimum operation.
2. Assumes crystal frequency of 4.096 MHz for the MC145426 and 2.048 MHz CCI for the MC145422.

DIGITAL CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Input High Level		3.5	—	V
Input Low Level		—	1.5	V
Input Current	Except LI LI	– 1.0 – 100	1.0 100	μA
Input Capacitance		—	7.5	pF
Output High Current (Except Tx on MC145422 and Tx and $\overline{PD}$ on MC145426)	V_{OH} = 2.5 V V_{OH} = 4.6 V	– 1.7 – 0.36	— —	mA
Output Low Current (Except Tx on MC145422 and Tx and $\overline{PD}$ on MC145426)	V_{OL} = 0.4 V V_{OL} = 0.8 V	0.36 0.8	— —	mA
$\overline{PD}$ Output High Current (MC145426) (See Note 1)	V_{OH} = 2.5 V V_{OH} = 4.6 V	– 90 – 10	— —	μA
$\overline{PD}$ Output Low Current (MC145426) (See Note 1)	V_{OL} = 0.4 V V_{OL} = 0.8 V	60 100	— —	μA
Tx Output High Current	V_{OH} = 2.5 V V_{OH} = 4.6 V	– 3.4 – 0.7	— —	mA
Tx Output Low Current	V_{OL} = 0.4 V V_{OL} = 0.8 V	1.7 3.5	— —	mA
Tx Input Impedance (TE1 = V_{SS}, MC145422)		100	—	kΩ
Crystal Frequency (MC145426, Note 2)		4.0	4.4	MHz
PCM Tone (TE = V_{DD}, MC145426)		– 22	– 18	dBm0
Three–State Current (SO1, SO2, VD, Tx on MC145422, Tx on MC145426)		—	± 1	μA
V_{ref} Voltage (See Note 3)		2	3	V
X2 — Oscillator Output High Drive Current (MC145426) (See Note 4)	V_{OH} = 4.6 V	– 450	—	μA
X2 — Oscillator Output Low Drive Current (MC145426) (See Note 4)	V_{OL} = 0.4 V	450	—	μA

NOTES:
1. To overdrive $\overline{PD}$ from a low level to 3.5 V or a high level to 1.5 V requires a minimum of ± 800 μA drive capability.
2. The MC145426 crystal frequency divided by 512 must equal the MC145422 MSI frequency ± 0.25% for optimum performance.
3. V_{ref} typically (9/20 $V_{DD} - V_{SS}$).
4. Output drive when X1 is being driven from an external clock.

ANALOG CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Modulation Differential Amplitude (R_L = 440 Ω)	LO1 to LO2	4.5	6.0	V p–p
Modulation Differential DC Offset		0	300	mV
Demodulator Input Amplitude (See Note)		0.050	2.5	V peak
Demodulator Input Impedance		50	150	kΩ

NOTE: The input level into the demodulator to reliably demodulate incoming bursts. Input referenced to V_{ref}.

MC145422 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Figure No.	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	—	4	µs
Input Fall Time	All Digital Inputs	1	t_f	—	4	µs
Pulse Width	TDC/RDC, RE1, MSI	1	t_W(H,L)	90	—	ns
CCI Duty Cycle		1	t_W(H,L)	45	55	%
Data Clock Frequency	TDC/RDC	—	t_{DC}	64	2560	kHz
Propagation Delay Time	MSI to SO1, SO2 VD ($\overline{PD}$ = V_{DD}) TDC to Tx	2 3	t_{PLH}, t_{PHL}	— —	90 90	ns
MSI to TDC/RDC Setup Time		4	t_{su3} t_{su4}	90 40	— —	ns
TE1/RE1 to TDC/RDC Setup Time		4	t_{su3} t_{su4}	90 40	— —	ns
Rx to TDC/RDC Setup Time		5	t_{su5}	60	—	ns
Rx to TDC/RDC Hold Time		5	t_{h1}	60	—	ns
SI1, SI2 to MSI Setup Time		6	t_{su6}	60	—	ns
SI1, SI2 to MSI Hold Time		6	t_{h2}	60	—	ns

MC145426 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Figure No.	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	—	4	µs
Input Fall Time	All Digital Inputs	1	t_f	—	4	µs
Clock Output Pulse Width	CLK	1	t_W(H,L)	3.8	4.0	µs
Crystal Frequency		—	f_{X1}	4.086	4.1	MHz
Propagation Delay Times	TE1 Rising to CLK (TE = V_{DD}) TE1 Rising to CLK (TE = V_{SS}) CLK to TE1 Falling CLK to RE1 Rising RE1 Falling to CLK (TE = V_{DD}) RE1 Falling to CLK (TE = V_{SS}) CLK to Tx TE1 to SO1, SO2	7 7 7 8 8 8 9 9	t_{p1} t_{p1} t_{p2} t_{p3} t_{p4} t_{p4} t_{p5} t_{p6}	– 50 438 — — – 50 438 — —	50 538 40 40 50 538 90 90	ns
Rx to CLK Setup Time		5	t_{su5}	60	—	ns
Rx to CLK Hold Time		5	t_{h1}	60	—	ns
SI1, SI2 to TE1 Setup Time		6	t_{su6}	60	—	ns
SI1, SI2 to TE1 Hold Time		6	t_{h2}	60	—	ns

SWITCHING WAVEFORMS

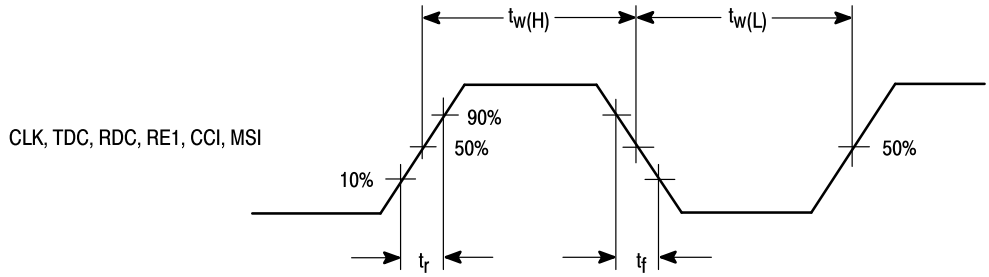


Figure 1.

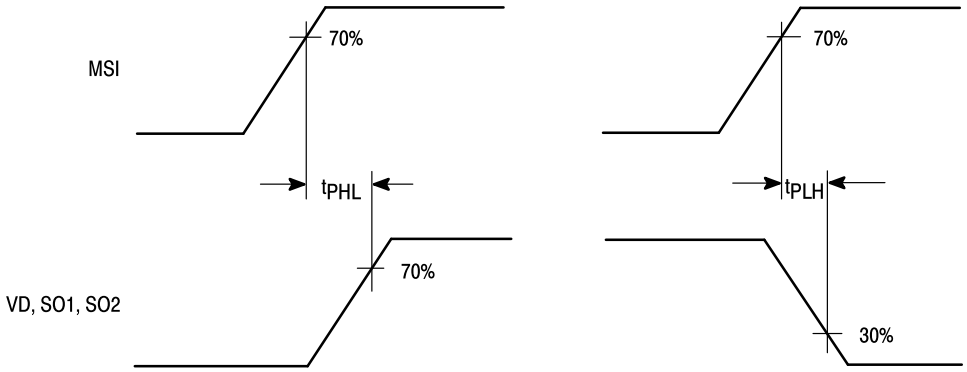


Figure 2.

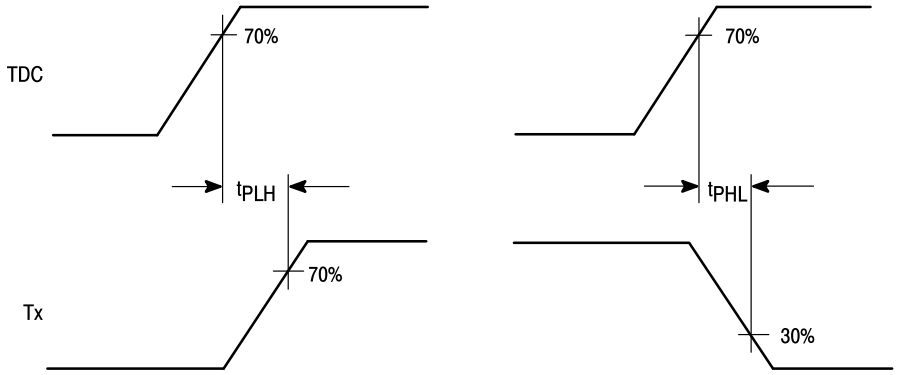


Figure 3.

SWITCHING WAVEFORMS (continued)

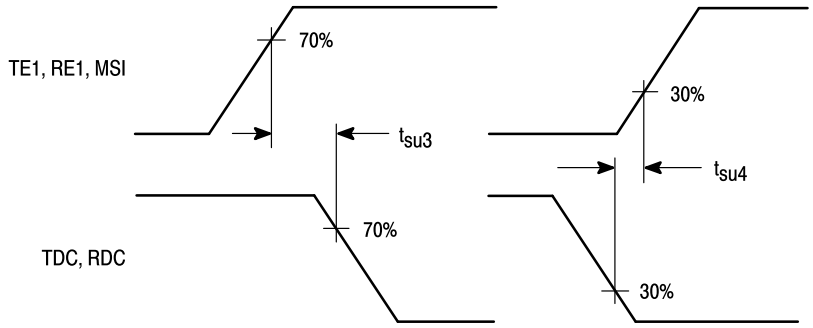


Figure 4.

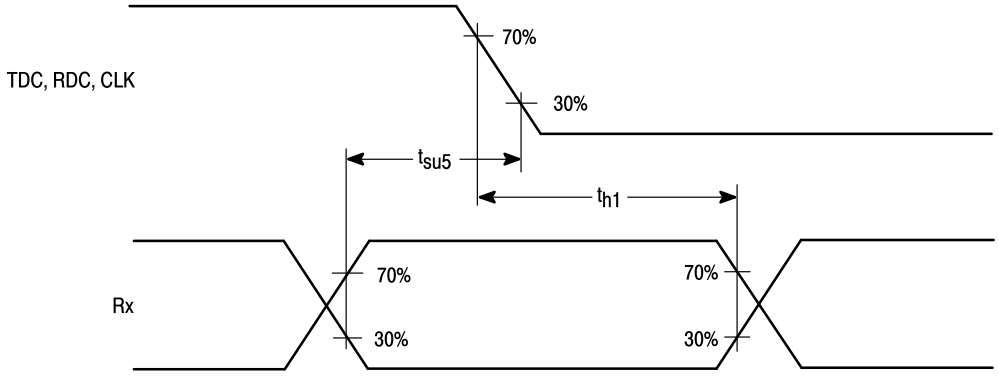


Figure 5.

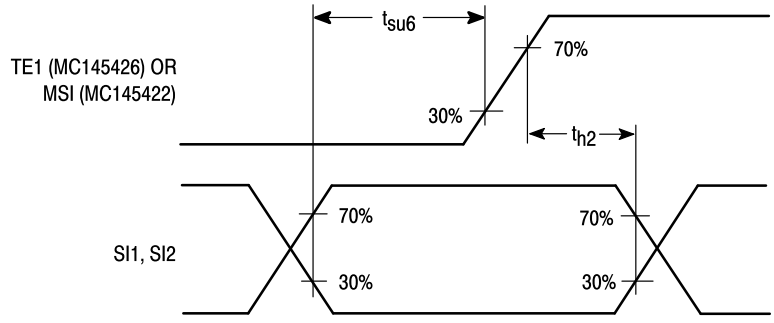


Figure 6.

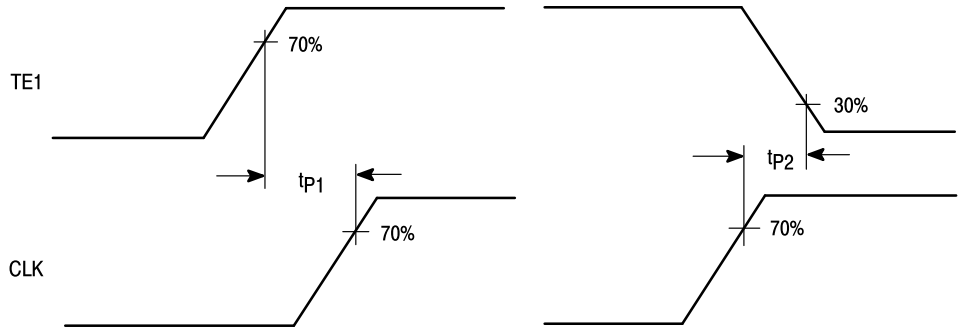


Figure 7.

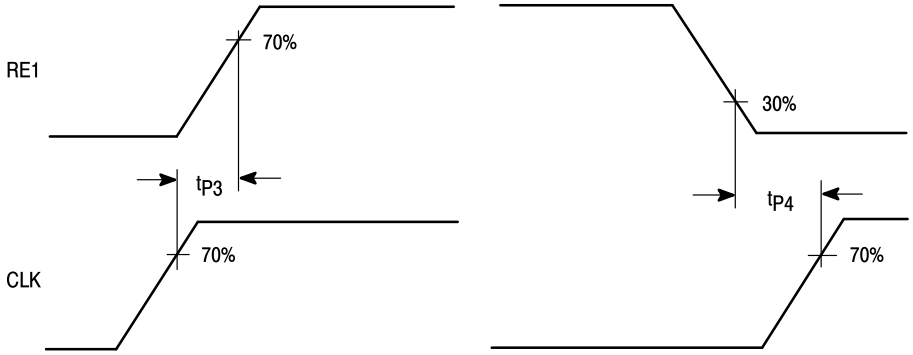


Figure 8.

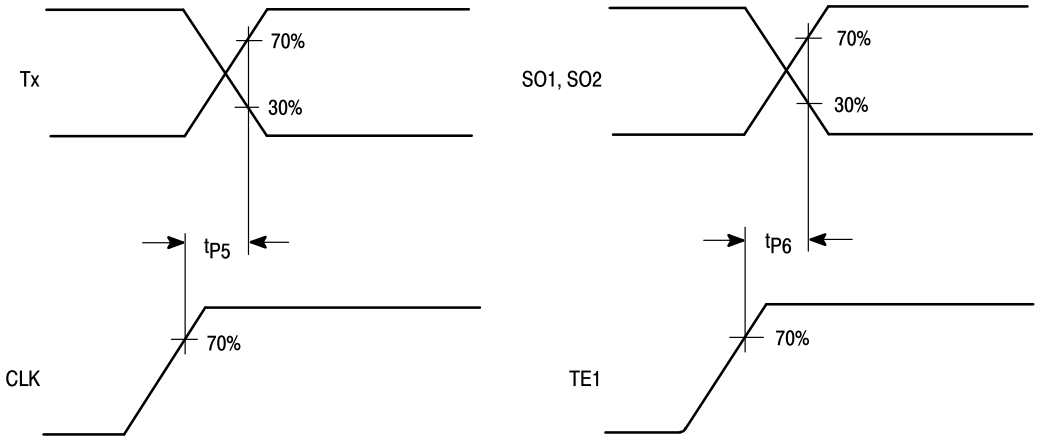


Figure 9.

MC145422 MASTER UDLT PIN DESCRIPTIONS

V_{DD}
Positive Supply

Normally 5 V.

V_{SS}
Negative Supply

This pin is the most negative supply pin, normally 0 V.

V_{ref}
Reference Output

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} by 0.1 µF capacitors. No external dc load should be placed on this pin.

LI
Line Input

This input to the demodulator circuit has an internal 100 kΩ resistor tied to the internal reference node so that an external capacitor and/or line transformer may be used to couple the input signal to the part with no dc offset.

$\overline{LB}$
Loopback Control

A low on this pin disconnects the LI pin from internal circuitry, drives LO1, LO2 to V_{ref} and internally ties the modulator output to the demodulator input which loops the part on itself for testing in the system. The state of this pin is internally latched if the SE pin is brought and held low. Loopback is active only when $\overline{PD}$ Is high.

VD
Valid Data Output

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a line transmission. VD is a standard B–series CMOS output and is high impedance when SE is held low.

SI1, SI2
Signaling Bit Inputs

Data on these pins is loaded on the rising edge of MSI for transmission to the slave. The state of these pins is internally latched if SE is held low.

SO1, SO2
Signaling Bit Outputs

These outputs are received signaling bits from the slave UDLT and change state on the rising edge of MSI if $\overline{PD}$ is high, or at the completion of demodulation if $\overline{PD}$ is low. These outputs have standard B–series CMOS drive capability and are high impedance if the SE pin is held low.

SE
Signal Enable Input

If held high, the $\overline{PD}$, $\overline{LB}$, SI1, SI2, and SIE inputs and the SO1, SO2, and VD outputs function normally. If held low, the state of these inputs is latched and held internally while the outputs are high impedance. This allows these pins to be bussed with those of other UDLTs to a common controller.

$\overline{PD}$
Power–Down Input

If held low, the UDLT ceases modulation. In power–down, the only active circuit is that which is necessary to demodulate an incoming burst and output the signal and valid data bits. Internal data transfers to the transmit and receive registers cease. When brought high, the UDLT powers up, and waits three positive MSI edges or until the end of an incoming transmission from the slave UDLT and begins transmitting every MSI period to the slave UDLT on the next rising edge of the MSI.

MSI
Master Sync Input

This pin is the system sync and initiates the modulation on the twisted pair. MSI should be approximately leading–edge aligned with TDC/RDC.

SIE
Signal Insert Enable

This pin, when held high, inserts signal bit 2 received from the slave into the LSB of the outgoing PCM word at Tx and will ignore the SI2 pin and use in place the LSB of the incoming PCM word at Rx for transmission to the slave. The PCM word to the slave will have LSB forced low in this mode. In this manner, signal bit 2 to/from the slave UDLT is inserted in to the PCM words the master sends and receives from the backplane for routing through the PABX for simultaneous voice/data communication. The state of this pin is internally latched if the SE pin is brought and held low.

TE1
Transmit Data Enable 1 Input

This pin controls the outputting of data on the Tx pin. While TE1 is high, the Tx data is presented on the eight rising edges of TDC/RDC. TE1 is also a high–impedance control of the Tx pin. If MSI occurs during this period, new data will be transferred to the Tx output register in the ninth high period of TDC/RDC after TE1 rises; otherwise, it will transfer on the rising edge of MSI. TE1 and TDC/RDC should be approximately leading–edge aligned.

Tx
Transmit Data Output

This three–state output presents new voice data during the high periods of TDC/RDC when TE1 is high (see TE1).

CCI
Convert Clock Input

A 2.048 MHz clock signal should be applied to this pin. The signal is used for internal sequencing and control. This signal should be coherent with MSI for optimum performance but may be asynchronous if slightly worse error rate performance can be tolerated.

TDC/RDC
Transmit/Receive Data Clock

This pin is the transmit and receive data clock and can be 64 kHz to 2.56 MHz. Data is output at the Tx pin while TE1 is high on the eight rising edges of TDC/RDC after the rising edge of TE1. Data on the Rx pin is loaded into the receive register of the UDLT on the eight falling edges of TDC/RDC after a positive transition on RE1. This clock should be approximately leading–edge aligned with MSI.

Rx
Receive Data

Voice data is clocked into the UDLT from this pin on the falling edges of TDC/RDC under the control of RE1.

RE1
Receive Data Enable 1 Input

A rising edge on this pin will enable data on the Rx pin to be loaded into the receive data register on the next eight falling edges of the data dock, TDC/RDC. RE1 and TDC/RDC should be approximately leading–edge aligned.

LO1, LO2
Line Driver Outputs

These outputs drive the twisted pair line with 256 kHz modified DPSK bursts each frame and are push–pull. These pins are driven to V_{ref} when not modulating the line.

MC145426 SLAVE UDLT PIN DESCRIPTIONS

V_{DD}
Positive Supply

Normally 5 V.

V_{SS}
Negative Supply

This pin is the most negative supply pin, normally 0 V.

V_{ref}
Reference Output

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} by 0.1 μF capacitors. No external dc load should be placed on this pin.

LI
Line Input

This input to the demodulator circuit has an internal 100 kΩ resistor tied to the internal reference node (V_{ref}) so that an external capacitor and/or line transformer may be used to couple the signal to this part with no dc offset.

$\overline{LB}$
Loopback Control

When this pin is held low and $\overline{PD}$ is high (the UDLT is receiving transmissions from the master), the UDLT will use the 8 bits of demodulated PCM data in place of the 8 bits of Rx data in the return burst to the Master, thereby looping the part back on itself for system testing. SI1 and SI2 operate normally in this mode. CLK will be held low during loopback operation.

VD
Valid Data Output

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors.VD changes state on the leading edge of TE1. If no transmissions from the master have been received in the last 250 μs (derived from the internal oscillator), VD will go low without TE1 rising since TE1 is not generated in the absence of received transmissions from the master (see TE pin description for the one exception to this).

SI1, SI2
Signaling Bit Inputs

Data on these pins is loaded on the rising edge of TE1 for transmission to the master. If no transmissions from the master are being received and $\overline{PD}$ is high, data on these pins will be loaded into the part on an internal signal. Therefore, data on these pins should be steady until synchronous communication with the master has been established, as indicated by the high on VD.

SO1, SO2
Signaling Bit Outputs

These outputs are received signaling bits from the master UDLT and change state on the rising edge of TE1. These outputs have standard B–series CMOS output drive capability.

$\overline{PD}$
Power–Down Input/Output

This is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the UDLT is powered down and the only active circuitry is that which is necessary for demodulation, TE1/RE1/CLK generation upon demodulation, the outputting of data received from the master, and updating of VD status. When held high, the UDLT is powered up and transmits in response to transmissions from the master. If no received bursts from the master have occurred when powered up for 250 μs (derived from the internal oscillator frequency), the UDLT will generate a free running 125 μs internal clock from the internal oscillator and will burst a transmission to the master every other internal 125 μs clock using data on the SI1 and SI2 pins and the last data word loaded into the receive register. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave UDLT to self power–up and down in demand powered loop systems.

TE
Tone Enable

A high on this pin generates a 500 Hz square wave PCM tone and inserts it in place of the demodulated voice PCM word from the master for outputting to the Tx pin to the telset mono–circuit. A high on TE will generate TE1 and CLK from the internal oscillator when the slave is not receiving bursts from the master so that the PCM square wave can be loaded into the codec–filter. This feature allows the user to provide audio feedback for the telset keyboard depressions except during loopback. During loopback of the slave UDLT, CLK is defeated so a tone cannot be generated in this mode.

TE1
Transmit Data Enable 1 Output

This is a standard B–series CMOS output which goes high after the completion of demodulation of an incoming transmission from the master. It remains high for 8 CLK periods and then low until the next burst from the master is demodulated. While high, the voice data just demodulated is output on the first eight rising edges of CLK at the Tx pin. The signaling data just demodulated is output on SO1 and SO2 on TE1's rising edge, as is VD.

Tx
Transmit Data Output

This is a standard B–series CMOS output. Voice data is output on this pin on the rising edges of CLK while TE1 is high and is high impedance when TE1 is low.

X1
Crystal Input

A 4.096 MHz crystal is tied between this pin and X2. A 10 MΩ resistor across X1 and X2 and 25 pF capacitors from X1 and X2 to V_{SS} are required for stability and to ensure startup. X1 may be driven by an external CMOS clock signal if X2 is left open.

X2
Crystal Output

This pin is capable of driving one external CMOS input and 15 pF of additional capacitance (see X1 pin description).

CLK
Clock Output

This is a standard B–series CMOS output which provides the data clock for the telset codec–filter. It is generated by dividing the oscillator down to 128 kHz and starts upon the completion of demodulation of an incoming burst from the master. At this time, CLK begins and TE1 goes high. CLK will remain active for 16 periods, at the end of which it will remain low until another transmission from the master is demodulated. In this manner, sync from the master is established in the slave and any clock slip between the master and the slave is absorbed each frame. CLK is generated in response to an incoming burst from the master, however, if TE is brought high, then CLK and TE1/RE1 are generated from the internal oscillator until TE is brought low or an incoming burst from the master is received. CLK is disabled when $\overline{LB}$ is held low.

Rx
Receive Data Input

Voice data from the telset codec–filter is input on this pin on the first eight falling edges of CLK after RE1 goes high.

Mu/A
Tone Digital Format Input

This pin determines if the PCM code of the 500 Hz square wave tone, when TE is high, is Mu–Law (Mu/A = 1) or A–Law (Mu/A = 0) format.

RE1
Receive Data Enable 1 Output

This is a standard B–series CMOS output which is the inverse of TE1 (see TE1 pin description).

LO1, LO2
Line Driver Outputs

These outputs drive the twisted pair line with 256 kHz modified DPSK bursts each frame and are push–pull. These pins are driven to V_{ref} when the device is not modulating.

BACKGROUND

The MC145422 master and MC145426 slave UDLT transceiver ICs main application is to bidirectionally transmit the digital signals present at a codec–filter digital–PABX backplane interface over normal telephone wire pairs. This allows the remoting of the codec–filter in a digital telephone set and enables each set to have a high speed data access to the PABX switching facility. In effect, the UDLT allows each PABX subscriber direct access to the inherent 64 kbps data routing capabilities of the PABX.

The UDLT provides a means for transmitting and receiving 64 kbits of voice data and 16 kbps of signaling data in two–wire format over normal telephone pairs. The UDLT is a two–chip set consisting of a master and a slave. The master UDLT replaces the codec–filter and SLIC on the PABX line card, and transmits and receives data over the wire pair to the teleset. The UDLT appears to the linecard and backplane as if it were a PCM Codec–Filter and has almost the same digital interface features as the MC145500 series codec–filters. The slave UDLT is located in the telset and interfaces the codec–filter to the wire pair. By hooking two UDLTs back–to–back, a repeater can also be formed. The master and slave UDLTs operate in a frame synchronous manner, sync being established at the slave by the timing of the master's transmission. The master's sync is derived from the PABX frame sync.

The UDLT operates using one twisted pair. Eight bits of voice data and two bits of signaling data are transmitted and received each frame in a half–duplex manner (i.e., the slave waits until the transmission from the master is completely received before transmitting back to the master). Transmission occurs at 256 kHz bit rate using a modified form of DPSK. This "ping– pong" mode will allow transmission of data at distances up to two kilometers before turnaround delay becomes a problem. The UDLT is so defined as to allow this data to be handled by the linecard, backplane, and PABX as if it were just another voice conversation. This allows existing PABX hardware and software to be unchanged and yet provides switched 64 kbps voice or data communications throughout its service area by simply replacing a subscriber's linecard and teleset. A feature in the master allows one of the two signaling bits to be inserted and extracted from the backplane PCM word to allow simultaneous voice and data transmission through the PABX. Both UDLTs have a loopback feature by which the device can be tested in the user system.

The slave UDLT has the additional feature of providing a 500 Hz Mu–Law or A–Law coded square wave to the codec–filter when the TE pin is brought high. This can be used to provide audio feedback in the telset during keyboard depressions.

CIRCUIT DESCRIPTION

GENERAL

The UDLT consists of a modulator, demodulator, two intermediate data buffers, sequencing and control logic, and transmit and receive data registers. The data registers interface to the linecard or codec–filter digital interface signals, the modulator and demodulator interface the twisted pair transmission medium, while the intermediate data registers buffer data between these two sections. The UDLT is

intended to operate on a single 5 V supply and can be driven by TTL or CMOS logic.

MASTER OPERATION

In the master, data from the linecard is loaded into the receive register each frame from the Rx pin under the control of the TDC/RDC clock and the receive data enable, RE1. RE1 controls loading of eight serial bits, henceforth referred to as the voice data word. Each MSI, these words are transferred out of the receive register to the modulation buffer for subsequent modulation onto the line. The modulation buffer takes the receive voice data word and the two signaling data input bits on SI1 and SI2 loaded on the MSI transition and formats the 10 bits into a specific order. This data field is then transmitted in a 256 kHz modified DPSK burst onto the line to the remote slave UDLT.

Upon demodulating the return burst from the slave, the decoded data is transferred to the demodulation buffer and the signaling bits are stripped ready to be output on SO1 and SO2 at the next MSI. The voice data word is loaded into the transmit register as described in the TE1 pin description for outputting via the Tx pin at the TDC/RDC data clock rate under the control of TE1. VD is output on the rising edge of MSI. Timing diagrams for the master are shown in Figure 10.

SLAVE OPERATION

In the slave, the synchronizing event is the detection of an incoming line transmission from the master as indicated by the completion of demodulation. When an incoming burst from the master is demodulated, several events occur. As in the master, data is transferred from the demodulator to the demodulation buffer and the signaling bits are stripped for outputting at SO1 and SO2. Data in the receive register is transferred to the modulation buffer. TE1 goes high loading in data at SI1 and SI2, which will be used in the transmission burst to the master along with the data in the transmit data buffer, and outputting SO1, SO2, and VD. Modulation of the burst begins four 256 kHz periods after the completion of demodulation.

While TE1 is high, voice data is output on Tx to the telset codec–filter on the rising edges of the data clock output on the CLK pin. On the ninth rising edge of CLK, TE1 goes low, RE1 goes high, and voice data from the codec–filter is input to the receiver register from the Rx pin on the next eight falling edges of CLK. RE1 is TE1 inverted and is provided to facilitate interface to the codec–filter.

The CLK pin 128 kHz output is formed by dividing down the 4.096 MHz crystal frequency by 32. Slippage between the frame rate of the master (as represented by the completion of demodulation of an incoming transmission from the master) and the crystal frequency is absorbed by holding the 16th low period of CLK until the next completion of demodulation. This is shown in the slave UDLT timing diagram of Figure 11.

POWER–DOWN OPERATION

In the master when $\overline{PD}$ is low, the UDLT stops modulating and only that circuitry necessary to demodulate the incoming bursts and output the signaling and VD data bits is active. In this mode, if the UDLT receives a burst from the slave, the SO1, SO2, and VD pins will change state upon completion of the demodulation instead of the the rising edge of MSI. The state of these pins will not change until either three rising MSI edges have occurred without the reception of a burst from the slave or until another burst is demodulated, whichever occurs first.

When $\overline{PD}$ is brought high, the master UDLT will wait either three rising MSI edges or until the MSI rising edge following the demodulation of an incoming burst before transmitting to the slave. The data for the first transmission to the slave after power–up is loaded into the UDLT during the RE1 period prior to the burst in the case of voice, and on the present rising edge of MSI for signaling data.

In the slave, $\overline{PD}$ is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the UDLT slave is powered–down and only that circuitry necessary for demodulation, TE1/RE1/CLK generation upon demodulation, and the outputting of voice and signaling bits is active. When held high, the UDLT slave is powered–up and transmits normally in response to transmissions from the master. If no bursts have been received from the master within 250 μs after power–up (derived from the internal oscillator frequency), the UDLT generates an internal 125 μs free–running clock from the internal oscillator. The slave UDLT then bursts a transmission to the master UDLT every other 125 μs clock period using data loaded into the Rx pin during the last RE1 period and SI1, SI2 data loaded in on the internal 125 μs clock edge. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave UDLT to self power–up and down in demand power–loop systems.

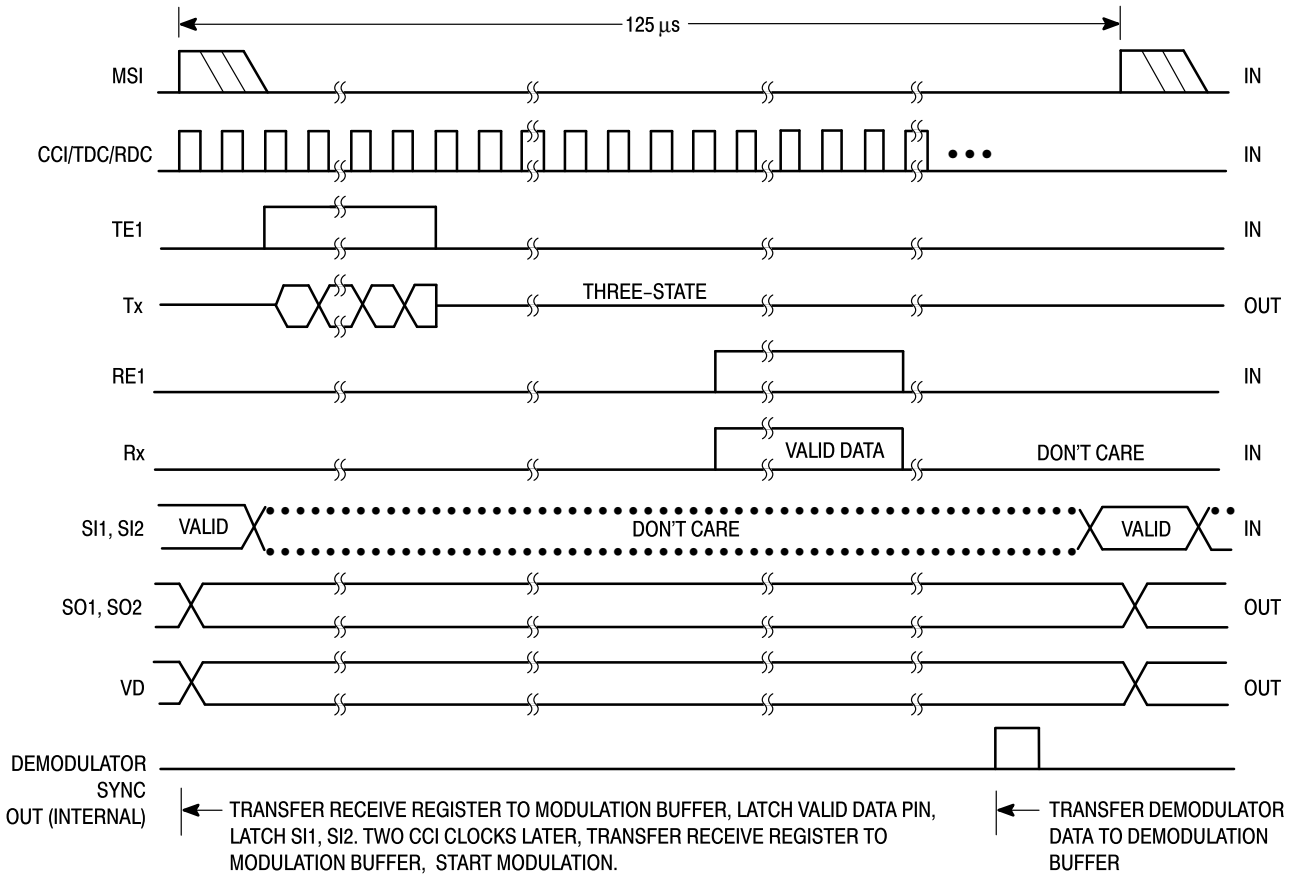
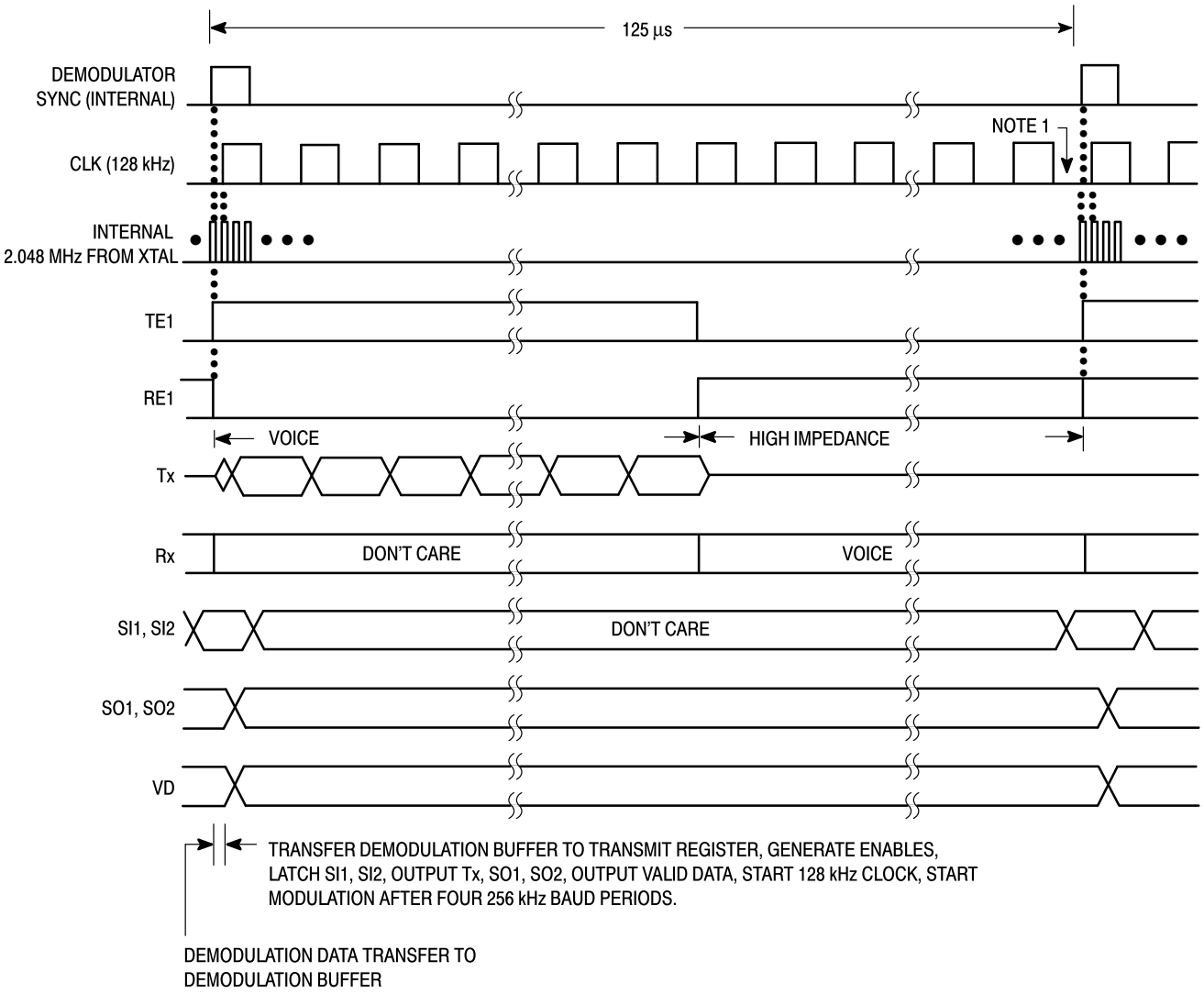


Figure 10. Master UDLT Timing



NOTE: 1. Slip between master and slave is taken up in this period.

Figure 11. Slave UDLT Timing

Both the Differential–Phase Shift Keying and the Modified Differential–Phase–Shift Keying waveforms are shown in Figures 12 thru 14. The DPSK encodes data as phase reversals of a 256 kHz carrier. A 0 is indicated by a 180° phase shift between bit boundaries, while the signal continues in phase to indicate a 1. This method needs no additional bits to indicate the start of the burst.

The modified DPSK waveform actually used in the transceivers is a slightly modified form of DPSK, as shown in Figure 12. The phase–reversal cusps of the DPSK waveform have been replaced by a 128 kHz half–cycle to lower the spectral content of the waveform, which, save for some key differences, appears quite similar to frequency shift keying. The burst always begins and ends with a half–cycle of 256 kHz, which helps locate bit boundaries.

The bit pattern shown in Figure 13a shows a stable waveform due to the even number of phase changes or zeros. The waveform shown in Figure 13b shows random data patterns being modulated.

Figure 14 shows the “ping–pong” signals on 3000 feet of 26 AWG twisted–pair wire as viewed at LI of the master UDLT and the slave UDLT.

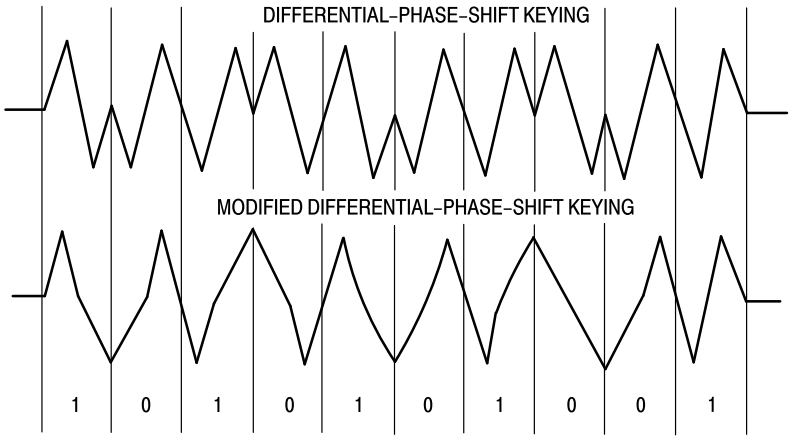
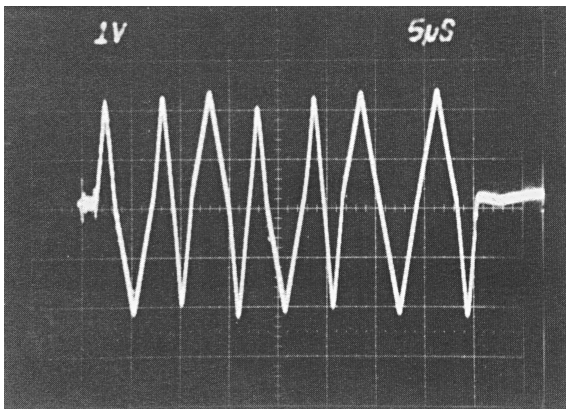
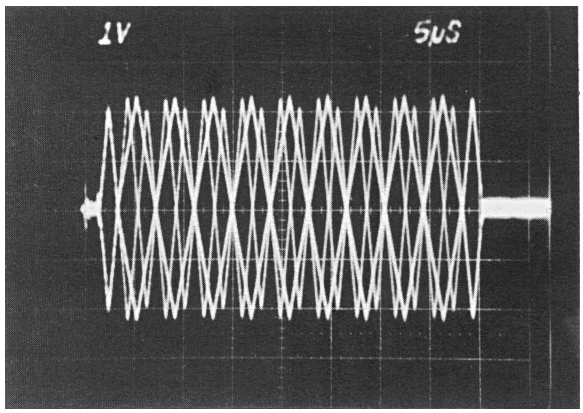


Figure 12. Modified Differential Phase Shift Keying



13a. Bit Pattern — 1010101000



13b. Bit Pattern — Random

Figure 13. Typical Signal Waveforms at Demodulator

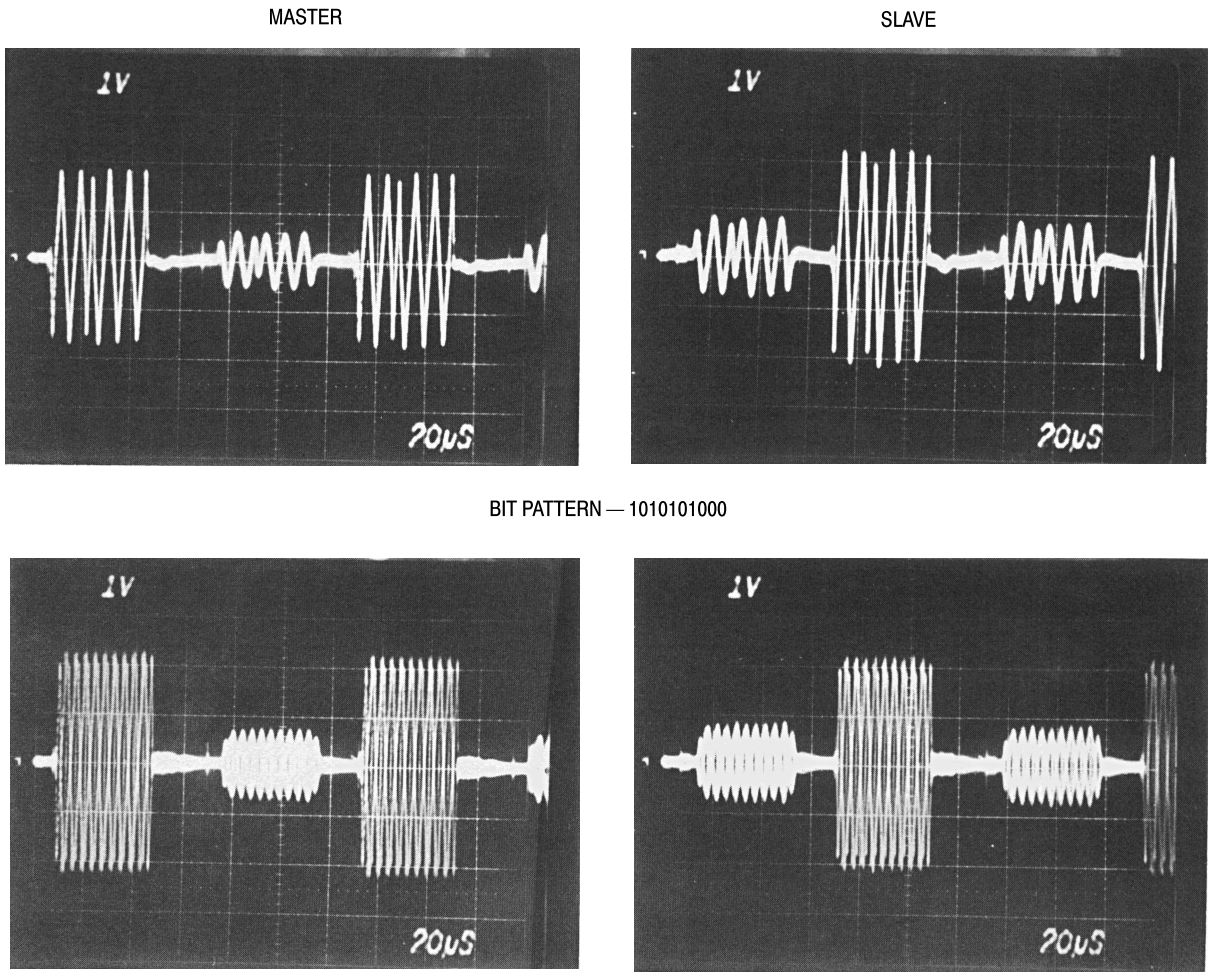


Figure 14. Typical Signal Waveforms at Demodulator

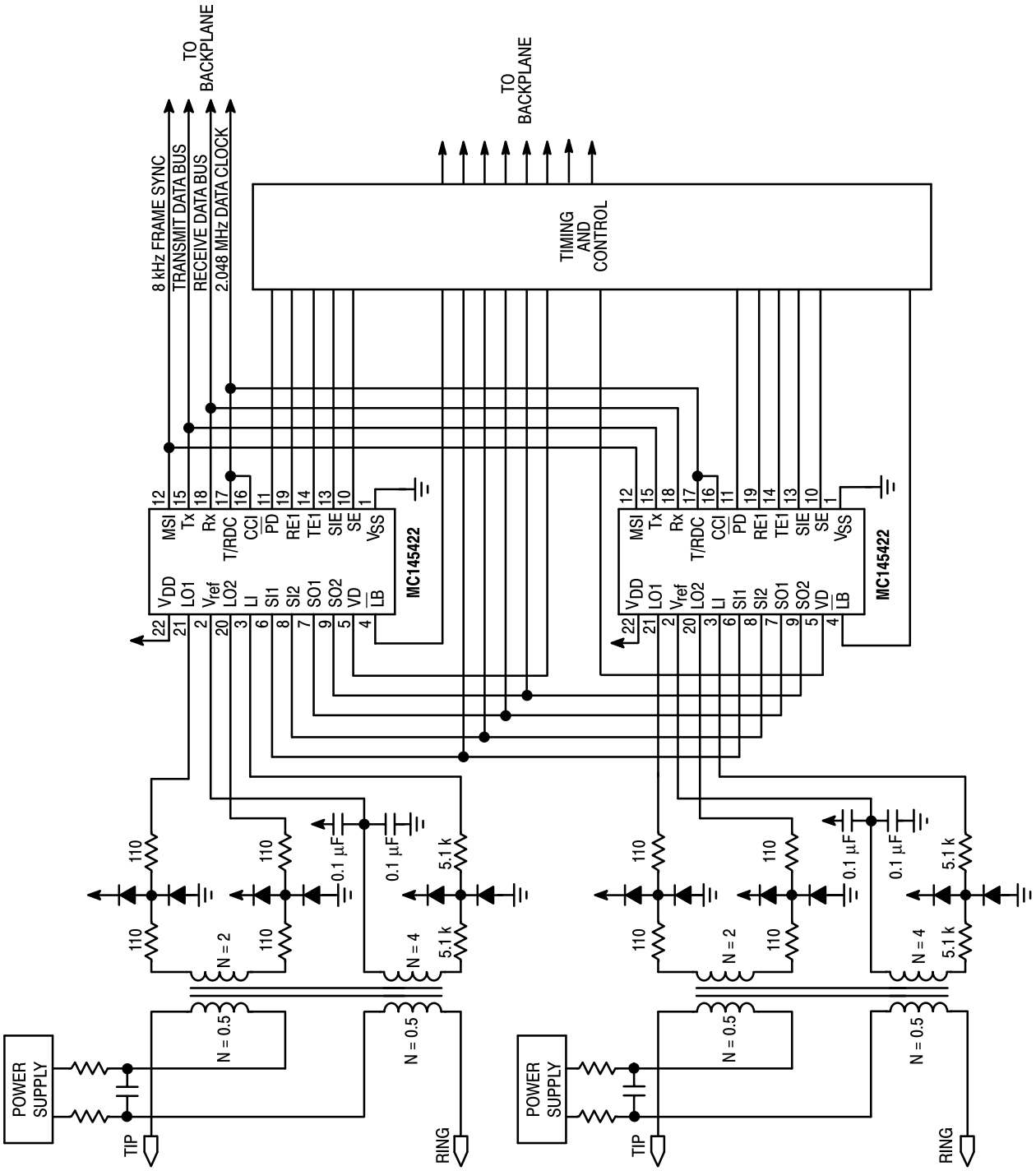


Figure 15. Typical Multichannel Digital Line Card

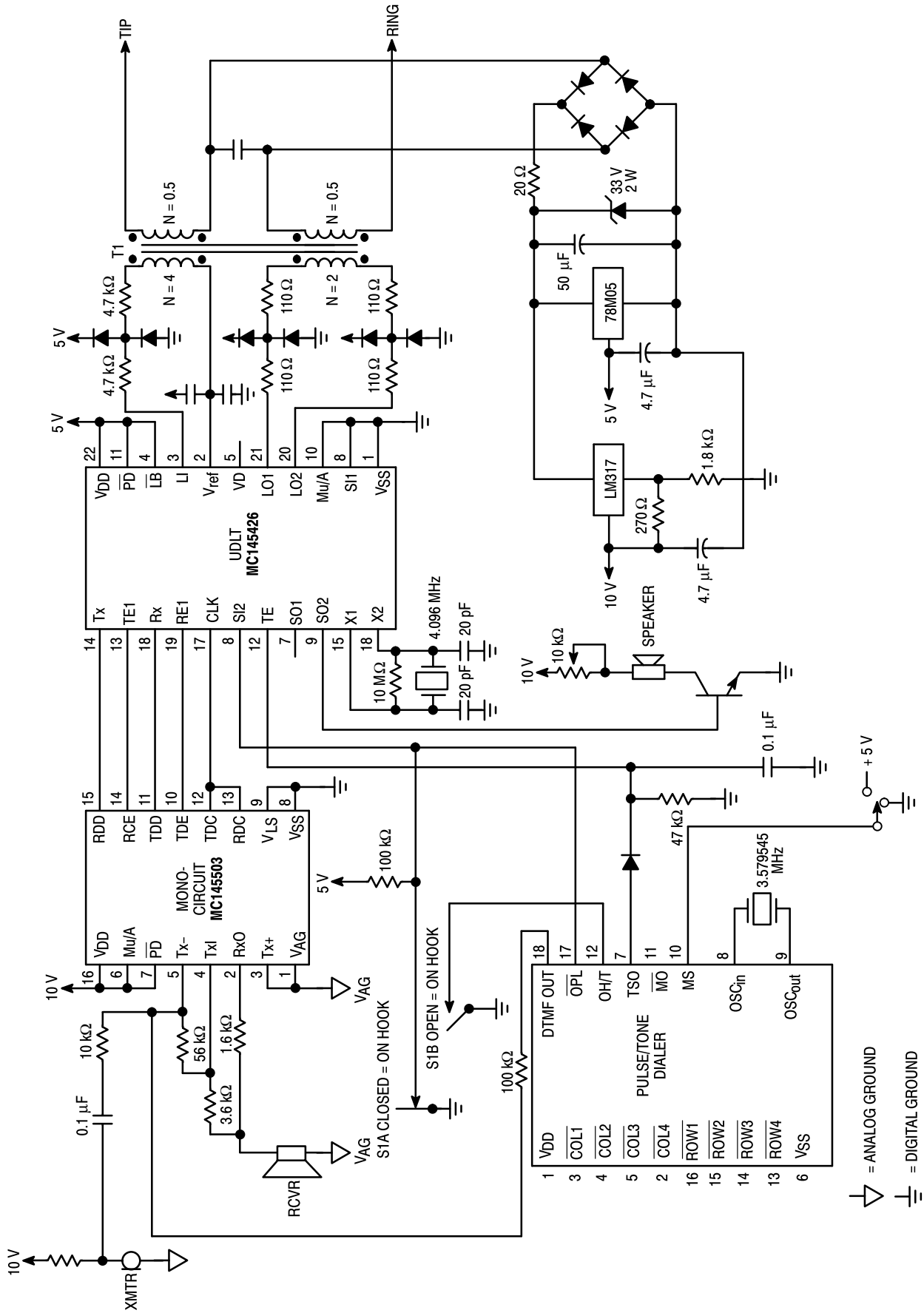


Figure 16. Basic Digital Telset

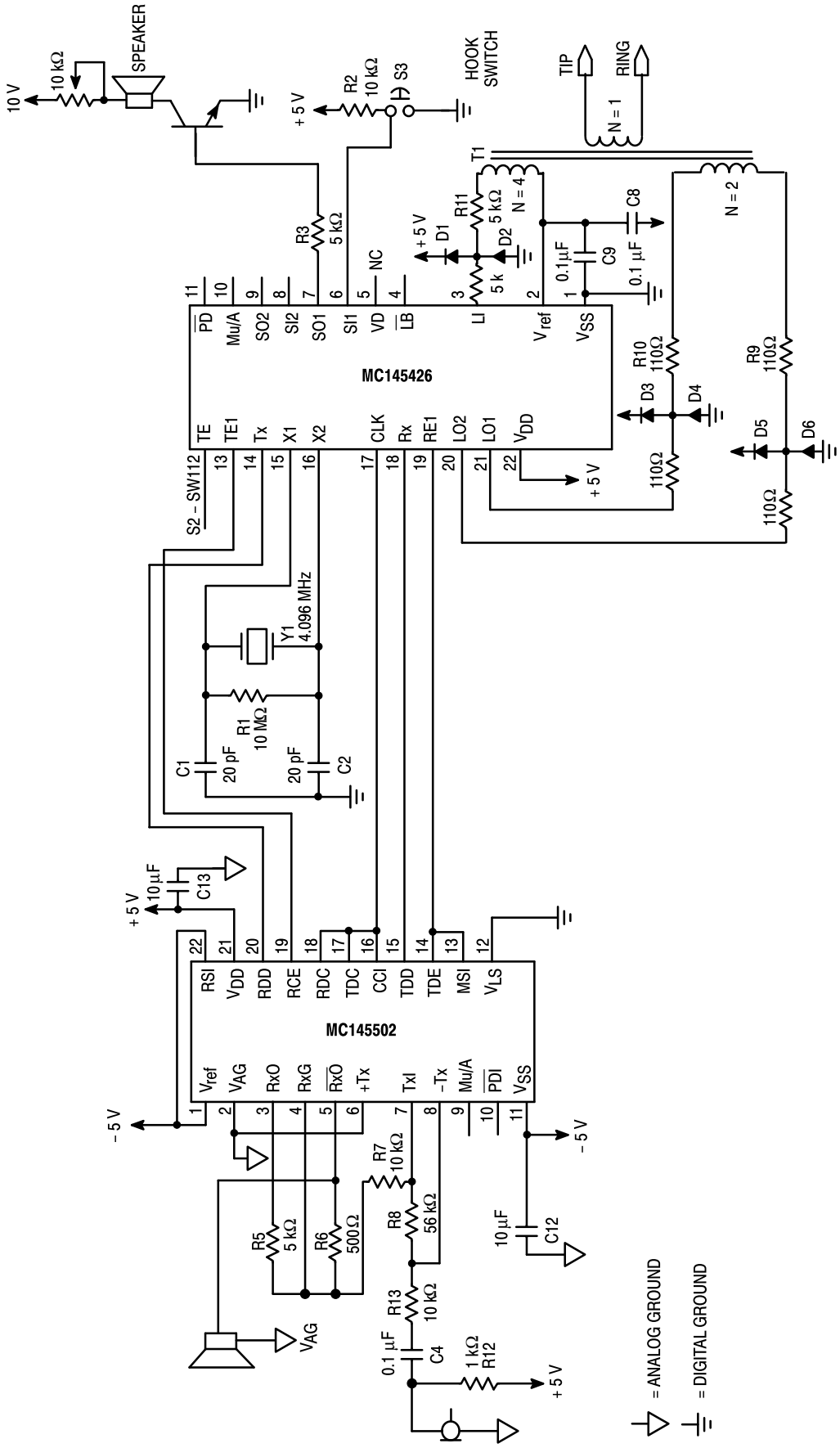
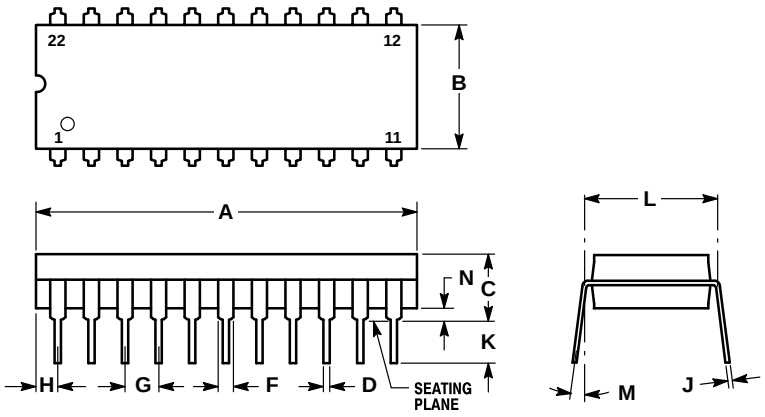


Figure 17. Full–Featured Digital Telset

PACKAGE DIMENSIONS

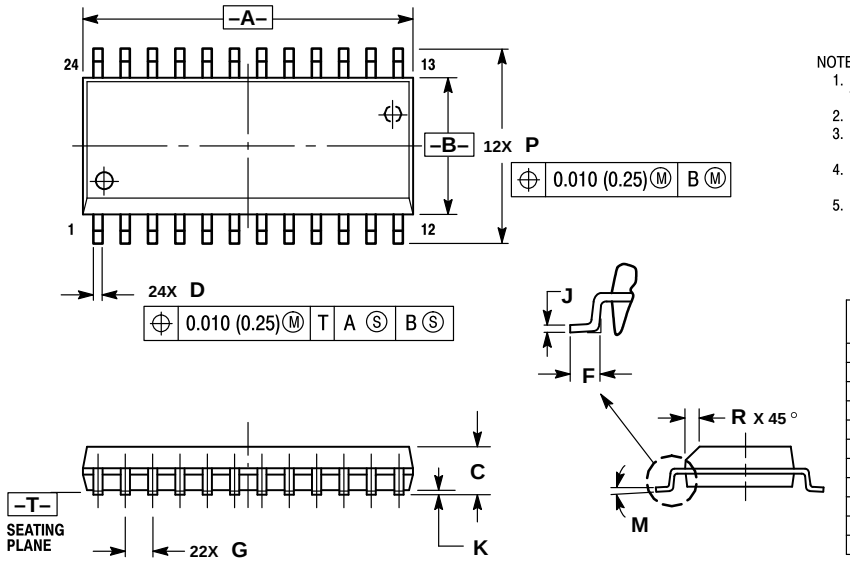
P SUFFIX
PLASTIC PACKAGE
CASE 708–04



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

DW SUFFIX
SOG PACKAGE
CASE 751E–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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