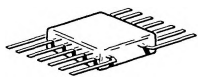
MC1541
MC1441

SENSE AMPLIFIERS

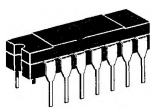
Dual-channel gated sense amplifier with separate wideband differential input amplifiers. Either input can be gated on from saturated logic levels. The sense amplifier features adjustable threshold, saturated logic output levels, and a strobe input that accommodates saturated logic levels. Designed to detect bipolar signals from either of two sense lines. Operates with core memory cycle times less than 0.5 μs.

Typical Amplifier Features:

- Nominal Threshold – 17 mV
- Input Offset Voltage – 1.0 mV typical
- Propagation Delay
  - Input to Gate-Output – 20 ns
  - Input to Amplifier-Output – 10 ns
  - Gate Response Time – 15 ns
  - Strobe Response Time – 15 ns
- Common Mode Input Range – 1.5 Volts
- Differential Mode Input Range
  - With Gate On – 600 mV
  - With Gate Off – 1.5 Volts
- Power Dissipation – 140 mW typical



F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86



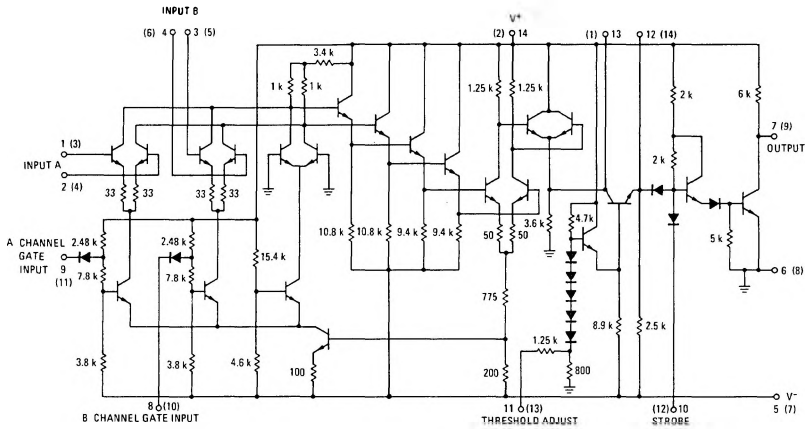
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS

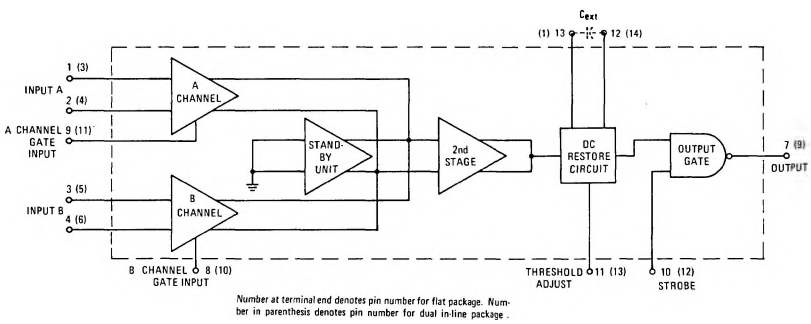
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+10 -10	Vdc Vdc
Differential Input Signal	V_{in}	±5	Vdc
Common Mode Input Voltage	CMV_{in}	±5	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Flat Package Derate above 25°C Ceramic Dual In-Line Package Derate above 25°C	P_D	 500 3.3 600 4.8	 mW mW/°C mW mW/°C
Operating Temperature Range MC1541F, MC1541L MC1441F, MC1441L,	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



Number at terminal end denotes pin number for flat (F) package.
Number in parenthesis denotes pin number for dual in-line ceramic (L) package

LOGIC DIAGRAM



Number at terminal end denotes pin number for flat package. Number in parenthesis denotes pin number for dual in-line package.

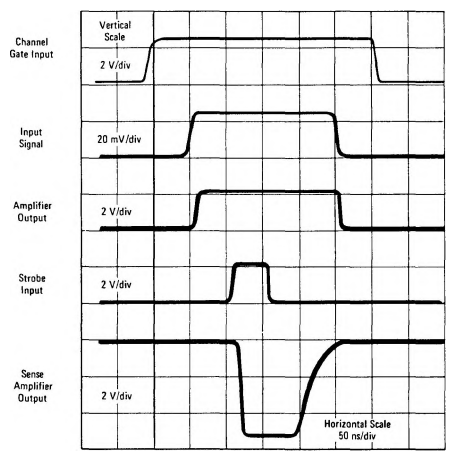


FIGURE 1 – TYPICAL OPERATION

ELECTRICAL CHARACTERISTICS

(V^+ = +5.0 Vdc ± 1%, V^- = -5.0 Vdc ± 1%, $V_{th(pin\ 11)}$ = -5.0 Vdc ± 1%, C_{ext} = 0.01 μF, T_A = 25°C unless otherwise noted)
(T_{low} = -55°C for MC1541 or 0°C for MC1441, T_{high} = +125°C for MC1541 or +75°C for MC1441. Pin numbers referenced in table denote flat package; to ascertain corresponding pin number for dual in-line package refer to the equivalent circuit)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage (T_A = +25°C)	8	V_{th}				mV
($T_{low} \leq T_A \leq T_{high}$) MC1441			14	17	20	
MC1541			13	-	21	
			12	17	22	
Input Offset Voltage	8	V_{io}	-	1.0	6.0	mV
Input Bias Current	9	I_b				μA
($V_1 = V_2 = V_3 = V_4 = 0$)			-	5.0	25	
($V_1 = V_2 = V_3 = V_4 = 0$, $T_A = T_{low}$)			-	-	50	
Input Offset Current	9	I_{io}	-	1.0	2.0	μA
Output Voltage High ($V_1 = V_2 = V_3 = V_4 = 0$, I_{OH} = 200 μA)		V_{OH}	3.0	-	-	Vdc
Output Voltage Low	10	V_{OL}				mVdc
($V_1 = V_2 = V_3 = V_4 = 0$, V_{12} = +5.0 Vdc, I_7 = 10 mAdc)			-	-	350	
(V_{12} = +5.0 Vdc, I_7 = 10 mAdc, $T_A = +T_{high}$)			-	-	400	
Strobe Load Current (V_{10} = 0)		I_S	-	-	1.5	mAdc
Strobe Reverse Current		I_{SR}				μAdc
(V_{10} = +5.0 Vdc)			-	-	2.0	
(V_{10} = +5.0 Vdc, $T_A = T_{high}$)			-	-	25	
Input Gate Voltage Low ($V_1 = V_3$ = 25 mVdc, $V_2 = V_4$ = 0)	11	V_{GL}	-	0.7	-	Vdc
Input Gate Voltage High ($V_1 = V_3$ = 25 mVdc, $V_2 = V_4$ = 0)	11	V_{GH}	-	1.6	-	Vdc
Input Gate Load Current (V_8 or V_9 = 0)		I_G	-	-	2.5	mAdc
Input Gate Reverse Current (V_8 or V_9 = 5.0 Vdc)		I_{GR}				μAdc
(T_A = 25°C)			-	-	2.0	
($T_A = T_{high}$)			-	-	25	
Common Mode Range	13	V_{CM}				Vdc
Input Gate High			-	±1.5	-	
Input Gate Low			-	±1.5	-	
Differential Mode Range	14					
Input Gate High		V_{DH}	-	±600	-	mV
Input Gate Low		V_{DL}	-	±1.5	-	Vdc
Power Dissipation		P_D	-	140	180	mW

SWITCHING CHARACTERISTICS

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Propagation Delay						ns
Input to Amplifier Output	8	t_{IA}				
(V_1 = 25 mV pulse, V_{10} = +2.0 Vdc)			-	10	15	
Input to Output	8	t_{IO}				
(V_1 = 25 mV pulse, V_{10} = +2.0 Vdc)			-	20	30	
Strobe to Output	12	t_{SO}				
($V_1 = V_2 = V_3 = V_4 = 0$, V_{10} = +2.0 V pulse)			-	15	20	
Gate Input to Amplifier Input	11	t_{GI}				
(V_1 = 25 mV pulse, V_9 = 2.0 V pulse)			-	10	15	
Gate Input to Amplifier Output	11	t_{GA}				
(V_1 = 25 mVdc, V_9 = 2.0 V pulse)			-	30	35	
Recovery Time						ns
Differential Mode	14	t_{DR}				
Input Gate High } V_1 or V_3 = 400 mV pulse			-	30	-	
Input Gate Low }			-	0	-	
Common Mode	13	t_{CMR}				
Input Gate High } V_1 or V_3 = 1.5 V pulse			-	15	30	
Input Gate Low }			-	15	30	

FIGURE 2 – TYPICAL INPUT THRESHOLD versus TEMPERATURE

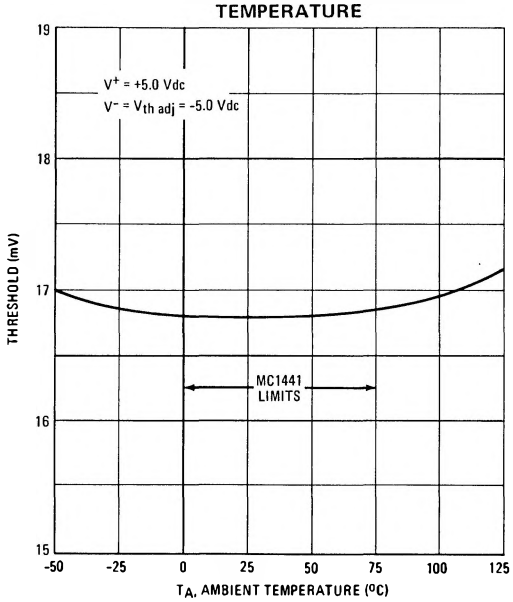


FIGURE 3 – TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST

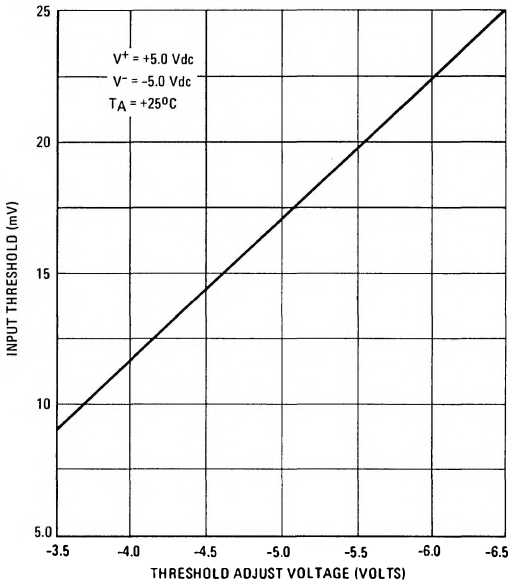


FIGURE 4 – TYPICAL INPUT THRESHOLD versus V-

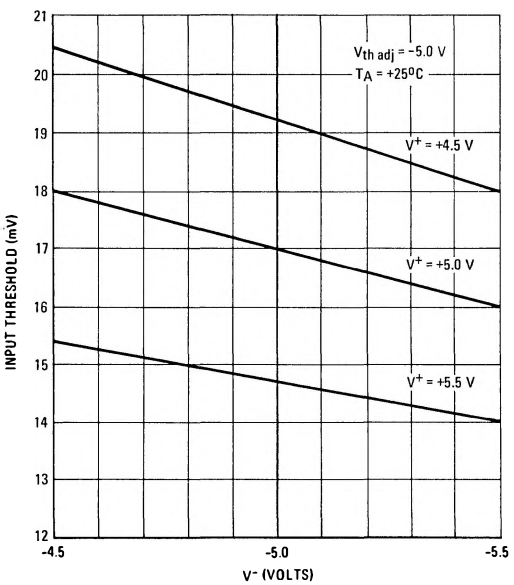


FIGURE 5 – TYPICAL INPUT THRESHOLD versus INPUT PULSE WIDTH

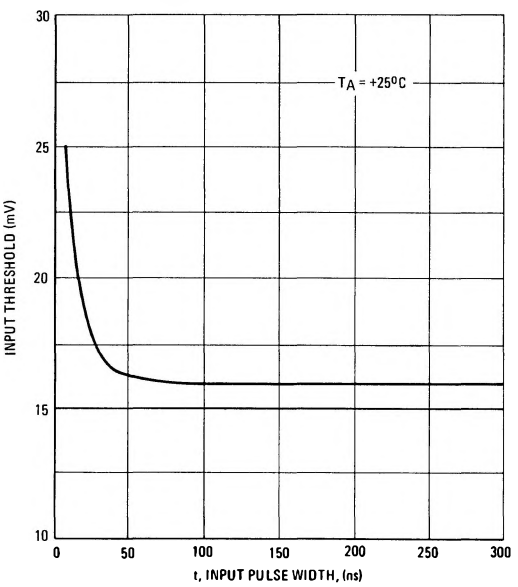


FIGURE 6 – INPUT-OUTPUT TRANSFER CHARACTERISTICS

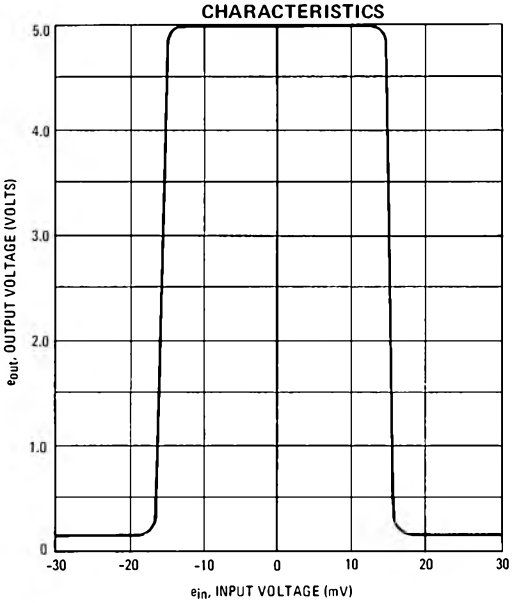


FIGURE 7 – CHANNEL GATE INPUT-AMPLIFIER OUTPUT TRANSFER CHARACTERISTICS

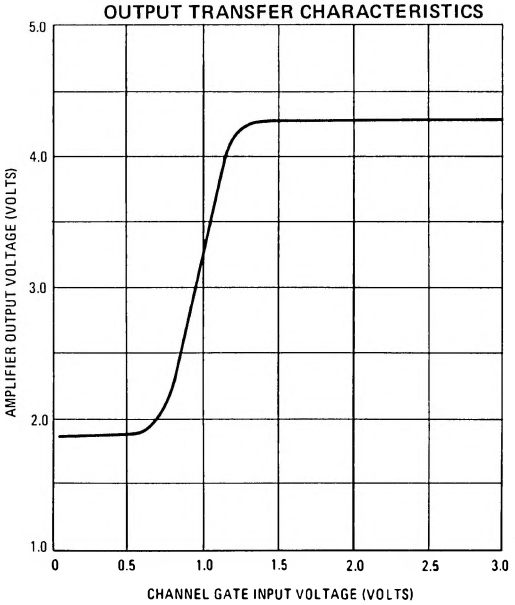
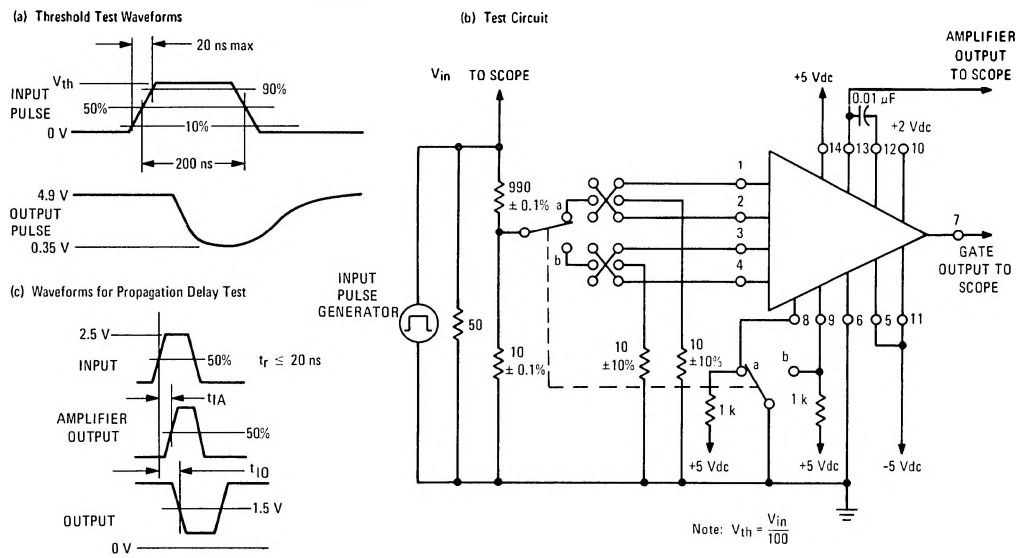
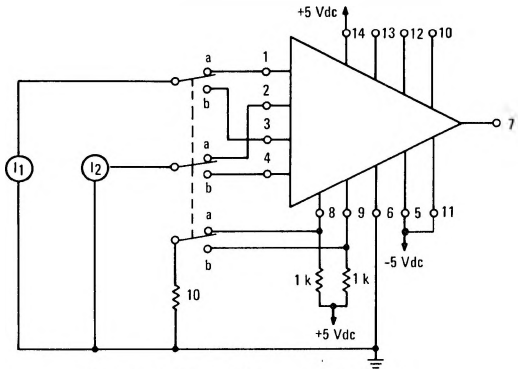


FIGURE 8 – INPUT THRESHOLD FOR OUTPUT VOLTAGE SWING FROM V_{OH} TO V_{OL} PROPAGATION DELAY FROM INPUT TO OUTPUT



Number at terminal end denotes the pin number for flat package only; to ascertain the corresponding pin number for the dual in line packages refer to the circuit schematic on the second page.

FIGURE 9 – INPUT BIAS CURRENT TEST CIRCUIT



$\frac{I_1 + I_2}{2}$ = I_b for "A" channel when switch is in "a" position

= I_b for "B" channel when switch is in "b" position

$|I_1 - I_2| = I_{io}$

FIGURE 10 – OUTPUT VOLTAGE LEVELS

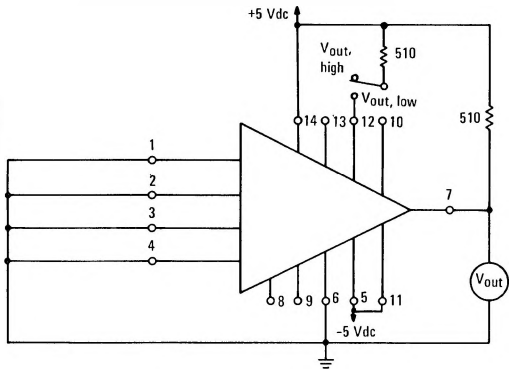
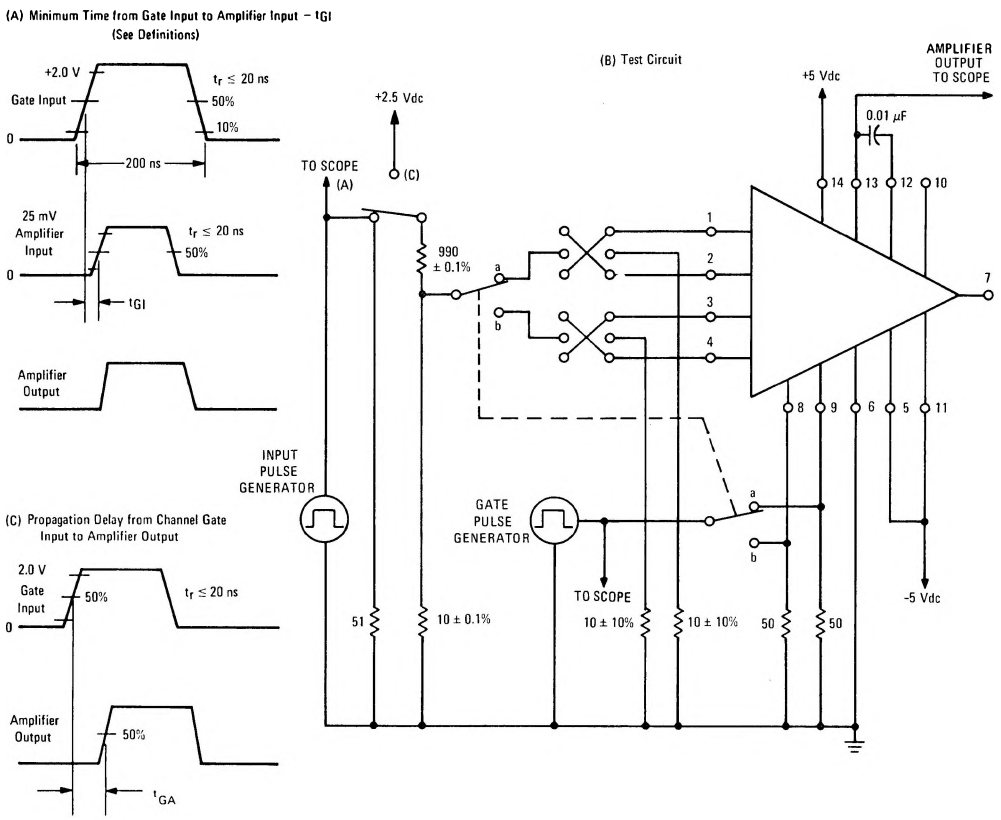


FIGURE 11 – MINIMUM TIME FROM CHANNEL GATE INPUT TO AMPLIFIER INPUT PROPAGATION DELAY FROM CHANNEL GATE INPUT TO AMPLIFIER OUTPUT



(Pin numbers shown on this page denote the pin numbers for the flat package only; to ascertain the corresponding pin numbers for the dual in-line package, refer to the circuit schematic on the second page.)

FIGURE 12 – PROPAGATION DELAY FROM STROBE INPUT TO OUTPUT

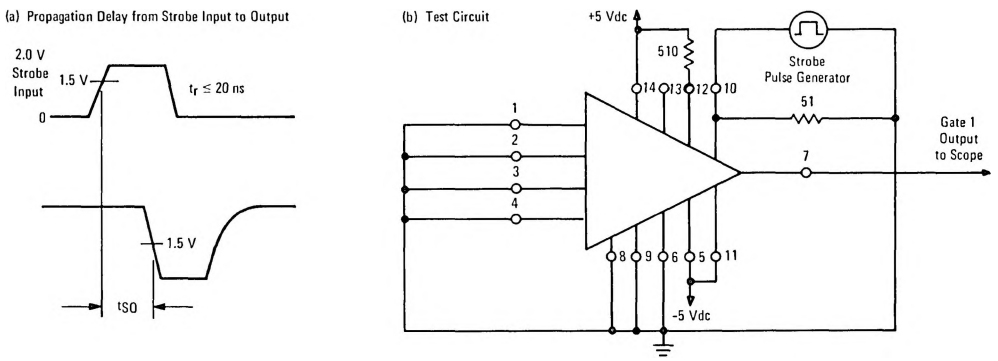


FIGURE 13 – COMMON-MODE RECOVERY AND COMMON-MODE RANGE

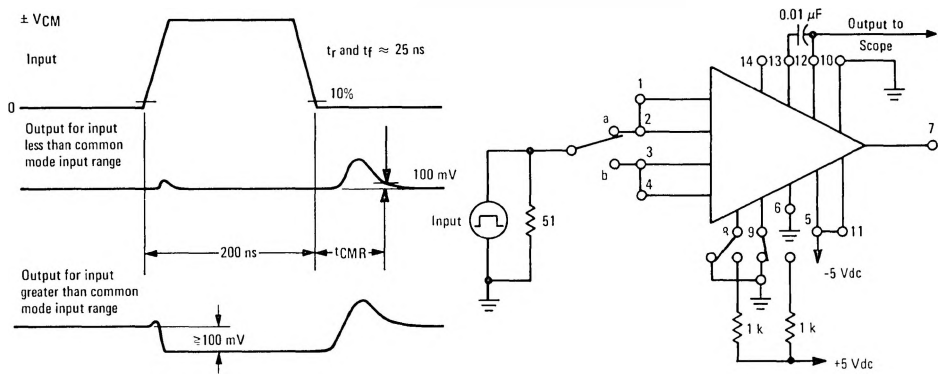
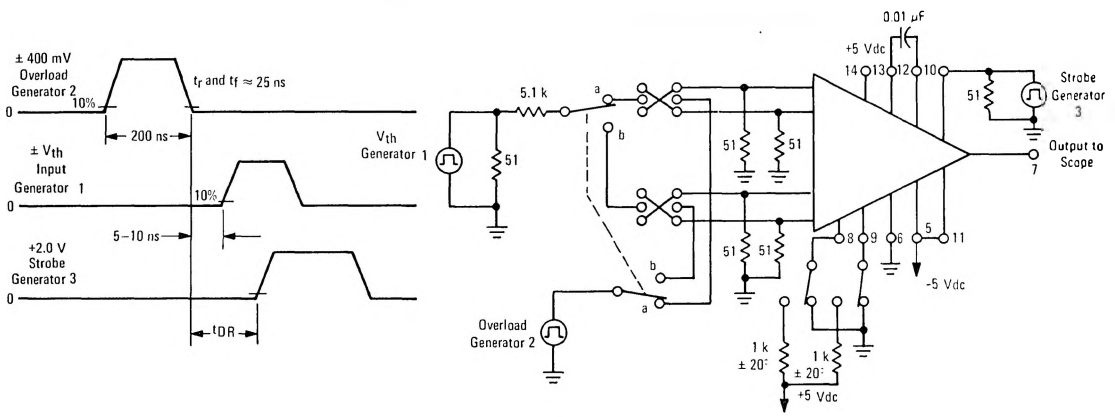


FIGURE 14 – DIFFERENTIAL RECOVERY AND DIFFERENTIAL RANGE



(Pin numbers shown on this page denote the pin numbers for the flat package only; to ascertain the corresponding pin numbers for the dual in-line package , refer to the circuit schematic on the second page.)

DEFINITIONS

Pin numbers referenced in the definitions below denote the flat package only; to ascertain the corresponding pin number for the dual in-line package refer to the circuit schematic.

I_B Input Bias Current — The average input current defined as $(I_1 + I_2 + I_3 + I_4)/4$.

I_G Channel Gate Load Current — The amount of current drain from the circuit when the channel gate input (Pin 8 or 9) is grounded.

I_{GR} Channel Gate Reverse Current — The leakage current when the channel gate input (Pin 8 or 9) is high.

I_{io} Input Offset Current — The difference between amplifier input current values $|I_1 - I_2|$ or $|I_3 - I_4|$.

I_S Strobe Load Current — The amount of current drain from the circuit when the strobe pin is grounded.

I_{SR} Strobe Reverse Current — The leakage current when the strobe input is high.

P_D Power Dissipation — The amount of power dissipated in the unit.

t_{CMR} Common Mode Recovery Time — The time required for the voltage at pin 12 to be within 100 mV of the dc value (after overshoot or ringing) as referenced to the 10% point of the trailing edge of a common mode overload signal.

t_{DR} Differential Recovery Time — The time required for the device to recover from the specified differential input prior to strobe enable as referenced to the 10% point of the trailing edge of an input pulse. The device is considered recovered when the threshold with the overload signal applied is within 1.0 mV of the threshold with no overload input.

t_{GI} Minimum Time Between Channel Gate Input and Signal Input — The minimum time between 50% point of channel gate input (Pin 8 or 9) and 50% point of signal input (Pins 1, 2, 3, or 4) that still allows a full width signal at amplifier output.

t_{GA} Propagation Delay, Channel Gate Input to Amplifier Output — The time required for the amplifier output at pin 13 to reach 50% of its final value as referenced to 50% of the input gate pulse at pin 8 or 9 (Amplifier input = 25 mVdc).

t_{IA} Propagation Delay, Input to Amplifier Output — The time required for the amplifier output pulse at pin 13 to achieve 50% of its final value referenced to 50% of the input pulse at pins 1 and 2 or 3 and 4.

t_{IO} Propagation Delay, Input to Output — The time required for the gate output pulse at pin 7 to reach the 1.5 Volt level as referenced to 50% of the input pulse at pins 1 and 2 or 3 or 4.

t_{SO} Strobe Propagation Delay to Output — The time required for the output pulse at pin 7 to reach the 1.5 Volt level as referenced to the 1.5 Volt level of the strobe input at pin 10.

V_{CM} Maximum Common Mode Input Range — The common mode input voltage which causes the output voltage level of the amplifier to decrease by 100 mV. (This is independent of the channel gate input level.)

V_{DH} Maximum Differential Input Range, Gate Input High — The differential input which causes the input stage to begin saturation.

V_{DL} Maximum Differential Input Range, Gate Input Low — The differential input signal which causes the output voltage level of the amplifier to decrease by 100 mV.

V_{GH} Channel Gate Input Voltage High — Gate pulse amplitude that allows the amplifier output pulse to just reach 100% of its final value. (Amplifier input is set at 25 mVdc).

V_{GL} Channel Gate Input Voltage Low — Gate pulse amplitude that allows the amplifier output to just reach a 100 mV level. (Amplifier input is set at 25 mVdc).

V_{io} Input Offset Voltage — The difference in V_{th} between inputs at pins 1 and 2 or 3 and 4.

V_{OH} Output Voltage High — The high-level output voltage when the output gate is turned off.

V_{OL} Output Voltage Low — The low-level output voltage when the output gate is saturated and the output sink current is 10 mA.

V_{th} Input Threshold — Input pulse amplitude at pins 1, 2, 3 or 4 that causes the output gate to just reach V_{OL}.