19-0953; Rev 0; 12/88

MAXIM

Pin and Resistor Programmed Universal Active Filters

General Description

The MAX265 and MAX266 switched-capacitor active filters are designed for precision filtering applications. Two independent 2nd-order filters implement lowpass, highpass, bandpass, notch or allpass functions. Center or cutoff frequency (f_0) is programmed by 6 pin-strapped inputs and with external resistors while Q is set only with resistors. A variety of filter configurations (Butterworth, Chebyshev, elliptic, etc.) can be realized. Two uncommitted op amps are also included.

The MAX265 operates with center/cutoff frequencies (f_0s) to 40kHz while the MAX266, by employing a lower range of f_{CLK}/f_0 ratios, operates with f_0s to 140kHz. Clock rates to 4MHz are accommodated with either a crystal or external source. The filters operate from ±2.37V to ±6.3V as well as from single +5V power. The MAX265/266 is supplied in 28-pin 0.6" wide DIP and 0.3" wide small outline (SO) packages. All devices are available in commercial, extended, and military temperature ranges.

Applications

Sonar and Avionics Instruments

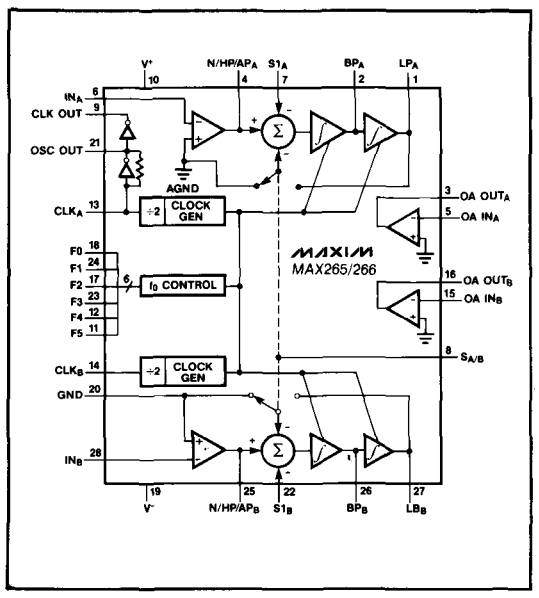
Anti-Aliasing Filters

Digital Signal Processing

Vibration and Audio Analysis

Telecom Test Equipment

Functional Diagram



Features

- ◆ Filter Design Software Available
- ◆ 256 Step Frequency (f_0) Control
- ◆ Resistors Adjust Q and f_0
- ◆ 140kHz Frequency Range (MAX266)
- ◆ ±5V or Single +5V Operation

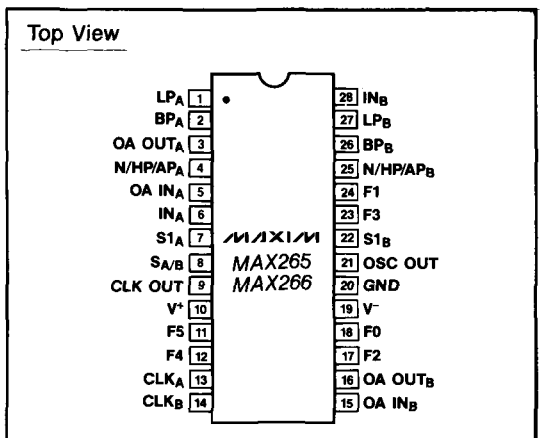
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX265ACPI	0°C to +70°C	Plastic DIP	1%
MAX265BCPI	0°C to +70°C	Plastic DIP	2%
MAX265AEPI	-40°C to +85°C	Plastic DIP	1%
MAX265BEPI	-40°C to +85°C	Plastic DIP	2%
MAX265ACWI	0°C to +70°C	Wide SO	1%
MAX265BCWI	0°C to +70°C	Wide SO	2%
MAX265AMJI	-55°C to +125°C	CERDIP	1%
MAX265BMJI	-55°C to +125°C	CERDIP	2%
MAX266ACPI	0°C to +70°C	Plastic DIP	1%
MAX266BCPI	0°C to +70°C	Plastic DIP	2%
MAX266AEPI	-40°C to +85°C	Plastic DIP	1%
MAX266BEPI	-40°C to +85°C	Plastic DIP	2%
MAX266ACWI	0°C to +70°C	Wide SO	1%
MAX266BCWI	0°C to +70°C	Wide SO	2%
MAX266AMJI	-55°C to +125°C	CERDIP	1%
MAX266BMJI	-55°C to +125°C	CERDIP	2%

* *Packages are 28-pin 0.6" wide DIP and 28-pin 0.3" wide SO (Small Outline).*

Pin Configuration

Top View



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 15V
Input Voltage, any pin ..... V^- -0.3V to V^+ +0.3V
Input Current, any pin ..... ±50mA
Power Dissipation
  Plastic DIP (derate 8.33mW/°C above 70°C) 660mW
  CERDIP (derate 12.5mW/°C above 70°C) 1000mW
  Wide SO (derate 11.8mW/°C above 70°C) 944mW

Operating Temperature
  MAX265/266CxI ..... 0°C to +70°C
  MAX265/266ExI ..... -40°C to +85°C
  MAX265/266MxI ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ±5V 1.5MHz, f_{CLK}/f_0 = 199.49 for MAX265 and 139.80 for MAX266, Filter Mode 1, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				See Table 1		
Maximum Clock Frequency				See Table 1		
f_{CLK}/f_0 Ratio Error (Note 1)	T_A = T_{MIN} to T_{MAX}, Q = 10	MAX265/66A MAX265/66B		±0.2 ±0.2	±1 ±2	%
f_0 Temperature Coefficient				±7		ppm/°C
Q Accuracy (deviation from ideal continuous filter)	T_A = T_{MIN} to T_{MAX}, Q = 10	MAX265/66A MAX265/66B		±1 ±1	±4 ±8	%
Q Temperature Coefficient		MAX265 MAX266		±75 ±20		ppm/°C
DC Low Pass Gain Accuracy		MAX265/66A MAX265/66B		±0.1	±0.125 ±0.2	dB
Gain Temperature Coefficient	Lowpass (at DC)			-10		ppm/°C
DC Offset Voltage LP, BP, N Outputs	T_A = T_{MIN} to T_{MAX}, Mode 1, Q = 10, BP Output	MAX265A MAX265B MAX266A MAX266B			±50 ±100 ±150 ±250	mV
	N Output	MAX265A MAX265B MAX266A MAX266B			±50 ±100 ±400 ±600	
	LP Output	MAX265A MAX265B MAX266A MAX266B			±150 ±300 ±600 ±900	
Offset Voltage Temperature Coefficient	f_{CLK}/f_0 = 100.53, T_A = T_{MIN} to T_{MAX}, Q = 10, LP Output	MAX265 MAX266		-0.25 -1.5		mV/°C
Clock Feedthrough		MAX265 MAX266		±2 ±8		mV
Crosstalk				-70		dB
Wideband Noise (Note 2)	Q = 1, 2nd-Order LP/BP 4th-Order LP 4th-Order BP			See Typ. Oper. Char. 90 100		μV_{RMS}

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ±5V 1.5MHz, f_{CLK}/f_0 = 199.49 for MAX265 and 139.80 for MAX266, Filter Mode 1, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Harmonic Distortion at f_0	Q = 10, V_{IN} = 0.75V_{PP}, BP Output, Gain = 10		-60		dB
Supply Voltage Range	T_A = T_{MIN} to T_{MAX}	±2.37	±5	±6.3	V
Power Supply Current	T_A = T_{MIN} to T_{MAX}		24	29	mA
f_0 Programming Inputs	T_A = T_{MIN} to T_{MAX}, F0-F5 High Threshold Low Threshold	V^+–0.5		 V^-+0.5	V
Clock Inputs	T_A = T_{MIN} to T_{MAX}, CLK_A, CLK_B High Threshold Low Threshold	2.4		 0.8	V
Input Leakage Current	T_A = T_{MIN} to T_{MAX} CLK_A = V^+ or V^- CLK_B = V^+ or V^- F0-F5 = V^+–0.5V or V^-+0.5V F0-F5 = V^+ or V^-		 6 20 5	10 60 200	µA
INTERNAL AMPLIFIERS					
Output Voltage Swing	T_A = T_{MIN} to T_{MAX}, 10kΩ load		±4.75		V
Output Short Circuit Current	Source Sink		50 2		mA
Power Supply Rejection Ratio	0Hz to 10kHz		-70		dB
Gain Bandwidth Product			2.5		MHz
Slew Rate			6		V/µs

ELECTRICAL CHARACTERISTICS (for V± = ±2.5V ±5%)

(V^+ = +2.37V, V^- = -2.37V, CLK_A = CLK_B = ±2.5V 1MHz, f_{CLK}/f_0 = 199.49 for MAX265 and 139.80 for MAX266, Filter Mode 1, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				(Note 3)		
Maximum Clock Frequency				(Note 3)		
f_{CLK}/f_0 Ratio Error (Notes 1, 4)	T_A = T_{MIN} to T_{MAX}, Q = 10	MAX26XA MAX26XB		±0.1 ±0.1	1 2	%
Q Accuracy (deviation from ideal continuous filter, Note 4)	T_A = T_{MIN} to T_{MAX}, Q = 10	MAX265/66A MAX265/66B			±4 ±8	%
Output Signal Swing	All Outputs			±2		V
Power Supply Current	*CMOS Level Logic Inputs* T_A = T_{MIN} to T_{MAX}			10		mA

Note 1: f_{CLK}/f_0 accuracy is tested at 100.53, 103.67, 106.81, 113.1, 125.66, 150.8, and 199.49 on the MAX265, and at 40.84, 43.98, 47.12, 53.41, 65.97, 91.11, and 139.8 on the MAX266.

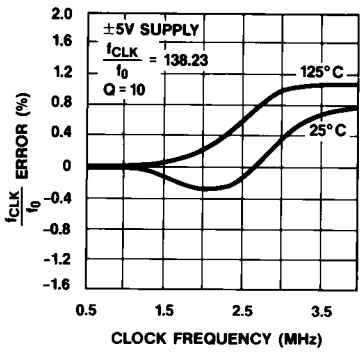
Note 2: Output noise is measured with an RC smoothing filter at 4 x f_0 to remove clock feedthrough.

Note 3: At ±2.5V supplies, the f_0 range and maximum clock frequency are typically 75% of the values listed in Table 1.

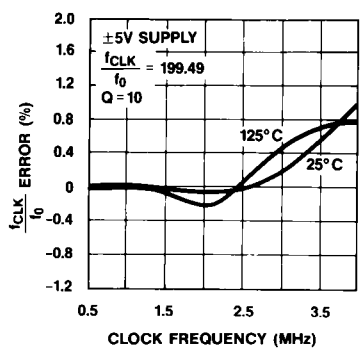
Note 4: f_{CLK}/f_0 accuracy is a function of the accuracy of internal capacitor ratios in the filter. No increase in error is expected at ±2.5V as compared to ±5V, however, this is only tested to the extent indicated by the MIN or MAX limits.

Typical Operating Characteristics

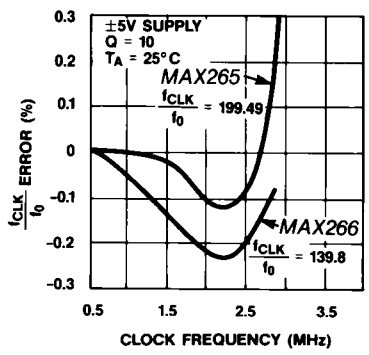
MAX266 f_0 ERROR vs CLOCK FREQ. (MODE 1)



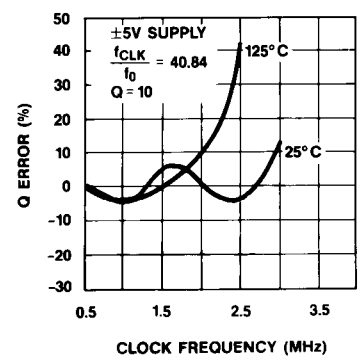
MAX265 f_0 ERROR vs CLOCK FREQ. (MODE 1)



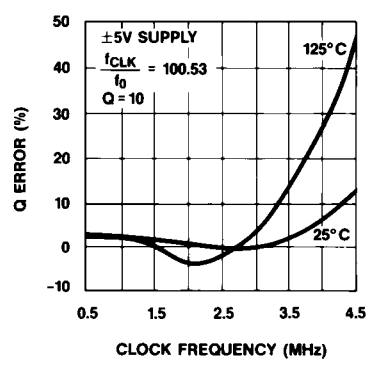
f_0 ERROR vs CLOCK FREQ. (MODE 3)



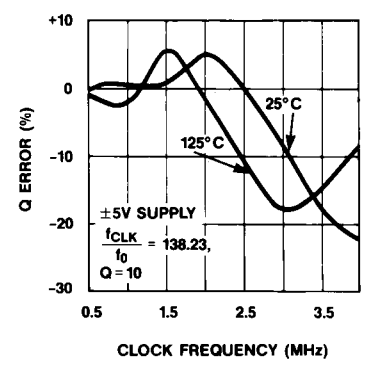
MAX266 Q ERROR vs CLOCK FREQ. (MODE 1)



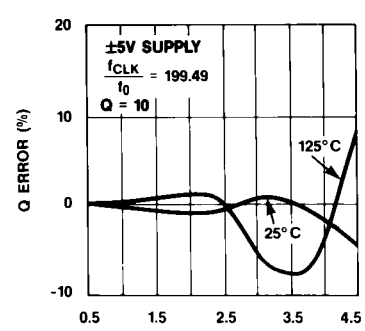
MAX265 Q ERROR vs CLOCK FREQ. (MODE 1)



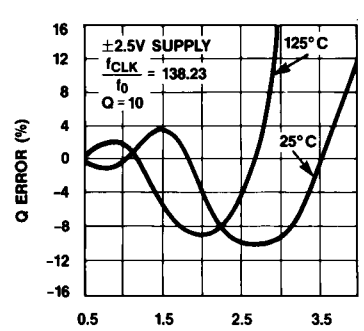
MAX266 Q ERROR vs CLOCK FREQ. (MODE 1)



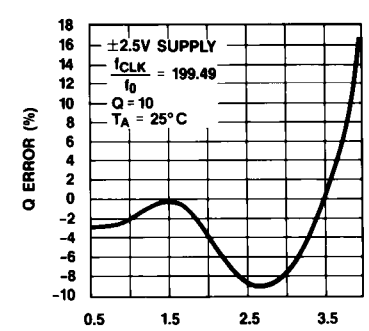
MAX265 Q ERROR vs CLOCK FREQ. (MODE 1)



MAX266 Q ERROR vs CLOCK FREQ. (MODE 1)

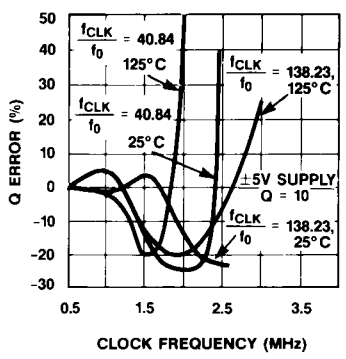


MAX265 Q ERROR vs CLOCK FREQ. (MODE 1)

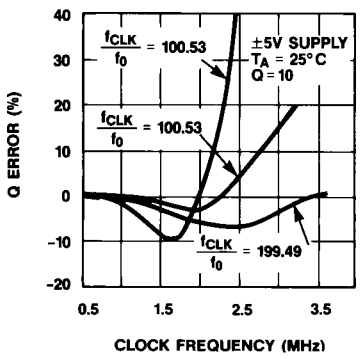


Typical Operating Characteristics (Continued)

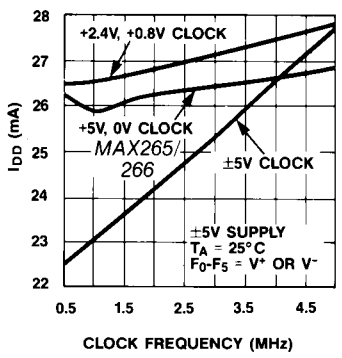
MAX266 Q ERROR vs CLOCK FREQ. (MODE 3)



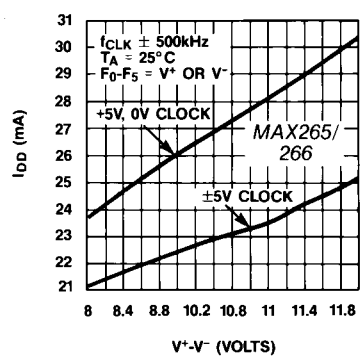
MAX265 Q ERROR vs CLOCK FREQ. (MODE 3)



SUPPLY CURRENT vs CLOCK FREQ.



SUPPLY CURRENT vs VOLTAGE



Wideband RMS Noise (dB ref. to 2.47V_{RMS}, 7V_{p-p}), ±5V Operation

Mode	Q = 1			Q = 8			Q = 64		
	LP	BP	N/HP/AP	LP	BP	N/HP/AP	LP	BP	N/HP/AP
1	-84	-90	-84	-80	-82	-85	-72	-73	-85
2	-88	-90	-88	-84	-82	-84	-77	-73	-76
3	-84	-90	-88	-80	-82	-82	-73	-73	-74
4	-83	-89	-84	-79	-81	-85	-71	-73	-85

Notes:
1. f_{CLK} = 1MHz
2. f_{CLK}/f_0 ratio programmed at N = 63 (see Table 2)
3. Clock feedthrough is removed with an RC lowpass at $4f_0$, i.e. R = 3.9kΩ, C = 2000pF for MAX265

Noise Spectral Distribution (MAX265, f_{CLK} = 1MHz, dB ref. to 2.47V_{RMS}, 7V_{p-p})

Measurement Bandwidth	Q=1	Q=8	Q=64
Wideband	-84	-80	-72
3kHz	-87	-87	-86
C Message Weighted	-93	-93	-93

Table 1. Typical Clock Center Frequency Limits

PART	Q	MODE	f_{CLK}	f_0
MAX265	1	1	40Hz-4.0MHz	0.4Hz-40kHz
	1	2	40Hz-4.0MHz	0.4Hz-57kHz
	1	3	40Hz-4.0MHz	0.4Hz-40kHz
	1	4	40Hz-4.0MHz	0.4Hz-40kHz
	10	1	40Hz-3.0MHz	0.4Hz-30kHz
	10	2	40Hz-2.1MHz	0.4Hz-30kHz
	10	3	40Hz-2.1MHz	0.4Hz-21kHz
	10	4	40Hz-3.0MHz	0.4Hz-30kHz
	64	1	40Hz-2.5MHz	0.4Hz-25kHz
	90	2	40Hz-1.2MHz	0.4Hz-18kHz
	64	3	40Hz-1.2MHz	0.4Hz-12kHz
	64	4	40Hz-2.5MHz	0.4Hz-25kHz

PART	Q	MODE	f_{CLK}	f_0
MAX266	1	1	40Hz-4.0MHz	0.4Hz-100kHz
	1	2	40Hz-4.0MHz	0.4Hz-140kHz
	1	3	40Hz-4.0MHz	0.4Hz-100kHz
	1	4	40Hz-4.0MHz	0.4Hz-100kHz
	10	1	40Hz-2.5MHz	0.4Hz-60kHz
	10	2	40Hz-1.5MHz	0.4Hz-50kHz
	10	3	40Hz-1.5MHz	0.4Hz-37kHz
	10	4	40Hz-2.5MHz	0.4Hz-60kHz
	64	1	40Hz-1.4MHz	0.4Hz-35kHz
	90	2	40Hz-1.0MHz	0.4Hz-35kHz
	64	3	40Hz-1.0MHz	0.4Hz-30kHz
	64	4	40Hz-1.4MHz	0.4Hz-35kHz

Table 2. f_{CLK}/f_0 Program Table
(This table assumes Mode 1, R1 = R2 = R4, and R3 = 10xR2. The f_{CLK}/f_0 ratios listed below are scaled by resistors in other operating modes. See Figures 5 through 20.)

f_{CLK}/f_0 RATIO		PROGRAM CODE						
MAX265	MAX266	N	F5	F4	F3	F2	F1	F0
100.53	40.84	0	0	0	0	0	0	0
102.10	42.41	1	0	0	0	0	0	1
103.67	43.98	2	0	0	0	0	1	0
105.24	45.55	3	0	0	0	0	1	1
106.81	47.12	4	0	0	0	1	0	0
108.38	48.69	5	0	0	0	1	0	1
109.96	50.27	6	0	0	0	1	1	0
111.53	51.84	7	0	0	0	1	1	1
113.10	53.41	8	0	0	1	0	0	0
114.67	54.98	9	0	0	1	0	0	1
116.24	56.55	10	0	0	1	0	1	0
117.81	58.12	11	0	0	1	0	1	1
119.38	59.69	12	0	0	1	1	0	0
120.95	61.26	13	0	0	1	1	0	1
122.52	62.83	14	0	0	1	1	1	0
124.09	64.40	15	0	0	1	1	1	1
125.66	65.97	16	0	1	0	0	0	0
127.23	67.54	17	0	1	0	0	0	1
128.81	69.12	18	0	1	0	0	1	0
130.38	70.69	19	0	1	0	0	1	1
131.95	72.26	20	0	1	0	1	0	0
133.52	73.83	21	0	1	0	1	0	1
135.08	75.40	22	0	1	0	1	1	0
136.66	76.97	23	0	1	0	1	1	1
138.23	78.53	24	0	1	1	0	0	0
139.80	80.11	25	0	1	1	0	0	1
141.37	81.68	26	0	1	1	0	1	0
142.94	83.25	27	0	1	1	0	1	1
144.51	84.82	28	0	1	1	1	0	0
146.08	86.39	29	0	1	1	1	0	1
147.65	87.96	30	0	1	1	1	1	0
149.23	89.54	31	0	1	1	1	1	1

f_{CLK}/f_0 RATIO		PROGRAM CODE						
MAX265	MAX266	N	F5	F4	F3	F2	F1	F0
150.80	91.11	32	1	0	0	0	0	0
152.37	92.68	33	1	0	0	0	0	1
153.98	94.25	34	1	0	0	0	1	0
155.51	95.82	35	1	0	0	0	1	1
157.08	97.39	36	1	0	0	1	0	0
158.65	98.96	37	1	0	0	1	0	1
160.22	100.53	38	1	0	0	1	1	0
161.79	102.10	39	1	0	0	1	1	1
163.36	102.67	40	1	0	1	0	0	0
164.93	105.24	41	1	0	1	0	0	1
166.50	106.81	42	1	0	1	0	1	0
168.08	108.38	43	1	0	1	0	1	1
169.65	109.96	44	1	0	1	1	0	0
171.22	111.53	45	1	0	1	1	0	1
172.79	113.10	46	1	0	1	1	1	0
174.36	114.66	47	1	0	1	1	1	1
175.93	116.24	48	1	1	0	0	0	0
177.50	117.81	49	1	1	0	0	0	1
179.07	119.38	50	1	1	0	0	1	0
180.64	120.95	51	1	1	0	0	1	1
182.21	122.52	52	1	1	0	1	0	0
183.78	124.09	53	1	1	0	1	0	1
185.35	125.66	54	1	1	0	1	1	0
186.92	127.23	55	1	1	0	1	1	1
188.49	128.81	56	1	1	1	0	0	0
190.07	130.38	57	1	1	1	0	0	1
191.64	131.95	58	1	1	1	0	1	0
193.21	133.52	59	1	1	1	0	1	1
194.78	135.09	60	1	1	1	1	0	0
196.35	136.66	61	1	1	1	1	0	1
197.92	138.23	62	1	1	1	1	1	0
199.49	139.80	63	1	1	1	1	1	1

Note 1: For the MAX265, $f_{CLK}/f_0 = 1.5708(64+N)$ in Mode 1. N varies from 0 to 63.
Note 2: For the MAX266, $f_{CLK}/f_0 = 1.5708(26+N)$ in Mode 1. N varies from 0 to 63.

Pin and Resistor Programmed Universal Active Filters

Pin Description

PIN #	NAME	FUNCTION
10	V^+	Positive supply voltage
19	V^-	Negative supply voltage
20	GND	Analog Ground. Connect to the system ground for ± supplies or to mid-supply for single supply operation. GND should be well bypassed in single supply applications.
13	CLK_A	Input to the oscillator and clock input to section A. This clock is internally divided by 2.
14	CLK_B	Clock input to filter B. This clock is internally divided by 2.
9	CLK OUT	Clock Output for crystal and R-C oscillator operation.
21	OSC OUT	Connects to crystal or R-C for self-clocked operation.
6,28	IN_A,IN_B	Filter inputs

PIN #	NAME	FUNCTION
2,26	BP_A,BP_B	Bandpass outputs
1,27	LP_A,LP_B	Lowpass outputs
4,25	N/HP/$AP_{A,B}$	Notch/Highpass/Allpass outputs
8	$S_{A/B}$	When $S_{A/B}$ is high, one filter summing node is tied to the LP output. When $S_{A/B}$ is low, the summing node is grounded. See Mode diagrams (Figures 5-20) for $S_{A/B}$ connections.
7,22	$S1_A$,$S1_B$	Auxiliary inputs to summing node in A and B filter. They receive feedback signals in various filter modes.
18,24,17 23,12,11	F0-F5	Programming inputs for f_{CLK}/f_0 ratio
3,16	OP OUT	Output of op amps A and B
5,15	OP IN	Inverting input of op amps A and B

Introduction

The two universal 2nd-order filter sections contained in each MAX265/266 are shown in the functional diagram on the front page of this data sheet. f_{CLK}/f_0 programming inputs (F0-F5) are shared by both halves of the filter, however, each half's f_0 may still be adjusted independently using external resistors. The Q of each filter section is also independently adjusted with external resistors.

The MAX266 uses a lower range of sampling (f_{CLK}/f_0) ratios than the MAX265 to allow higher signal bandwidths and a wider f_0 programming range. A side effect is that the MAX266's reduced f_{CLK}/f_0 ratios result in somewhat more deviation from ideal continuous filter parameters than with the MAX265, however, these differences can be compensated for by using the graphs in Figure 23 (See "Applications Hints") or with Maxim's filter design software.

In all MAX26X series filters, the internal sample rate is one half the input clock rate (CLK_A or CLK_B) due to an internal division by two. All data sheet data, tables, and discussions concerning the filter clock refer to the frequency at the CLK_A or CLK_B input, i.e., twice the internal sample rate.

Filter Design Software

Maxim provides software programs to help speed the transition from frequency response design requirements to working hardware. A series of programs are available, including:

Program PZ. Given the requirements, such as center frequency, Q, passband ripple, and stopband attenuation, PZ calculates the pole frequencies, Q's, zeros, and the number of stages needed.

Program RP. Given the specs of the individual 1st and 2nd-order stages (from PZ), RP calculates the necessary resistor values for the following operating modes: 1, 2, 3, 3A, 4, 5, 6A, 6B.

Program RPCHECK. Given any set of programming resistors, the clock rate, and the f_{CLK}/f_0 ratio, RPCHECK calculates the actual performance of a stage for all of the modes. The sensitivity of a design to resistor tolerance can then be tested.

Program FR. When a design of one or more stages is completed, FR checks the response of the final cascaded assembly. The output frequency response can be compared with that expected from PZ.

Quick Look Design Procedure

MAX26X series filters, with Maxim's filter design software, greatly simplify the design procedure for many active filters. Most designs can be realized using the steps in this section. If the filter software is not used, or if the complexity is beyond the scope of this section, refer to the remainder of this data sheet for further applications details.

Step 1—Filter Design

Starting with the design program "PZ", determine what type of filter is needed. PZ helps determine the polynomial (Butterworth, Chebyshev, etc.) and the number of poles for the optimum choice. The program also plots the frequency response and finds the pole (and zero) frequencies and Q values for each 2nd-order section. Each MAX265/66 contains two such sections and devices are cascaded in higher order filters.

Step 2—Select a Filter Mode

The next step is to determine the optimum filter operating mode. See the "Operating Modes" section for descriptions and advantages of each mode. The descriptions are organized by filter type (lowpass, bandpass, etc.) to simplify mode selection. Modes can be mixed in cascaded filters.

Step 3—Programming and Resistor Values

Starting with the f_0 and Q values from PZ in Step 1, proceed to the RP design program. RP picks the program codes for f_{CLK}/f_0 which are listed in Table 2. The program also picks values for the external resistors for the most common filter modes. These are Mode 1, 2, 3, 3A, 4, 5, 6A, and 6B.

Detailed Description

f_0 Programming

Each 2nd-order filter section has its own clock input, however, pin limitations require that the six f_{CLK}/f_0 pin-programming inputs (F0-F5) be shared by both sections. Besides the programming inputs, each section's f_0 is also controlled by the filter clock and with external resistors. The degree to which these resistors tune f_0 depends on the filter's operating mode.

Oscillator and Clock Inputs

The clock circuitry of the MAX265/266 operates with a crystal, external clock source, or a resistor capacitor network (RC) as shown in Figure 1. The clock rate, f_{CLK}, nominally equals 0.45/RC when an RC network is used, however, this relationship is not guaranteed. Consequently an RC clock is not recommended for precise filter applications.

The duty cycle of an external clock input at CLK_A and CLK_B is unimportant because this signal is internally divided by two to generate the sampling clock for each filter section. It is important to note that this internal division also halves the sample rate when considering aliasing and other sampled system phenomenon.

Filter Operating Modes

The MAX265/266's filter sections can be configured in several basic "Modes" as selected by the $S_{A/B}$, $S1_A$, and $S1_B$ inputs and external resistors. Figures 5 through 20 show symbolic representations of the MAX265/266 filter modes. Only one 2nd-order section is shown in each case. The f_0, f_N (notch), Q, and various output gains for each mode are shown in each figure. Advantages of various modes for each filter type are discussed in the following sections. Table 1 lists typical f_0 and f_{CLK} ranges for each mode at various Qs.

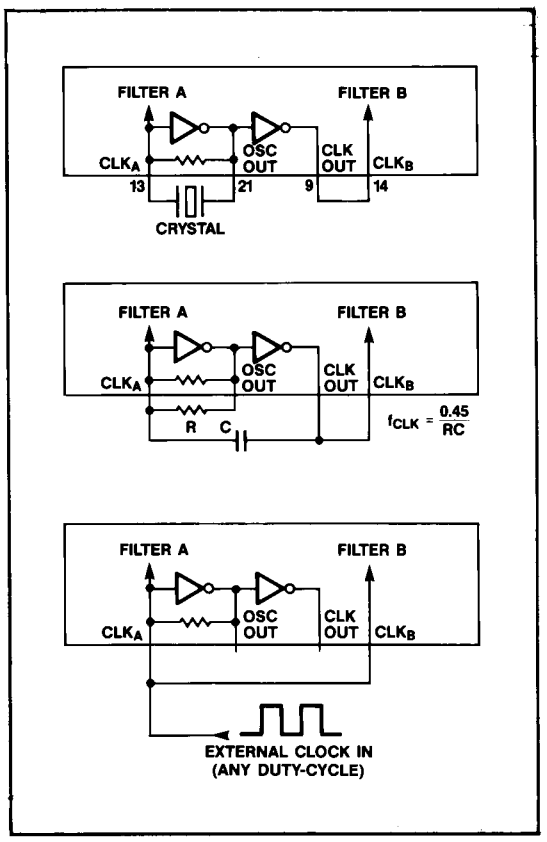


Figure 1. Clock Input Connections

Modes for Bandpass and Lowpass Filters

MODE 1 and 1A-1D (Figures 5-9) are useful when implementing all-pole lowpass and bandpass filters such as Butterworth, Chebyshev, and Bessel. These modes support the highest f_0s because the input amplifier is outside the filter's resonant loop. Mode 1A, with only two resistors, is the simplest implementation of lowpass and bandpass filters. In 1A there are two BP outputs, one of these (BP2) has unity gain regardless of resistor values.

In Mode 1, 1A, and 1D, f_0 is controlled by f_{CLK} and the f_{CLK}/f_0 program inputs (F0-F5) but is not tuned with resistors. Mode 1B and 1C allow resistor tuning in addition to programming. f_0 can be increased from the programmed value in 1B and decreased in 1C. Mode 1D is slightly simpler for bandpass and lowpass filters but only for Qs of one or more.

MODE 2, 2A, and 2B (Figures 10-12) exhibit the lowest noise for lowpass filters (see Typical Operating Characteristics).

MODE 3 and 3A (Figures 13, 14) allow the most flexible tuning of f_0 and f_N for pole-zero filters such as elliptics and is recommended when the f_0s are comfortably within the ranges listed in Table 1.

In Mode 3A, the HP and LP outputs are summed either by the input amplifier of the next filter stage, or by one of the other on-chip amplifiers, to form a notch. Resistors control the notch/zero (f_N) location which can be tuned above or below f_0.

Although Mode 3A's output is labeled "Notch", it is used for cascaded bandpass, lowpass, and highpass filters as well (see Figure 11).

BANDPASS EQUATIONS:

$$G(s) = H_{OBP} \frac{s(\omega_o/Q)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OPB} = Bandpass gain at $\omega = \omega_o$

$f_0 = \omega_o/2\pi$ = The center frequency of the complex pole pair. Input-output phase shift is -180° at f_0.

Q = The quality factor of the complex pole pair. Also the ratio of f_0 to -3dB bandwidth of the second-order bandpass response.

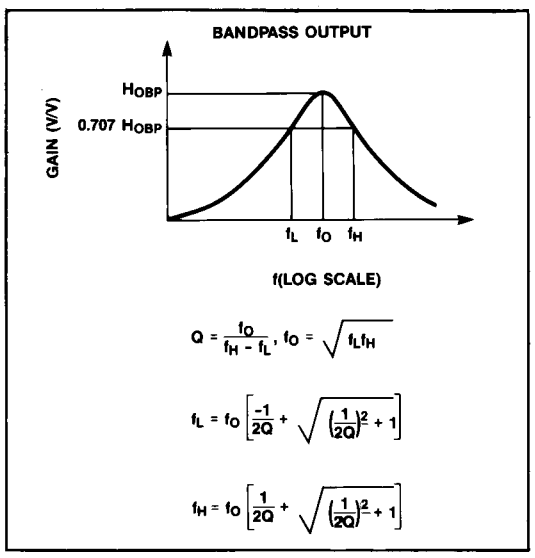


Figure 2. Bandpass Response

LOWPASS EQUATIONS:

$$G(s) = H_{OLP} \frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OLP} = Lowpass gain at DC

$f_0 = \omega_o/2\pi$

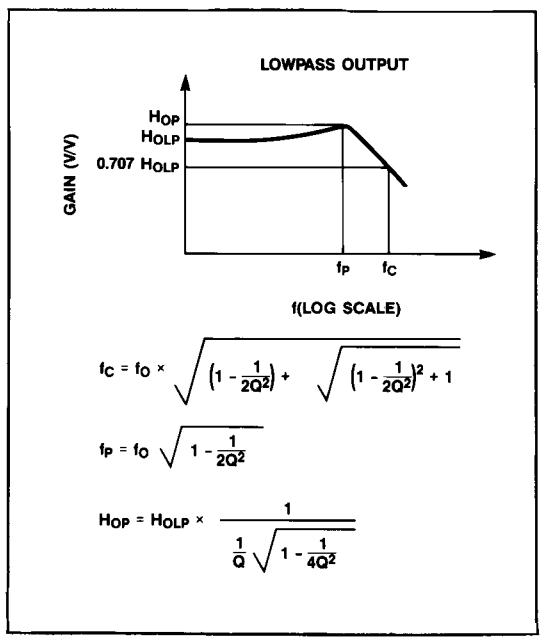


Figure 3. Lowpass Response

Modes For Highpass Filters

MODE 2 (Figure 10) can be used for elliptic highpass filters using the "N" output. Here f_N (the zero frequency) is less than f_0.

MODE 3 and 3A (Figures 13, 14) provide a highpass output. Mode 3 is preferred for all-pole filters such as Bessel, Butterworth and Chebyshev. In 4th-order and greater filters with zeros such as elliptics, Mode 3A sections can be cascaded (using the "Notch" output, Figure 11).

Pin and Resistor Programmed Universal Active Filters

HIGHPASS EQUATIONS:

$$G(s) = H_{OLP} \frac{s^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OHP} = Highpass output gain as f approaches $f_{CLK}/4$

$f_0 = \omega_o/2\pi$

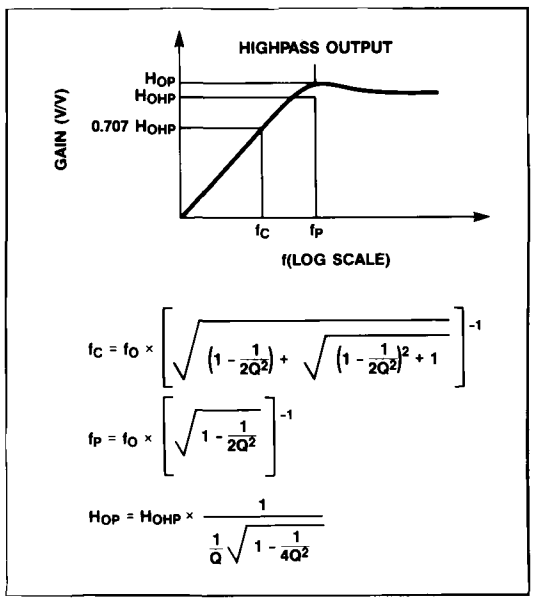


Figure 4. Highpass Response

Modes for Notch Filters

MODE 1, 1B, and 1C (Figures 5, 7, 8) work well in 2nd-order notches. These modes have the highest bandwidth and are the most basic since the notch (f_N) and f_0 occur at the same point. In Mode 1, f_N is set only by the clock and the programmed f_{CLK}/f_0 ratio. In Mode 1B and 1C, f_N can be tuned with resistors, but is still equal to f_0.

MODE 2, 2A, and 2B (Figures 10, 11, 12) are useful when cascading 2nd-order functions to form high-order notches. f_N may be independently tuned with resistors to a frequency below f_0. These modes are slower than Mode 1 notches but also exhibit lower noise.

MODE 3A (Figure 14) allows the most flexible tuning of f_0 and f_N for pole-zero filters such as elliptics. Resistor ratios control the notch location which can be tuned above or below f_0. In Mode 3A, highpass and lowpass outputs are summed by the input amplifier of the next filter stage, or by one of the other on-chip amplifiers, to form a notch.

NOTCH EQUATIONS:

$$G(s) = H_{ON2} \frac{s^2 + \omega_n^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{ON2} = Notch output gain as f approaches $f_{CLK}/4$

H_{ON1} = Notch output gain as f approaches DC

$f_n = \omega_n/2\pi$

Modes for Allpass Filters

MODE 4 and 4A (Figures 15, 16) provide the only allpass output, i.e., a nearly flat amplitude response and linear phase shift with frequency (constant time delay). The numerator complex zero pair and denominator complex pole pair have the same center frequency and Q so that the magnitude response is a straight line. In Mode 4, f_0 is controlled by the clock and f_{CLK}/f_0 programming while in Mode 4A, f_0 can also be tuned with resistors.

MODE 5 (Figure 17) places the center frequency of the numerator complex zero pair (f_Z), at a different frequency from f_0. The magnitude response therefore has a notch at f_Z which is proportional to the numerator's Q.

ALLPASS EQUATIONS:

$$G(s) = H_{OAP} \frac{s^2 - s(\omega_o/Q) + \omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = Allpass output gain for $DC < f < f_{CLK}/4$

$f_0 = \omega_o/2\pi$

Modes for 1st-Order Filters

MODE 6A, 6B, and 6C (Figures 18-20) form simple tunable single-pole functions. These can be used separately or added to 2nd-order functions for cascaded odd-order filters. Lowpass, highpass, and allpass outputs are available.

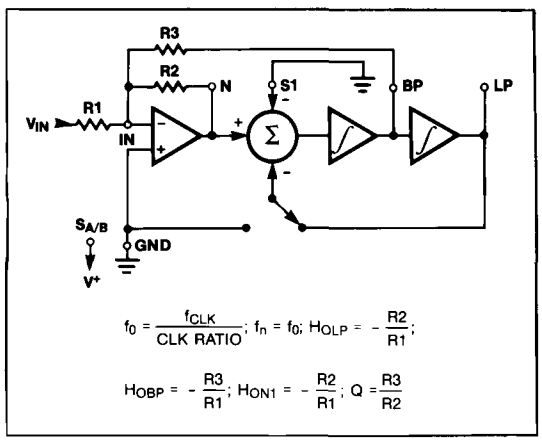
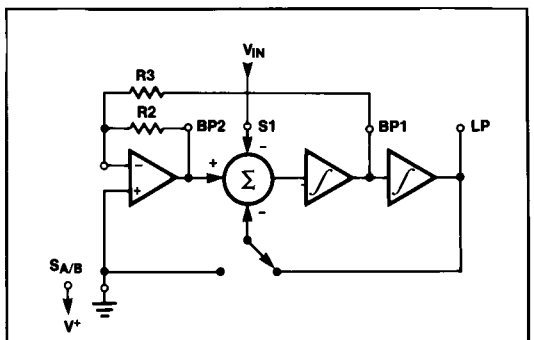


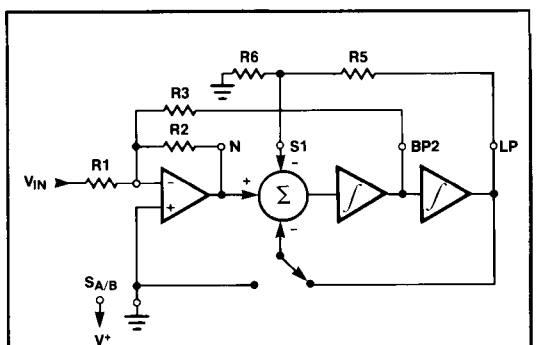
Figure 5. Mode 1: 2nd-Order Filter Providing Notch, Bandpass, Lowpass



$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}};\ Q = \frac{R3}{R2};\ H_{OBP1} = -\frac{R3}{R2};$$

$$H_{OBP2} = 1(\text{NONINVERTING});\ H_{OLP} = -1$$

Figure 6. Mode 1a: 2nd-Order Filter Providing Bandpass, Lowpass

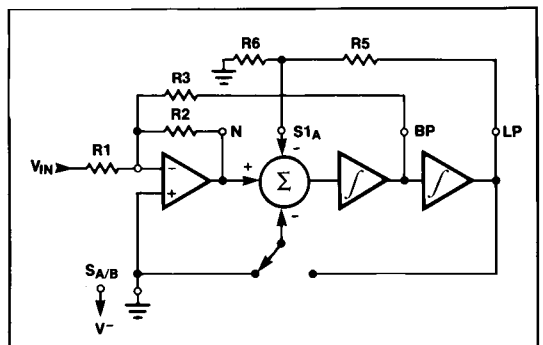


$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{1 + \frac{R6}{R5 + R6}};\ f_n = f_0;\ Q = \frac{R3}{R2}\sqrt{1 + \frac{R6}{R5 + R6}}$$

$$H_{ON1}(f \to 0) = H_{ON2}\left(f \to \frac{f_{CLK}}{4}\right) = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};$$

$$H_{OLP} = \frac{-R2/R1}{1 + R6/(R5 + R6)};\ R5 < 5k\Omega$$

Figure 7. Mode 1b: 2nd-Order Filter Providing Notch, Bandpass, Lowpass

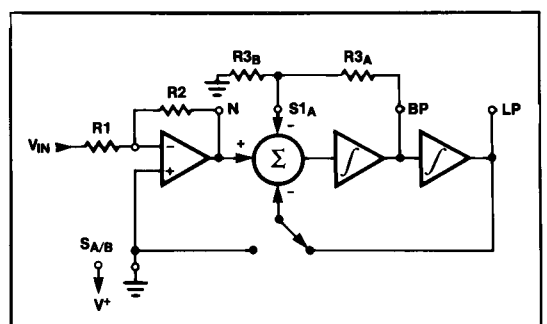


$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{\frac{R6}{R5 + R6}};\ f_n = f_0;\ Q = \frac{R3}{R2}\sqrt{\frac{R6}{R5 + R6}};$$

$$H_{ON1}(f \to 0) = H_{ON2}\left(f \to \frac{f_{CLK}}{4}\right) = -\frac{R2}{R1};\ H_{OLP} = \frac{-R2/R1}{R6/(R5 + R6)};$$

$$H_{OBP} = -\frac{R3}{R1};\ R5 < 5k\Omega$$

Figure 8. Mode 1c: 2nd-Order Filter Providing Notch, Bandpass, Lowpass

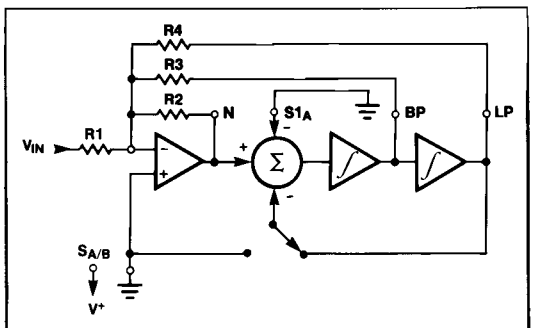


$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}};\ Q = 1 + \frac{R3_A}{R3_B};\ H_{OBP} = -\frac{R2}{R1} \times Q$$

$$H_{OLP} = -\frac{R2}{R1};\ V_N = -\frac{R2}{R1}V_{IN}$$

Figure 9. Mode 1d: 2nd-Order Filter Providing Bandpass and Lowpass for Qs Greater or Equal to 1

Pin and Resistor Programmed Universal Active Filters

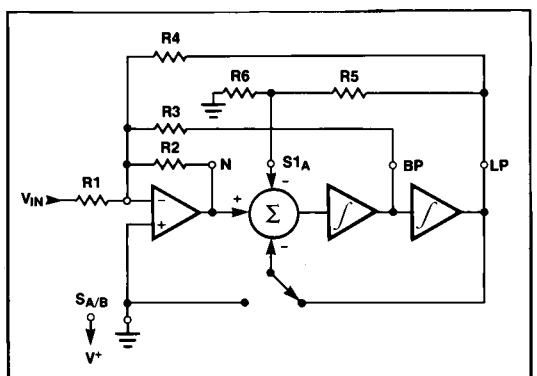


$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{1 + \frac{R2}{R4}};\quad f_n = \frac{f_{CLK}}{\text{CLK RATIO}};\quad Q = \frac{R3}{R2}\sqrt{1 + \frac{R2}{R4}};$$

$$H_{OLP} = \frac{-R2/R1}{1 + (R2/R4)};\quad H_{OBP} = -\frac{R3}{R1};\quad H_{ON1}(f \to 0) = \frac{-R2/R1}{1 + (R2/R4)};$$

$$H_{ON2}\left(f \to \frac{f_{CLK}}{4}\right) = -\frac{R2}{R1}$$

Figure 10. Mode 2: 2nd-Order Filter Providing Notch, Bandpass, Lowpass



$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{1 + \frac{R2}{R4} + \frac{R6}{R5 + R6}};\quad f_n = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{1 + \frac{R6}{R5 + R6}};$$

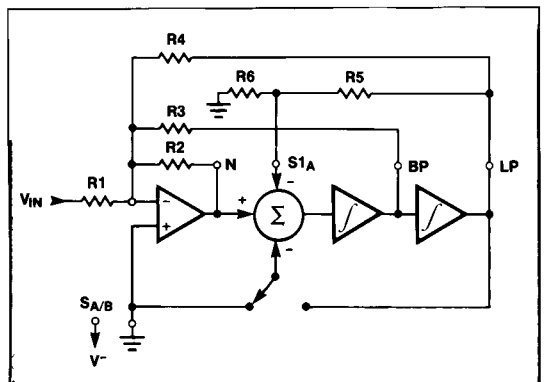
$$Q = \frac{R3}{R2}\sqrt{1 + \frac{R2}{R4} + \frac{R6}{R5 + R6}}$$

$$H_{ON1}(f \to 0) = -\frac{R2}{R1}\left\{\frac{1 + R6/(R5 + R6)}{1 + (R2/R4) + [R6/(R5 + R6)]}\right\};$$

$$H_{ON2}\left(f \to \frac{f_{CLK}}{4}\right) = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1};\quad H_{OLP} = \frac{-R2/R1}{1 + (R2/R4) + [R6/(R5 + R6)]}$$

Figure 11. Mode 2a: 2nd-Order Filter Providing Notch, Bandpass, Lowpass



$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{\frac{R2}{R4} + \frac{R6}{R5 + R6}};\quad f_n = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{\frac{R6}{R5 + R6}};$$

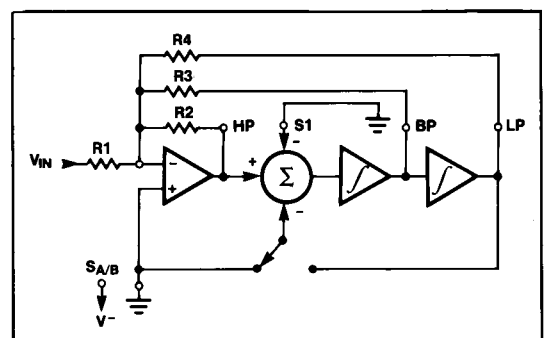
$$Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4} + \frac{R6}{R5 + R6}}$$

$$H_{ON1}(f \to 0) = -\frac{R2}{R1}\left\{\frac{R6/(R5 + R6)}{(R2/R4) + [R6/(R5 + R6)]}\right\};$$

$$H_{ON2}\left(f \to \frac{f_{CLK}}{4}\right) = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1};\quad H_{OLP} = \frac{-R2/R1}{1 + (R2/R4) + [R6/(R5 + R6)]}$$

Figure 12. Mode 2b: 2nd-Order Filter Providing Notch, Bandpass, Lowpass

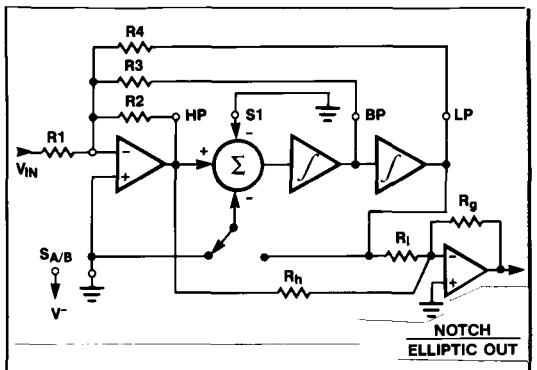


$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{\frac{R2}{R4}};\quad Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}};$$

$$H_{OHP} = -\frac{R2}{R1};\quad H_{OLP} = -\frac{R4}{R1};\quad H_{OBP} = -\frac{R3}{R1}$$

Figure 13. Mode 3: 2nd-Order Filter Providing Highpass, Bandpass, Lowpass

Pin and Resistor Programmed Universal Active Filters



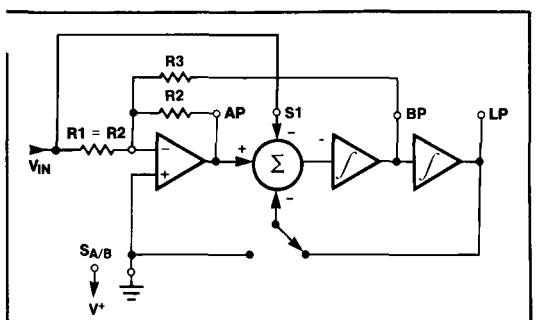
$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{\frac{R_h}{R_I}};$$

$$H_{OHP} = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{OLP} = -\frac{R4}{R1}$$

$$H_{ON1}\ (f \rightarrow 0) = \frac{R_g}{R_I} \times \frac{R4}{R1};\ H_{ON2}\left(f \rightarrow \frac{f_{CLK}}{4}\right) = \frac{R_g}{R_h} \times \frac{R2}{R1};$$

$$H_{ON}(f = f_0) = Q\left(\frac{R_g}{R_I} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)$$

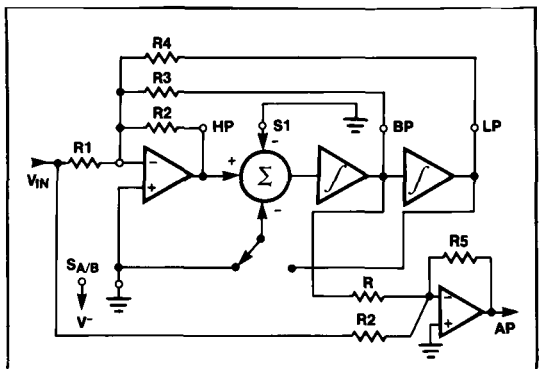
Figure 14. Mode 3a: 2nd-Order Filter Providing Highpass, Bandpass, Lowpass, Notch



$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}};\ Q = \frac{R3}{R2};\ H_{OAP} = -\frac{R2}{R1};$$

$$H_{OLP} = -2;\ H_{OBP} = -2\left(\frac{R3}{R2}\right)$$

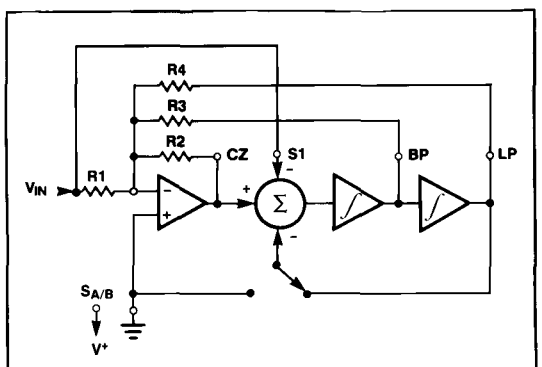
Figure 15. Mode 4: 2nd-Order Filter Providing Allpass, Bandpass, Lowpass



$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{\frac{R2}{R4}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}};\ H_{OAP} = \frac{R5}{R2};\ H_{OHP} = -\frac{R2}{R1};$$

$$H_{OBP} = -\frac{R4}{R1};\ H_{OLP} = -\frac{R3}{R1}$$

Figure 16. Mode 4a: 2nd-Order Filter Providing Highpass, Bandpass, Lowpass, Allpass



$$f_0 = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{1 + \frac{R2}{R4}};\ f_z = \frac{f_{CLK}}{\text{CLK RATIO}}\sqrt{1 - \frac{R1}{R4}};$$

$$Q = \frac{R3}{R2}\sqrt{1 + \frac{R2}{R4}}\quad Q_Z = \frac{R3}{R1}\sqrt{1 - \frac{R1}{R4}};\ H_{OZ}(f \rightarrow 0) = \frac{(R4/R1) - 1}{(R4/R2) + 1};$$

$$H_{OZ}\left(f \rightarrow \frac{f_{CLK}}{4}\right) = \frac{R2}{R1};\ H_{OBP} = \frac{R3}{R2}\left(1 + \frac{R2}{R1}\right);\ H_{OLP}\frac{1 + (R2/R1)}{1 + (R2/R4)}$$

Figure 17. Mode 5: 2nd-Order Filter Providing Numerator Complex Zeros, Bandpass, Lowpass

Pin and Resistor Programmed Universal Active Filters

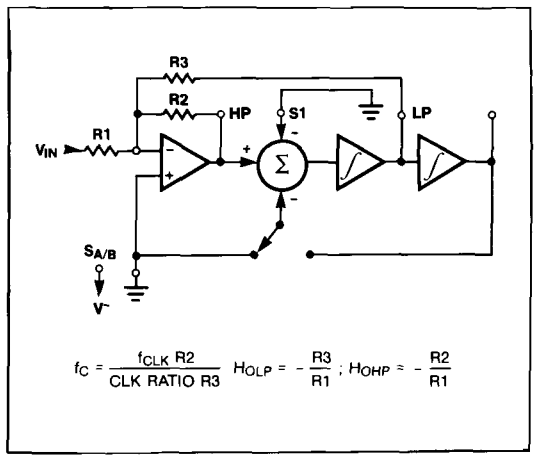


Figure 18. Mode 6a: 1st-Order Filter Providing Highpass, Lowpass

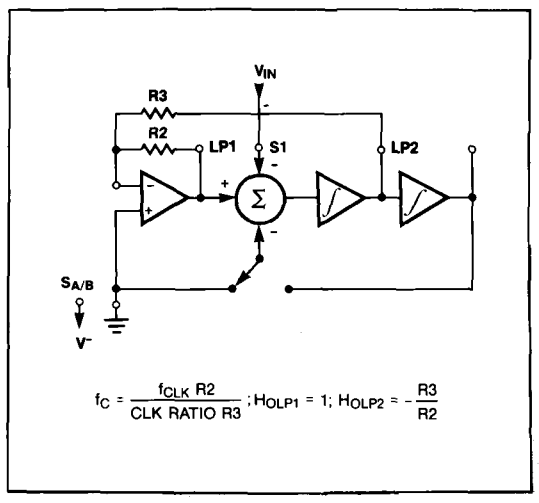


Figure 19. Mode 6b: 1st-Order Filter Providing Lowpass

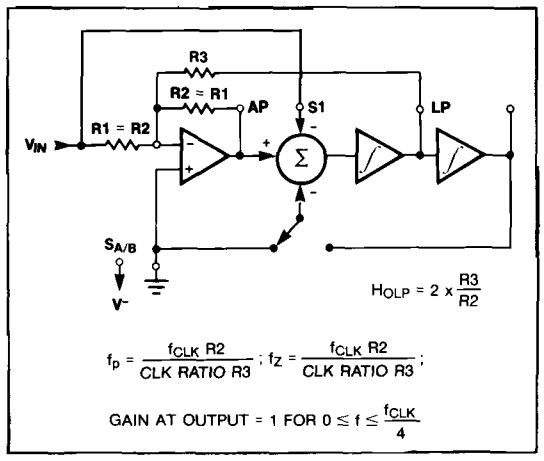


Figure 20. Mode 7: 1st-Order Filter Providing Allpass, Lowpass

Filter Design Procedure

Most designs are begun by converting the required frequency response specifications to f_0s and Qs for one or more cascaded 2nd-order filter sections. This can be done by using design equations or tables in available literature, or can be conveniently determined with program "PZ" in Maxim's filter design software. Once the f_0s and Qs have been found, the next step is to select an appropriate operating mode for the filter type.

Next, the f_{CLK}/f_0 ratio, and clock frequency are selected, and the required resistors are calculated. Filter design program "RP" can be used here to select values for each section.

If the sample rate ($f_{CLK}/2$) is slow enough to cause significant errors, the selected f_0s and Qs may be corrected to account for sampling effects by using Figure 23 or Maxim's design programs. In most cases, the sampling error is not significant, i.e., less than 1 or 2%. In any case, the required f_0s, with or without correction, can then be obtained from Table 2 or the filter design software.

Cascading Filters

In some designs, such as very narrow band filters, or in modes where f_0 cannot be tuned with resistors, several 2nd-order sections with identical f_0 may be cascaded. The total Q of the resultant filter (Q_T) is:

$$\text{Total } Q_T = \frac{Q}{\sqrt{(2^{1/N} - 1)}}$$

Where Q is the Q of each individual filter section, and N is the number of sections. In Table 3, the total Q and bandwidth are listed for up to five identical 2nd-order sections. B is the bandwidth of each section.

Table 3. Cascading Identical Bandpass Filter Sections

Total Sections	Total B.W.	Total Q
1	1.000 B	1.00 Q
2	0.644 B	1.55 Q
3	0.510 B	1.96 Q
4	0.435 B	2.30 Q
5	0.386 B	2.60 Q

Note: B = individual stage bandwidth, Q = individual stage Q.

In higher order polynomial filters, multiple stages with different f_0s and Qs are often cascaded. In such cases, the overall gain is not simply the product of the individual gains at the individual f_0s, since those f_0s are not the same. The combined gain for a 4th-order filter is:

$$\text{Gain at } f_{OBP} = \frac{H_{01}H_{02}F_1F_2/(Q_1Q_2)}{\sqrt{[(F_1^2-1)^2 + (F_1/Q_1)^2][(F_2^2-1)^2 + (F_2/Q_2)^2]}}$$

where $F_1 = f_{01}/f_{0BP}$, $F_2 = f_{02}/f_{0BP}$, and H_{01} and H_{02} are the gain of each 2nd-order section at its own f_0.

Application Hints

Power Supplies

The MAX265/66 can be operated with a variety of supplies including ±2.5V to ±5V, or a +5V to +12V single supply. When a single supply is used, V^- is connected to system ground and the filter's GND pin should be externally biased at $V^+/2$. The input signal is then either capacitively coupled to the filter input or also biased to $V^+/2$. Figure 21 shows circuit connections for single supply operation.

Power consumption at ±5V is reduced if CLK_A and CLK_B are driven with ±5V input levels, rather than TTL or 0 to 5V levels. Operation with +5V or ±2.5V power lowers power consumption but also reduces bandwidth compared to +12V or ±5V supplies.

Best performance is achieved if V^+ and V^- are bypassed to ground with 4.7µF electrolytic (Tantalum preferred) and 0.1µF ceramic capacitors located as close to the IC supply pins as possible. When using a single supply, V^+ and GND should be bypassed to V^-.

Output Swing and Clipping

The MAX265/66 outputs are designed to drive 5kΩ loads to within 0.25V of each supply rail. To ensure that the outputs are not driven beyond their maximum range (output clipping), the peak amplitude response, individual section gains (H_{OBP},H_{OLP},H_{OHP}), input signal levels, and filter offset voltages must be carefully considered. It is especially important to check UNUSED filter outputs for clipping (i.e., the lowpass output in a bandpass hookup) because overload at ANY filter stage severely distorts the overall response.

Choosing Resistors

Resistors that are calculated, or generated by the design programs, may be scaled to other values as long as the ratios remain the same. The lower resistance limit is set by the MAX265/266's ability to drive 5kΩ or more, however, other loads connected to the filter outputs must also be considered. Very large value resistors (>100kΩ) should be used with care because noise pickup and the effects of stray capaci-

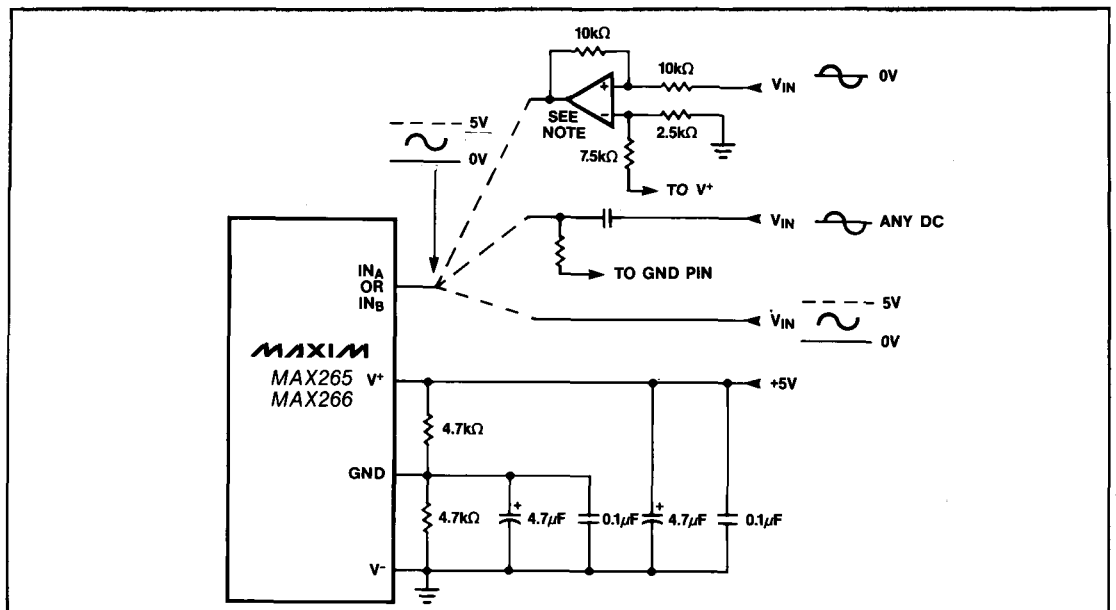


Figure 21. Power Supply and Input Connections for Single Supply Operation

tance will be magnified. Best performance is achieved with resistors scaled to their minimum values without exceeding the load limit on any filter output (5kΩ).

Clock Feedthrough and Noise

Typical wideband noise is $0.5mV_{pp}$ from DC to 100kHz. Output noise is virtually independent of clock frequency. Noise vs. center frequency and Q is plotted in the Typical Operating Characteristics section. Note that clock feedthrough is removed from the noise measurements by an external RC output filter.

The output waveform of the MAX265/66 and other switched capacitor filters appears as a sampled signal with "staircasing" of the output waveform occurring at the internal sample rate ($f_{CLK}/2$). This stepping, if objectionable, is removed by adding a single pole passive RC filter. With no input signal, clock related feedthrough is approximately $8mV_{pp}$. This is also attenuated with an RC smoothing filter as shown with the MAX265 in Figure 22.

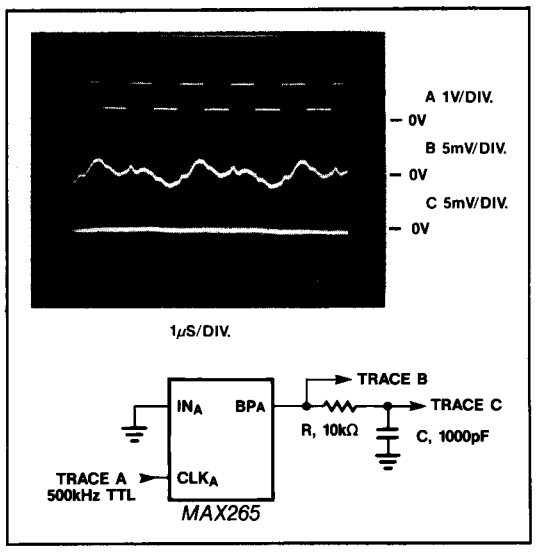


Figure 22. MAX265 Bandpass Output Clock Noise

f_0 and Q at Low Sample Rates

When low f_{CLK}/f_0 ratios and low Qs are selected, deviation from ideal continuous filter response may be noticable in some designs. This is due to interaction between Q, and f_0 at low f_{CLK}/f_0 ratios and Qs. The data in Figure 23 quantifies these differences. Since the errors are predictable, the graphs can correct the selected f_0 and Q so that the actual realized parameters are on target. These predicted errors are not unique to MAX26X series devices and in fact occur with all types of sampled filters. Consequently, the corrections apply to other switched-capacitor filters as well. In many cases, the error is not significant and correction is not needed. However, the MAX266 does employ a lower range of f_{CLK}/f_0 ratios than the MAX265 and is more prone to sampling errors as the graphs in Figure 23 show.

Maxim's filter design software applies the previous corrections automatically as a function of desired f_{CLK}/f_0, and Q. Therefore, Figure 23 should NOT be used when Maxim's software determines f_0 and Q. This results in overcompensation of the sampling errors since the correction factors are then counted twice.

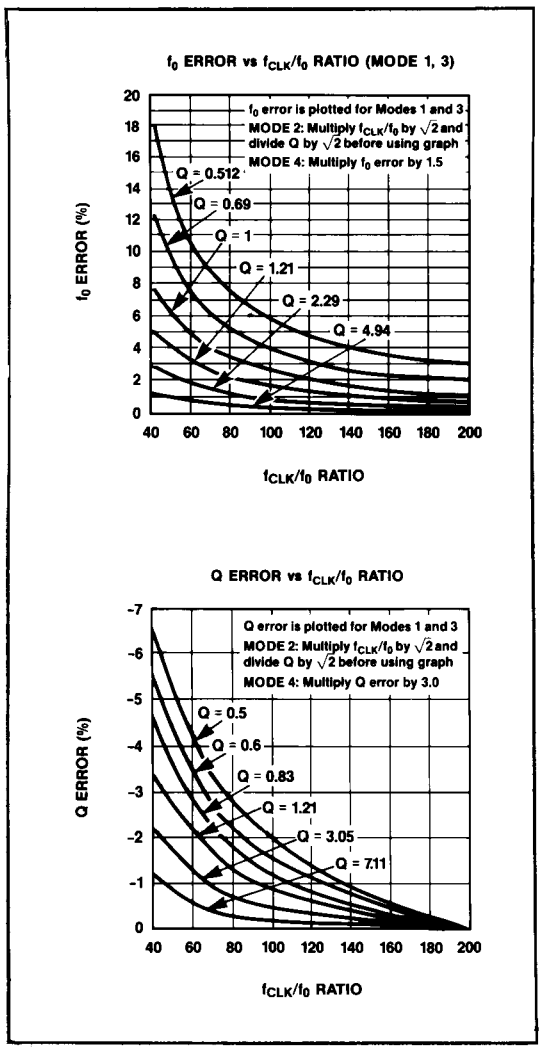


Figure 23. Sample Errors in f_{CLK}/f_0 and Q at Low f_{CLK}/f_0 and Q Settings

Aliasing

As with all sampled systems, frequency components of the input signal above one half the sampling rate will be aliased. In particular, input signal components near the sampling rate generate difference frequencies that often fall within the passband of the filter. Such aliased signals, when they appear at the output, are indistinguishable from real input information. For example, the aliased output signal generated when a 99kHz waveform is applied to a filter sampling at 100kHz, (f_{CLK} = 200kHz) is 1kHz. This waveform is an attenuated version of output that would result from a true 1kHz input. Remember that with the MAX260 series filters, the Nyquist rate (one half the sample rate) is in fact $f_{CLK}/4$ because f_{CLK} is internally divided by two.

A simple passive RC lowpass input filter is usually sufficient to remove input frequencies that can cause aliasing. In many cases the input signal itself may be band limited and require no special anti-alias filtering. The wideband MAX266 uses lower f_{CLK}/f_0 ratios than the MAX265 and for this reason is more likely to require input filtering.

Nulling DC Offset

The DC offset voltage at the LP or Notch output can be nulled with the connection in Figure 24. The circuit also uses the op amp to implement a single-pole anti-alias filter. Note that the total offset will usually be less in multistage filters than when only one section is used since each offset is typically negative each section inverts. When the HP or BP outputs are used, the offset can be removed with capacitor coupling.

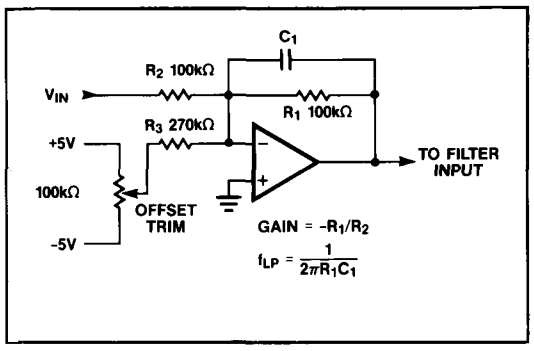


Figure 24. Circuit for DC Offset Adjustment

Design Examples

4th-Order Butterworth Lowpass Filter

Cutoff Frequency = 30kHz
$f_{0A} = f_{0B}$ = 30kHz
Q_A = 1.307, Q_B = 0.541
Gain = 1

The MAX266 works well in this application because of its high operating frequency. Since f_0 is the same for both 2nd-order sections, Mode 1 works well. The above "cookbook" f_0 and Q values for Butterworth filters can be used directly, or the filter design program, PZ, can be used.

If we arbitrarily pick a 2MHz clock for both sections, f_{CLK}/f_0 would be 66.7. By checking the sampling error graphs in Figure 23, however, we see errors approaching 9% at low f_{CLK}/f_0 ratio and low Q. The errors can either be corrected using the data from the graphs, or the filter software (Programs PZ and RP) can be used. The RP design program outputs (rounded to 3 digits here), with error corrections, are:

Sec#1: R1 = 20kΩ, R2 = 20kΩ, R3 = 26.6kΩ
Programmed Clk Ratio = 69.12
Clk Frequency = 2MHz

Sec#2: R1 = 35.9kΩ, R2 = 35.9kΩ, R3 = 20kΩ
Programmed Clk Ratio = 72.26
Clk Frequency = 2Mhz

Note that different programmed clock ratios are selected by RP for each Mode 1 section because slightly different sampling error corrections are applied to each section. The MAX265/266 does not allow separate programming of each filter half (This is allowed by the MAX260/261/262. See appropriate data sheet.) so here we can:

1) Use a clock ratio of 69.12 in both halves and accept the resulting response error.
2) Use a ratio of 69.12 in both halves but change section #2's clock to (69.12/72.26) x 2MHz = 1.913MHz to correct for the error.
3) Use a ratio of 69.12 and a 2MHz clock in both halves but change section 2 to Mode 1B which allows f_0 to be raised with resistors.

We continue the design to demonstate 3), so the above Mode 1 design for section 2 is changed to Mode 1B. This way the clock ratio of 72.26, which can't be set directly (since sections 1 and 2 are one value, 69.12) is tuned by R5 and R6:

$$\frac{\text{Desired } f_{CLK}/f_0 \text{ of section 2}}{\text{Programmed } f_{CLK}/f_0 \text{ of sections 1 and 2}} = \sqrt{1 + R6/(R5 + R6)}$$

$$72.26/69.12 = \sqrt{1 + R6/(R5 + R6)} = 1.045$$

A side effect of tuning f_0 with resistors is that section 2's Q and gain also are shifted. They are restored to their original values (from the Mode 1 design above) by changing R3 and R1 as described below.

The Q of section 2 in Mode 1B is:

$$Q = (R3/R2)\sqrt{1 + R6/(R5 + R6)} = 1.045(R3/R2).$$

Dividing R3 (20kΩ) by 1.045 provides the value needed (19.1kΩ) to compensate for the Q shift caused by R5 and R6.

Pin and Resistor Programmed Universal Active Filters

The gain of section 2 in Mode 1C is:

$$H_{0LP} = -(R2/R1)/(1 + R6/(R5 + R6)) = -1.092(R2/R1)$$

Multiplying R1 (35.9kΩ) by 1.092 provides the value needed (39.2kΩ) to compensate for the gain shift caused by R5 and R6. Figure 25 shows the connection and response for the complete filter. The final design values are tabulated below, but the resistors may be scaled to other values as long as the ratios are maintained.

Sec#1: R1 = 20kΩ, R2 = 20kΩ, R3 = 26.6kΩ
Programmed Clk Ratio = 69.12
Clk Frequency = 2MHz

Sec#2: R1 = 39.2kΩ, R2 = 35.9kΩ, R3 = 19.1kΩ
R5 = 20kΩ, R6 = 2.04kΩ
Programmed Clk Ratio = 69.26
Clk Frequency = 2MHz

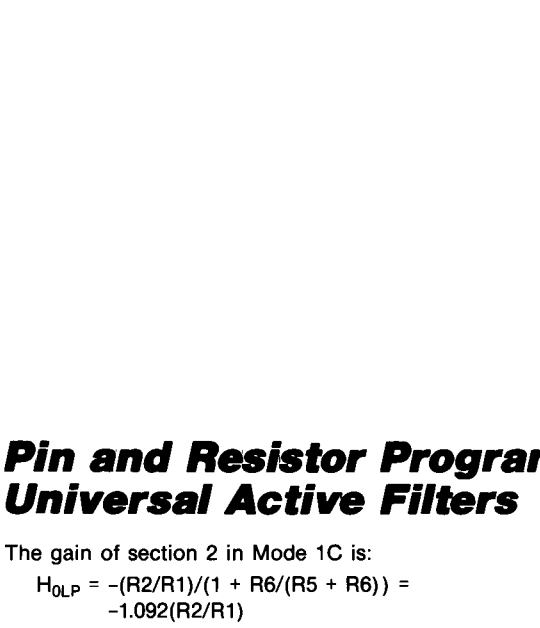


Figure 25. 30kHz Butterworth Lowpass with 2MHz Clock

8th-Order Chebyshev Bandpass

Center frequency = 12.8kHz
Pass Bandwidth = 9.05kHz (1 octave)
Stop Bandwidth = 19.2kHz
Attenuation = 35dB
Passband Ripple = 0.5dB

This example is designed to be a 1-octave bandpass filter at 12.8kHz that provides 35dB of attenuation at the center of the adjacent 1-octave bands (6.4kHz and 25.6kHz). The above specs are given to design program PZ which outputs the following f_0s and Qs.

9.294kHz	Q = 9.37
17.629kHz	Q = 9.37
11.178kHz	Q = 3.73
14,657kHz	Q = 3.73

Two MAX266 ICs make the 8th-order filter. A 1MHz clock is preferred for all sections so filter Mode 3, which allows the ost flexible tuning of f_0 and Q, is selected. Program RP picks resistors and programmed clock ratios. It asks for each section's f_0, Q, f_{CLK}, and gain. All sections are set for a gain of one.

Program RP asks for: 1) clock frequency, 2) clock ratio, or 3) both as input data for each filter half, but in the MAX265/266 both halves use the same clock ratio. Therefore when designing section 1, we tell RP the clock frequency (1MHz) and ask the program to pick the clock ratio. In section 2, we specify the clock frequency and ratio to be the same as section 1. In section 3 (the second filter chip), the program picks the ratio, and we use this same ratio for section 4. As the circuit connection in Figure 26 shows, the order of the sections is changed so that those with the closest f_0 are in the same IC. This way f_0 is tuned the least amount by resistors. The design values are listed below. Remember that these may be scaled to other values if the ratios are maintained.

Sec#1: R1 = 189kΩ, R2 = 20.2kΩ, R3 = 189kΩ
R4 = 20kΩ
Programmed Clk Ratio = 108.38
Clk Frequency = 1MHz

Sec#2: R1 = 90kΩ, R2 = 29kΩ, R3 = 90kΩ
R4 = 20kΩ
Programmed Clk Ratio = 108.38
Clk Frequency = 1MHz

Sec#3: R1 = 75.6kΩ, R2 = 20.2kΩ, R3 = 75.6kΩ
R4 = 20kΩ
Programmed Clk Ratio = 69.12
Clk Frequency = 1MHz

Sec#4: R1 = 229kΩ, R2 = 29.5kΩ, R3 = 229kΩ
R4 = 20kΩ
Programmed Clk Ratio = 108.38
Clk Frequency = 1MHz

Pin and Resistor Programmed Universal Active Filters

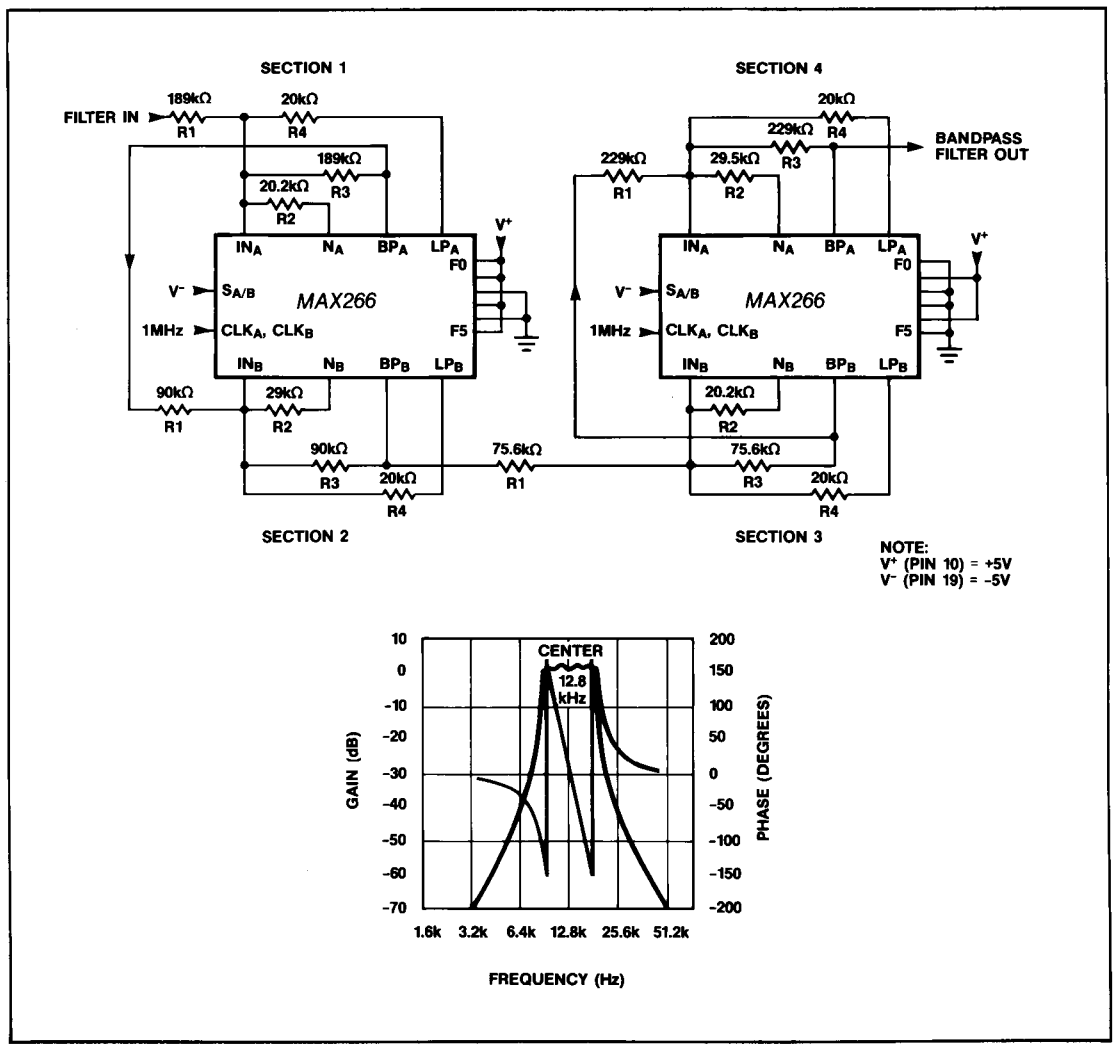


Figure 26. 12.8kHz, 1-Octave Bandpass with 1MHz Clock

Pin and Resistor Programmed Universal Active Filters

Chip Topography