COS/MOS INTEGRATED CIRCUITS

M 755
M 756

PRELIMINARY DATA

CLOCK/DISPLAY INTERFACE FOR MICROPROCESSORS

- DAY, HOUR AND MINUTE COUNT
- 1 Hz FLASHING COLON
- 24 HOUR (M755) or 12 HOUR (M756) MODES
- INTERNAL OSCILLATOR (32.768 KHz)
- OVERFLOW OUTPUT
- BCD MULTIPLEXED OUTPUTS FOR STANDARD 7-SEGMENT DECODER/DRIVER
- DISPLAY OF TIME OR OF DATA REGISTERS
- MICROPROCESSOR CONTROLLED DECIMAL POINT

The M755 and M756 are COS/MOS clocks specially designed for battery backed up applications in Microprocessor based systems. The circuits include also a day of the week count section.
The content of the counters can be read by the Microprocessor and/or displayed using a standard BCD to 7-segment LED decoder driver.
The circuits also provide a 1 Hz flashing colon output.
It is possible to display the content of the data registers instead of the clock section output to show, for instance, the TV channel and program number.
The same registers can be used as a 5 x 4 non-volatile memory.
The M755 and M756 interface with a Microprocessor I/O port by a 4 bit bidirectional bus and two strobe signals which are used to address, load and read the internal registers and counters.
The circuits are produced using a Low-Voltage COS/MOS technology and are assembled in 24-lead dual in-line plastic or ceramic frit seal packages.

ABSOLUTE MAXIMUM RATING*

V_{DD} **	Supply voltage	-0.3 to 6	V
V_I	Input voltage	-0.3 to V_{DD} +0.3	V
I_I	DC input current	± 1	mA
$V_{o(off)}$	Off-state output voltage	6	V
I_{OH}	Continuous output source current DP, PM outputs	-25	mA
	D1 to D4 outputs	-10	mA
P_{tot}	Total power dissipation (per package)	300	mW
	Dissipation per output transistor	100	mW
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

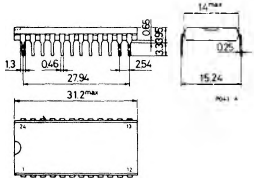
** All voltages are with respect to V_{SS} (GND).

ORDERING NUMBERS: M755 B1 for dual in-line plastic package
M756 B1 for dual in-line plastic package
M755 F1 for dual in-line ceramic frit seal package
M756 F1 for dual in-line ceramic frit seal package

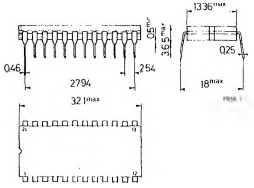
M 755
M 756

MECHANICAL DATA (dimension in mm)

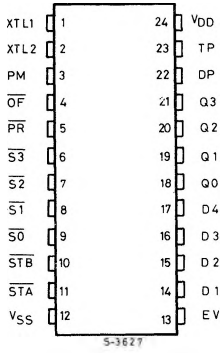
Dual in-line plastic package



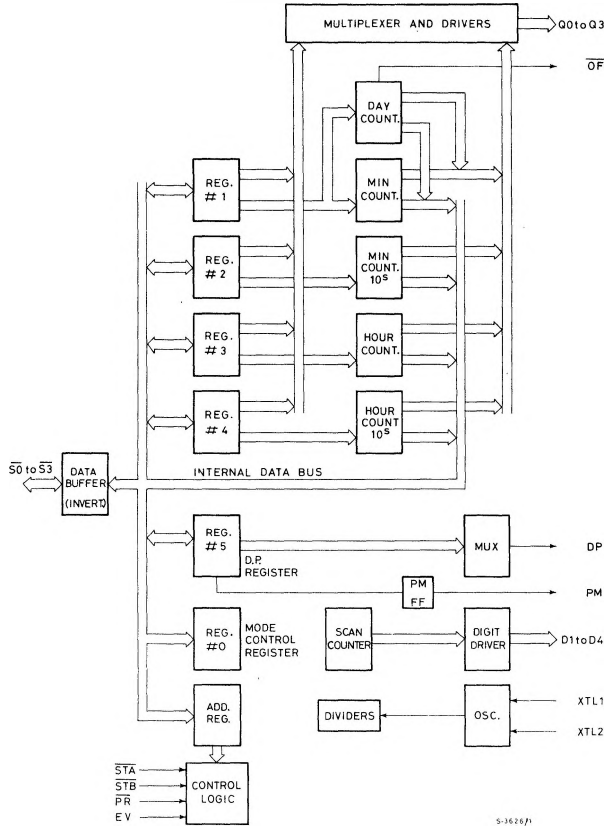
Dual in-line ceramic frit seal package



PIN CONNECTIONS



BLOCK DIAGRAM



PIN DESCRIPTION

PIN NAME	FUNCTION	NOTE
$\overline{S0}$ to $\overline{S3}$	Data/address bus (4 bits)	Bidirectional, open drain outputs
$\overline{STA}$	Address strobe	Input
$\overline{STB}$	Data strobe	Input
XTL1, XTL2	Crystal connections	XTL1 osc. in, XTL2 osc. out.
D1 to D4	Digit strobes	Outputs, emitter follower
Q0 to Q3	BCD data display	Outputs
DP	Decimal point/flashing colon	Output, emitter follower
PM	PM indication	Output, emitter follower
$\overline{OF}$	Overflow	Output, open drain
$\overline{PR}$	Load counter	Input
EV	External voltage indication	Input
TP	Test pin	Input/output. Leave open circuit

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	2 to 5.25	V
V_I	Input voltage	0 to V_{DD}	V
$V_{O(off)}$	Off-state output voltage	max. 5.25	V
I_{OH}	Pulsed output current DP, PM outputs	max. -20	mA
	D1 to D4 outputs	max. -7	mA
T_{op}	Operating temperature	0 to 70	°C

STATIC ELECTRICAL CHARACTERISTICS

(Over recommended operating conditions, V_{DD}= 5V, unless otherwise specified) Typ. values are at T_{amb}= 25°C

Parameter			Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	All inputs		2.6			V
V_{IL}	Input low voltage	All inputs				0.8	V
I_I	Input leakage current	All inputs	V_I = 0 to 5.25V			10	μA
V_{OL}	Output low voltage	Q0 to Q3 S0 to S3	I_{OL}= 1.6 mA			0.4	V
		D1 to D4 DP, PM	I_{OL}= 40 μA			0.5	
V_{OH}	Output high voltage	DP, PM	I_{OH}= 0	4.25	4.5		V
			I_{OH}= -20 mA	3	4		
		D1 to D4	I_{OH}= 0	4.5	4.75		
			I_{OH}= -7 mA	2	4		
		Q0 to Q3	I_{OH}= -40 μA	3.5	3.75		
I_{DD}	Supply current		V_{DD}= 2.5V (EV input grounded)		15	30	μA
			V_{DD}= 5.25V (all out. and inp. open)		0.5	1	mA

DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{DD}= 5V, T_{amb}= 25°C, C_L= 15 pF at each output)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{w1}	Digit display time	see fig. 1		1.5		ms
t_{w2}	Interval between two digits			0.5		ms
t_{p1}	Propagation delay time				100	ns
t_w	$\overline{STA}$ and $\overline{STB}$ width	see fig. 2, 3	500			ns
t_{h1}	Hold time of $\overline{S0}$ to $\overline{S3}$ from $\overline{STA}$ or $\overline{STB}$	see fig. 2	250			ns
t_{setup}	Set up time of $\overline{STA}$ from $\overline{STB}$		800			ns
t_{h2}	Hold time of $\overline{STA}$ from $\overline{STB}$	see fig. 3	500			ns
t_r	Release time of DATA out from $\overline{STB}$		250			ns

Fig. 1 - Display timing

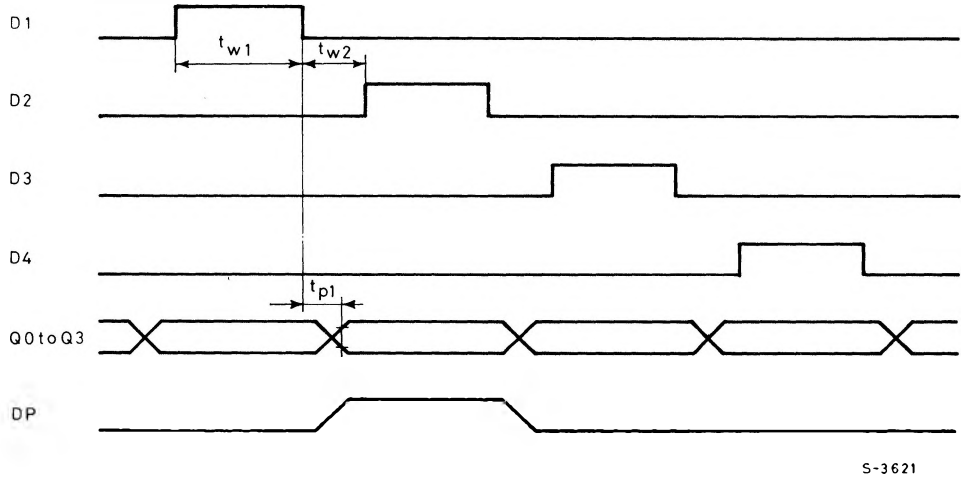


Fig. 2 - Write timing

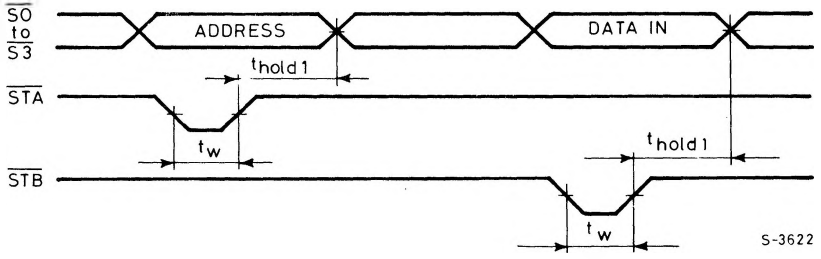
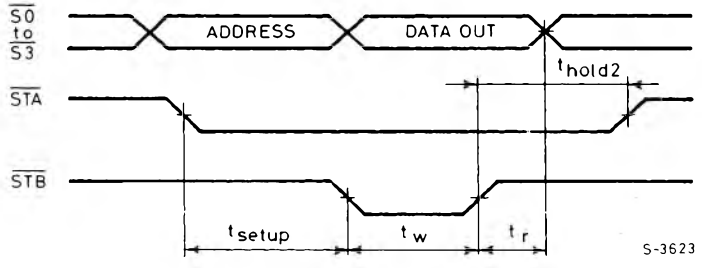


Fig. 3 - Read timing



DESCRIPTION

Data Buffer

This bidirectional, open drain, four bit data buffer is used to interface the M755/6 with the Microprocessor. Data is transmitted or received by the buffer and also Control words and Address are received through it. Note that this buffer is inverting and the I/O lines are not provided with pull-up.

Control Logic

The function of this block is to manage all the internal and external Data transfers.
This block in controlled by Data and Address Strobes ($\overline{STA}$ and $\overline{STB}$), by two other inputs ($\overline{PR}$ and EV) and in turn generates the operation as described in table 1.
The source or the destination of data depends on the contents of the Address Register and Control Register.

Table 1 - Truth table of the control logic block

EV	$\overline{PR}$	$\overline{STA}$	$\overline{STB}$	OPERATION
L	H	X	X	Outputs off, all inputs disabled
H	H	H	H	Data Buffer High impedance
H	H	L	H	Address Register loading
H	H	H	L	Data loading in the selected register
H	H	L	L	Reading back of the selected register or counter
H	L	X	X	Counters loading from registers 1 to 5,count off
H	⌐	X	X	Normal operation

Address Register

The function of this register is to latch the address of the register involved on the actual I/O cycle. Therefore it must be loaded at the start of any I/O cycle.
It is possible to address six registers: a 0 in this register always addresses the Mode Control Register and a BCD 5 addresses the D.P. Register, independently of the content of the Mode Control Register.
The BCD figure from 1 to 4 can address many registers, in conjunction with the content of the Mode Control Register.

Mode Control Register

This register selects the operating mode in order to select the group of counters or registers that must be read, displayed or loaded.
Table 2 shows the function that can be selected.

Table 2 - Truth table of the Mode Control Register

Mode number	Control word				Function
	$\overline{S3}$	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	
0	X	H	H	H	Set Register out (Read and Display)
1	X	H	H	L	Set Clock Counters out (Read and Display)
2	X	H	L	H	Day Counter out (Read and Display)
3	X	H	L	L	Load Clock Counter and PM
4	X	L	H	H	Load Day Counter
5	X	L	H	L	Don't care
6	X	L	L	H	Don't care
7	X	L	L	L	Don't care (see note 1)

Note 1: This configuration must be used for a very low power consumption during battery back-up.

Mode 0-Set Registers read/display
When programmed, this mode enables the content of Register 1 to 4 to be displayed or read back through the Data Buffer.
This mode resets automatically the Mode 1, if previously programmed.

Mode 1-Set Clock Counters read/display
When programmed, this mode enables the content of Clock Counters to be displayed or read back through the Data Buffer. This mode resets the Mode 0, if previously programmed.

Table 3 - Counters Selection (Read)

Address	Counter
1	Minutes
2	10's of minutes
3	Hours
4	10's of hours

Mode 2-Day Counter read/display
When selected, this mode enables the content of the Day Counter to be displayed or read back through the Data Buffer. This mode is active only if Mode 1 was previously programmed.
The content of the Day Counter is displayed during the digit 1 time and can be read back as register 1.

Mode 3-Load Clock Counters and PM
This mode enables the loading of Data from Registers 1 to 5 into the clock counters and PM flip-flop. This can also be done by connecting the $\overline{PR}$ input Low.

Table 4 - Register to Counter transfer

Register	Counter
1	Minutes
2	10's of minutes
3	Hours
4	10's of hours

Table 5 - PM flip-flop, Set/Reset table

Register-5	PM
0	Set
any	Reset

Mode 4-Load Day Counter
This mode enables the loading of register 1 into the Day counter.
All other counters are unaffected.

D.P. Register, output

The function of this register is to latch the value of decimal point output D.P. for any of the four digits. A bit "1" turns on the D.P. output, a "0" turns it off.

Table 6 - D.P. (Register 5)

3	2	1	0	Bit number
4	3	2	1	Digit
10's hour	hour	10's min.	min.	

When M755/M756 are programmed in Mode 1, the decimal point D.P. is switched at 1 Hz rate, if generated at digits time 3 or 2.
This feature is provided to accomodate displays with right hand D.P., left hand D.P. or with a colon. The output has emitter follower configuration.

Oscillator

An external quartz crystal, resonant a 32 768 KHz, connected at XTL1 and XTL2 pins sets the internal oscillator to the correct input frequency. This frequency is divided and used for both scanning of the display control (500 Hz) and time counting (1 Hz).
An external clock signal may be applied to pin 1 or pin 2 with pin 1 connected to V_{SS} to V_{DD}.

P.M. output

This output is available for P.M. time indication only in 12 hour mode and has emitter follower configuration.
The P.M. status can be read back checking the conditions of the bit number 3 of the 10's of hours counter (1 = P.M., 0 = A.M.).

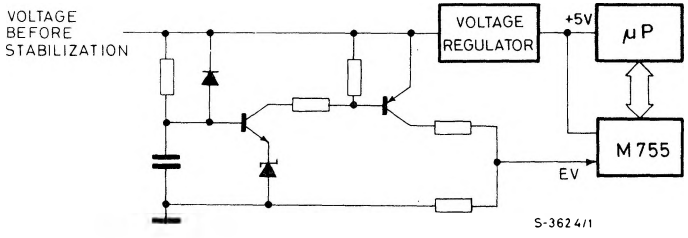
$\overline{OF}$ output

The $\overline{OF}$ output (overflow) has open drain configuration. It goes active (Low) on the 23.59/0.00 transition for 30" (M755) or on PM/AM transition 11.59/12.00 for 60' (M756).

EV input

This EV input (External Voltage) is used during battery powered operation.
In this case, a low level on the EV input switches off all outputs in order to reduce power consumption. In addition, all inputs are disabled in order to prevent affecting of register during power down of the microprocessor which controls the M755/M756.
Figure 5 shows a circuit which could be used to generate EV:

Fig. 5 - EV Signal Generation



APPLICATION CIRCUIT