

HC690 DECADE COUNTER/REGISTER (3-STATE) HC691 4-BIT BINARY COUNTER/REGISTER (3-STATE)

- **HIGH SPEED**
 $f_{MAX} = 33\text{MHz (TYP.) at } V_{CC} = 5\text{V}$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4\text{ }\mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 15 LSTTL LOADS (FOR Q_A to Q_D)
 10 LSTTL LOADS (FOR RCO)
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 6\text{ mA (MIN.) FOR } Q_A \text{ to } Q_D$
 OUTPUT
 $|I_{OH}| = I_{OL} = 4\text{ mA (MIN.) FOR RCO OUTPUT}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC}(\text{OPR}) = 2\text{V to } 6\text{V}$
- **PIN AND FUNCTION COMPATIBLE**
 WITH LSTTL 54/74LS690/691

DESCRIPTION

The HC690/691 are high speed CMOS COUNTER/REGISTER fabricated in silicon gate C²MOS technology.

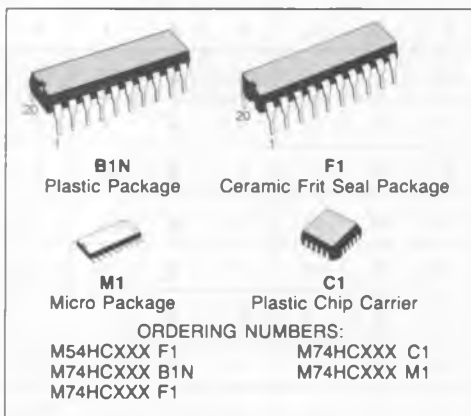
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

The internal circuit is composed of 3 stages including buffer output, which offers high noise immunity and stable output.

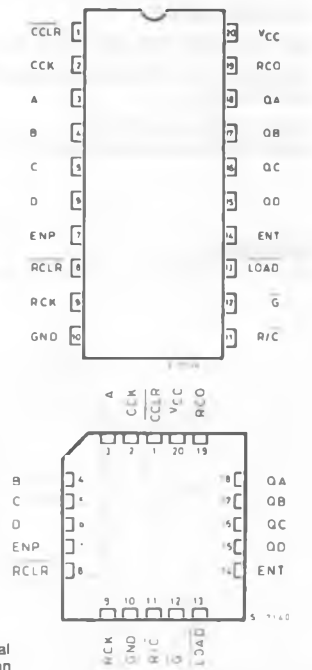
These devices incorporate a synchronous counter, four-bit D-type register, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counter can be programmed from the data inputs and have enable P and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/C, selects the counter when low or the register when high for the three-state outputs, Q_A , Q_B , Q_C , and Q_D .

Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are active low and is synchronous.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.



PIN CONNECTIONS (top view)



NC =
No Internal
Connection

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{\text{CCLR}}$	$\overline{\text{LOAD}}$	ENP	ENT	CCK	$\overline{\text{RCLR}}$	RCK	R/C	$\overline{\text{G}}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X		X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	L	X		X	X	L	L	NO CHANGE				NO COUNT
H	H	X	L		X	X	L	L	NO CHANGE				NO COUNT
H	H	H	H		X	X	L	L	COUNT UP				COUNT UP
H	X	X	X		X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	X	H	L	L	L	L	L	CLEAR REGISTER
X	X	X	X	X	H		H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	H		H	L	NO CHANGE				NO LOAD

X : DON'T CARE

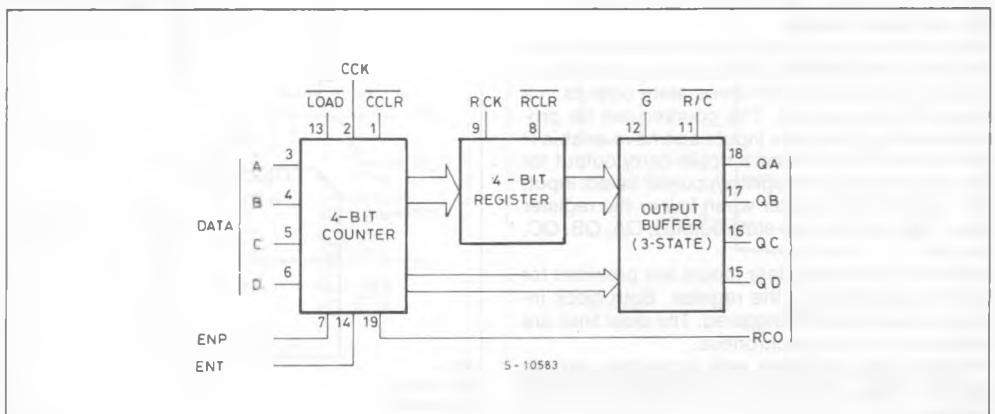
Z : HIGH IMPEDANCE

a-d : THE LEVEL OF STEADY STATE INPUTS AT INPUTS A THROUGH D RESPECTIVELY.

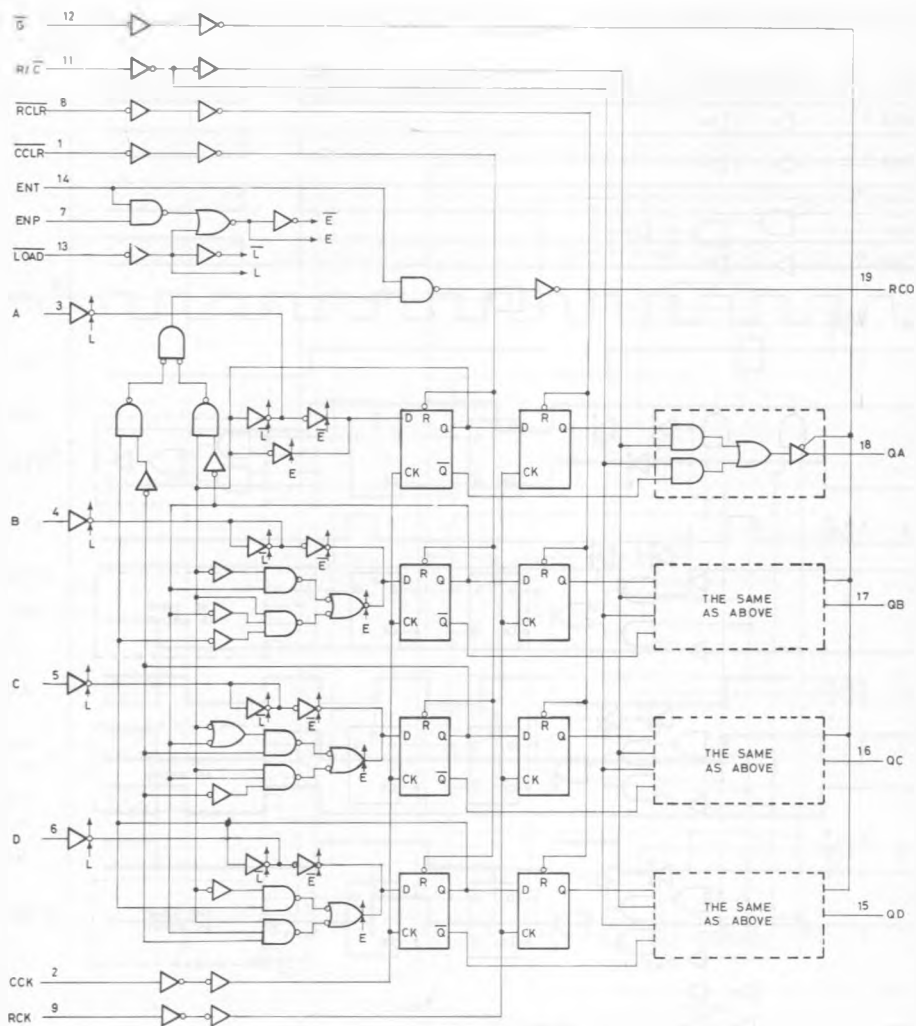
a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS QA' THROUGH QD' RESPECTIVELY.

HC690 $\text{RCO} = \text{QA} \cdot \text{QD} \cdot \text{ENT}$ HC691 $\text{RCO} = \text{QA} \cdot \text{QB} \cdot \text{QC} \cdot \text{QD} \cdot \text{ENT}$

BLOCK DIAGRAM

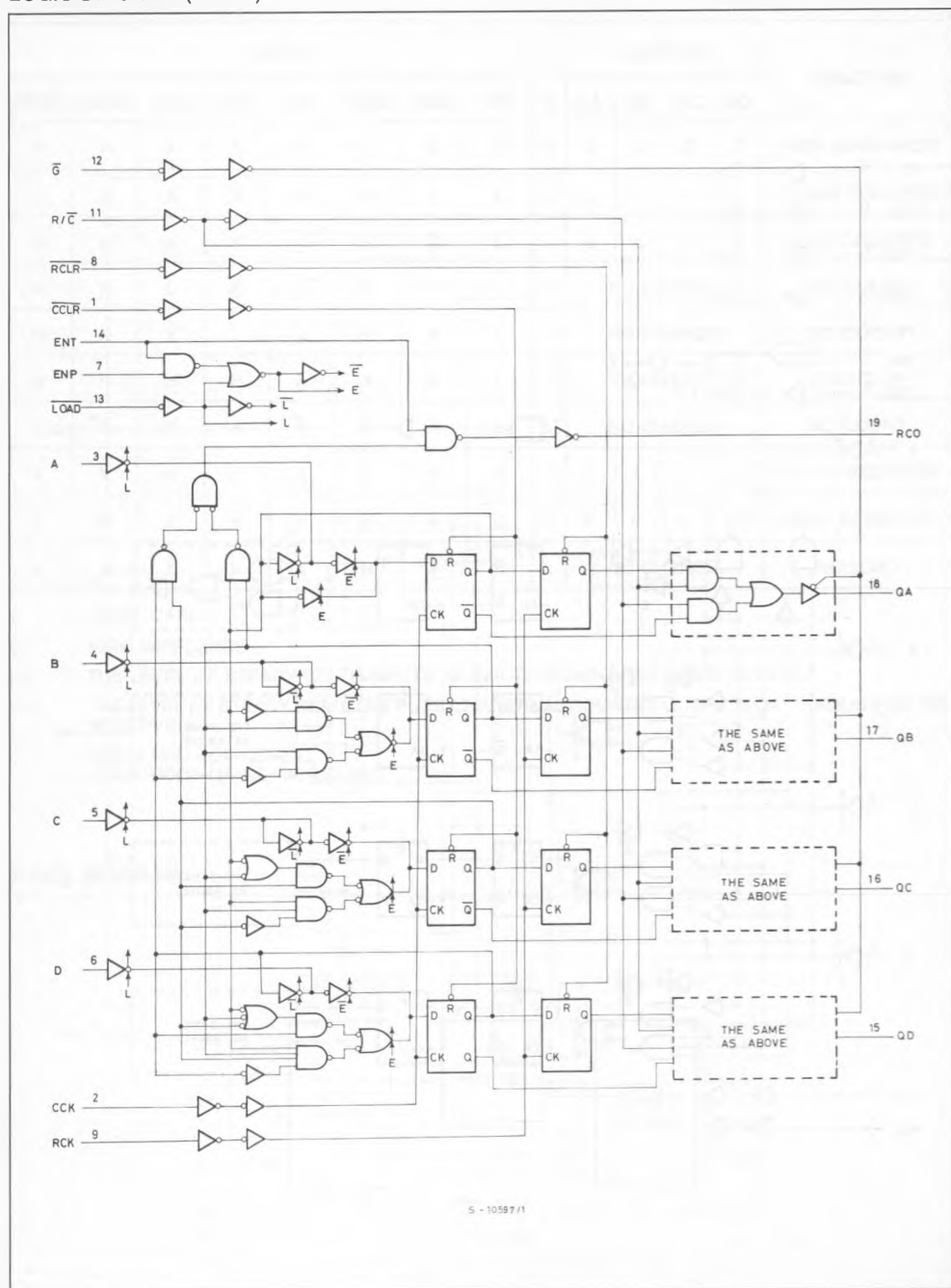


LOGIC DIAGRAM (HC690)



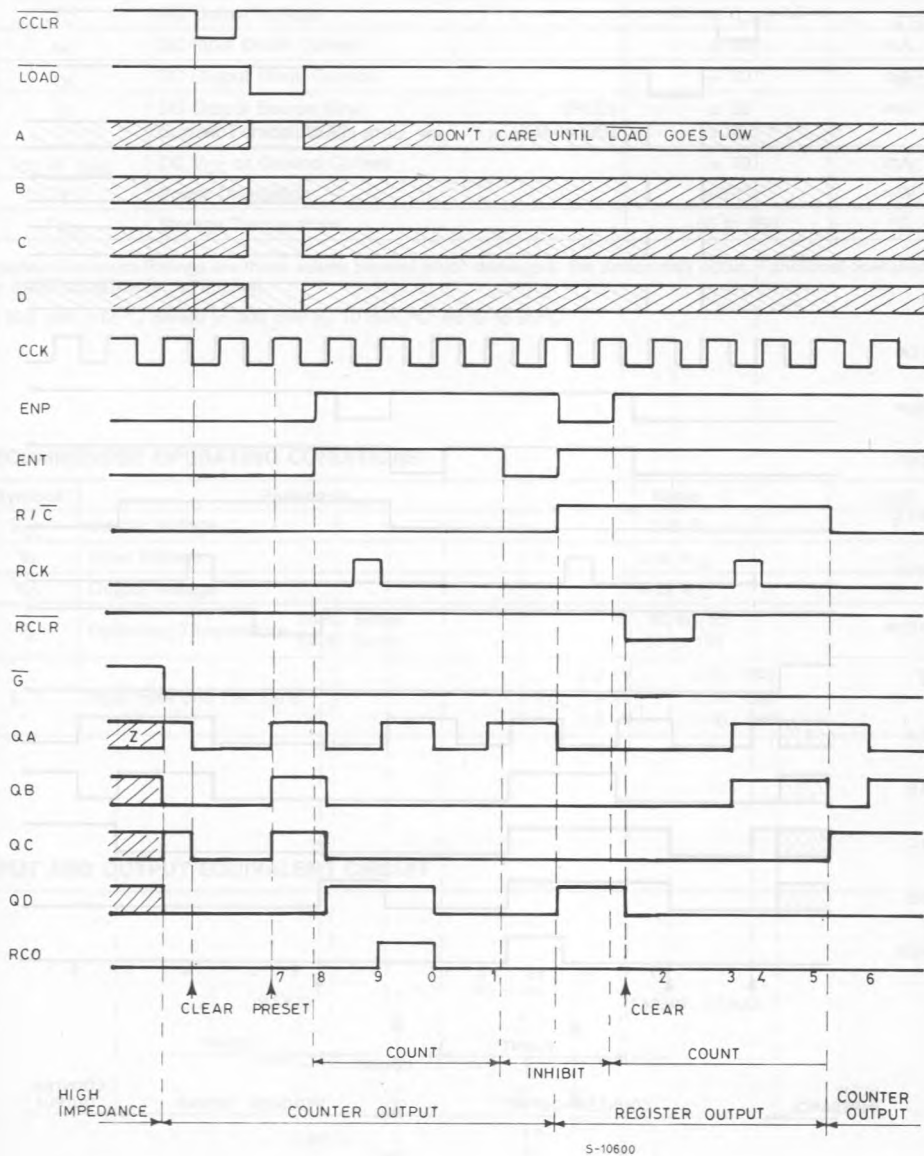
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LOGIC DIAGRAM (HC691)

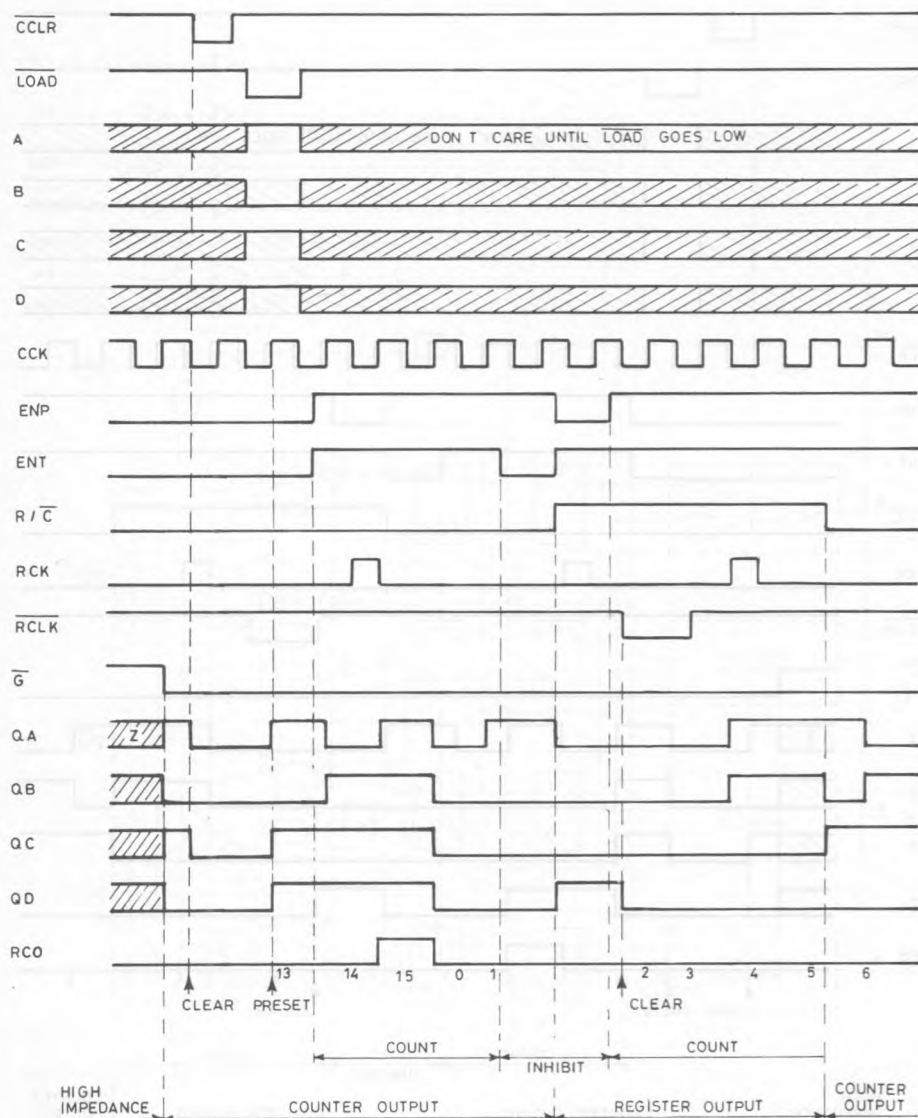


TIMING CHART (HC690)

(HIGH) TRAP CHART



TIMING CHART (HC691)



S-10599 / 1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	− 0.5 to 7	V
V _I	DC Input Voltage	− 0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	− 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin (RCO) (QA to QD)	± 25 ± 35	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	− 65 to 150	°C

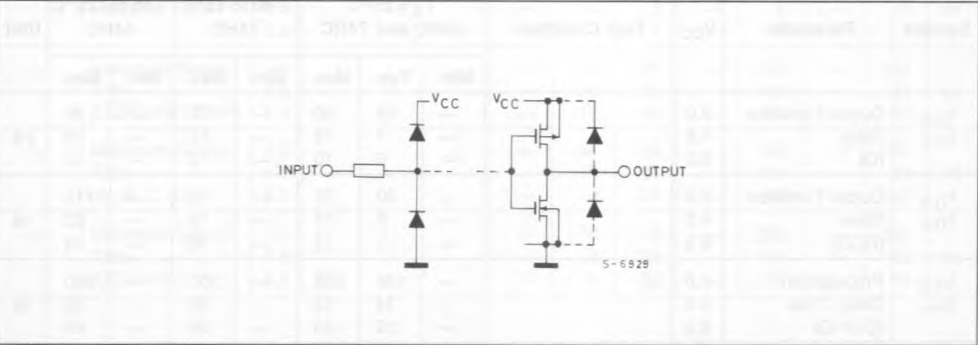
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2 to 6	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 − 55 to 125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} { 2 V 0 to 1000 4.5V 0 to 500 6 V 0 to 400	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
					Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _{IN}	I _{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH}	– 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	V _{IH} or V _{IL}		5.9	6.0	—	5.9	—	5.9	—	
		4.5 6.0	Q _A -Q _D	– 6.0 mA – 7.8 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
		4.5 6.0	R _{CO}	– 4.0 mA – 5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V _{OL}	Low Level Output Voltage	2.0	V _{IN}	I _{OL}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V _{IH}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0	V _{IH} or V _{IL}		—	0	0.1	—	0.1	—	0.1	
		4.5 6.0	Q _A -Q _D	6.0 mA 7.8 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
		4.5 6.0	R _{CO}	4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I _{OZ}	3-State Off-State Current	6.0	V _{IN} = V _{IL} or V _{IH} V _{OUT} = V _{CC} or GND		—	—	± 0.5	—	± 5.0	—	± 10	μA
I _{IN}	Input Leakage Current	6.0	V _{IN} = V _{CC} or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	
I _{CC}	Quiescent Supply Current	6.0	V _{IN} = V _{CC} or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transition Time (Q)	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13	— — —	90 18 15	ns
t _{TLH} t _{THL}	Output Transition Time (RCO)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CCK-Q)	2.0 4.5 6.0		— — —	136 34 29	265 53 45	— — —	335 66 56	— — —	400 80 68	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time (RCK-Q)	2.0 4.5 6.0		— — —	148 37 31	285 57 48	— — —	355 71 60	— — —	430 86 73	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CCK-RCO)	2.0 4.5 6.0		— — —	128 32 27	250 50 43	— — —	315 63 54	— — —	375 75 64	ns
t _{PLH} t _{PHL}	Propagation Delay Time (R/C-Q)	2.0 4.5 6.0		— — —	104 26 22	200 40 34	— — —	250 50 43	— — —	300 60 51	ns
t _{PLH} t _{PHL}	Propagation Delay Time (ENT-RCO)	2.0 4.5 6.0		— — —	56 14 12	110 22 19	— — —	140 28 24	— — —	165 33 28	ns
t _{PHL}	Propagation Delay Time (CCLR-Q)	2.0 4.5 6.0		— — —	160 40 12	305 61 52	— — —	385 77 66	— — —	460 92 78	ns
t _{PLH}	Propagation Delay Time (CCLR-RCO)	2.0 4.5 6.0		— — —	132 33 28	255 51 43	— — —	320 64 54	— — —	385 77 65	ns
t _{PHL}	Propagation Delay Time (RCLR-Q)	2.0 4.5 6.0		— — —	148 37 31	285 57 48	— — —	355 71 60	— — —	430 86 73	ns
f _{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		4 20 24	8 30 35	— — —	3 16 19	— — —	3 13 15	— — —	MHz
t _{W(H)} t _{W(L)}	Minimum Pulse Width (CCK, RCK)	2.0 4.5 6.0		— — —	40 10 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
t _{W(L)}	Minimum Pulse Width (CCLR, RCLR)	2.0 4.5 6.0		— — —	44 11 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
t _{REM}	Minimum Removal Time	2.0 4.5 6.0		— — —	— — —	25 5 5	— — —	30 6 6	— — —	40 8 7	ns
t _S	Minimum Set-up Time (LOAD, ENT, ENP)	2.0 4.5 6.0		— — —	80 20 17	175 35 30	— — —	220 44 37	— — —	265 53 45	ns
t _S	Minimum Set-up Time (A, B, C, D)	2.0 4.5 6.0		— — —	48 12 10	125 25 21	— — —	155 31 26	— — —	190 38 32	ns
t _S	Minimum Set-up Time (CCK-RCK)	2.0 4.5 6.0		— — —	76 19 16	175 35 30	— — —	220 44 37	— — —	265 53 45	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

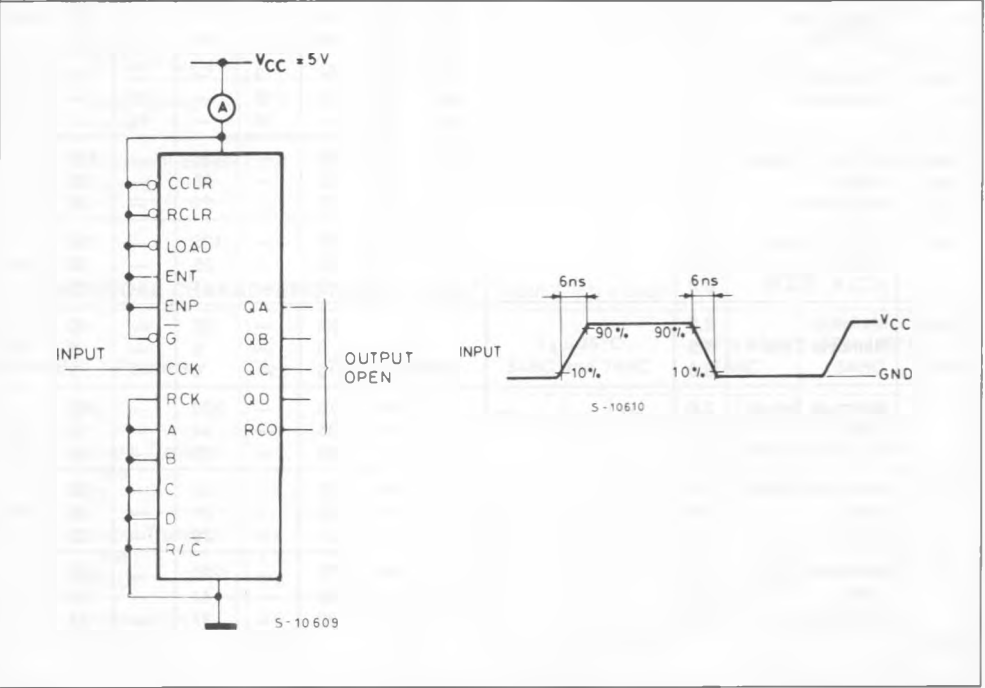
Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _H	Minimum Hold Time	2.0 4.5 6.0		—	—	0	—	0	—	0	ns
				—	—	0	—	0	—	0	
				—	—	0	—	0	—	0	
t _{PZL} t _{PZH}	3-State Output Enable Time	2.0 4.5 6.0	R _L = 1kΩ	—	72 18 15	145 29 25	—	180 36 31	—	220 44 38	ns
				—			—		—		
				—			—		—		
t _{PLZ} t _{PHZ}	3-State Output Disable Time	2.0 4.5 6.0	R _L = 1kΩ	—	92 23 20	170 34 29	—	215 43 37	—	255 51 43	ns
				—			—		—		
				—			—		—		
C _{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C _{PD} (*)	Power Dissipation Capacitance			—			—		—		
				—	80	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).

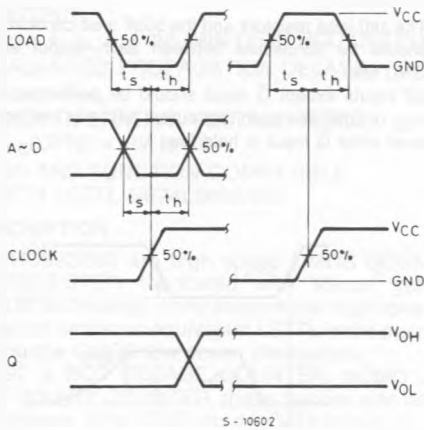
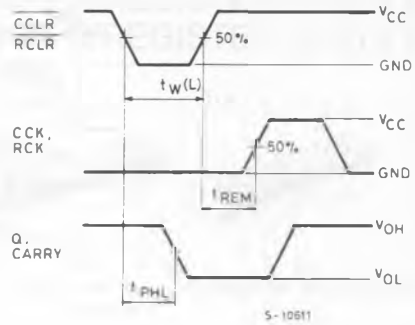
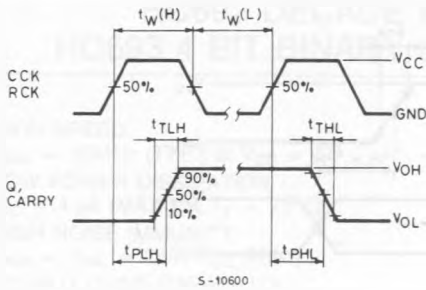
Average operating current can be obtained from the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

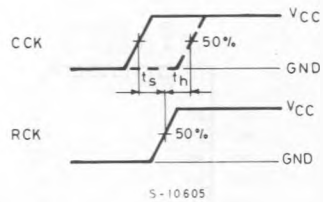
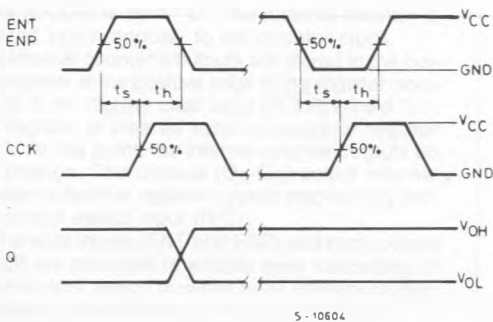
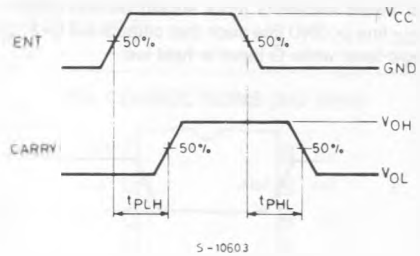
TEST CIRCUIT I_{CC} (Opr.)



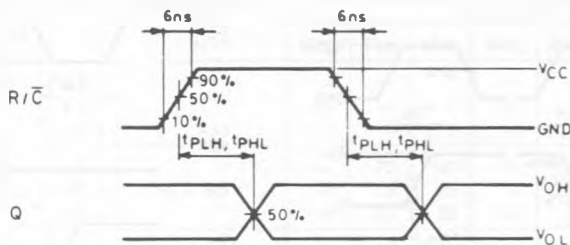
SWITCHING CHARACTERISTICS TEST WAVEFORM



(Fix Maximum Count)



SWITCHING CHARACTERISTICS (Continued)



S-10606

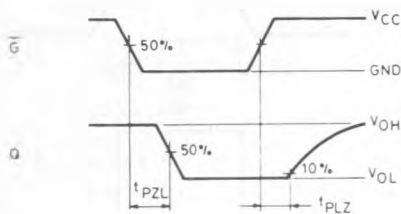
 t_{PLZ} , t_{PZL}

The 1k Ω load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except $\bar{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\bar{G}$ input is held low.

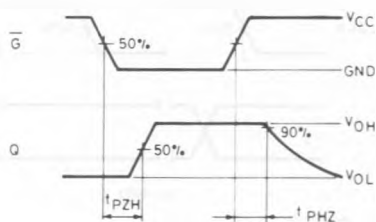
 t_{PHZ} , t_{PZH}

The 1k Ω load resistors and the 50pF load capacitors should be connected between each output and GND line.

All inputs except $\bar{G}$ input should be connected to V_{CC} or GND line such that output will be in low logic level while $\bar{G}$ input is held low.



S-10607



S-10608