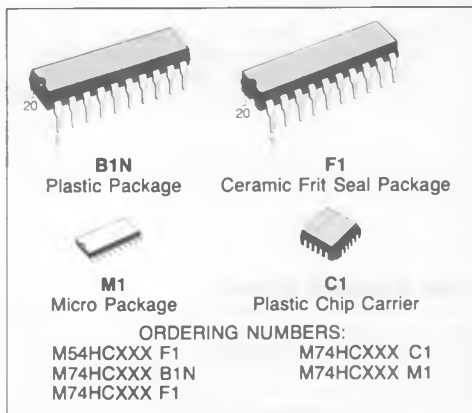


OCTAL BUS TRANSCEIVER (3-STATE) HC245 NON INVERTING, HC640 INVERTING, HC643 INVERTING/NON INVERTING

PRELIMINARY DATA

- **HIGH SPEED**
 $t_{PD} = 11 \text{ ns (TYP.) at } V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu A \text{ (MAX.) at } T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 15 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = |I_{OL}| = 6 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS245/640/643



DESCRIPTION

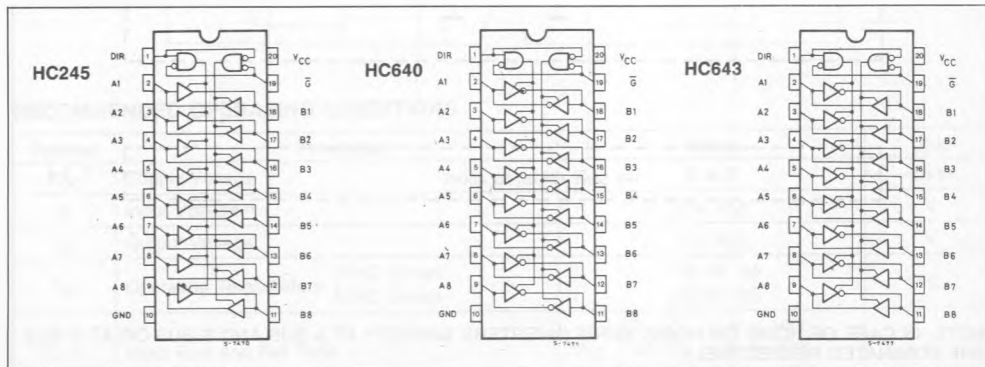
The M54/74HC245, M54HC640 and M54HC643 utilise silicon gate C²MOS technology to achieve operating speed equivalent to LSTTL devices. Along with the low power dissipation and high noise immunity of standard C²MOS integrated circuit, it possesses the driving capability of 15 LSTTL loads. These IC's are intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by DIR input. The enable input ($\bar{G}$) can be used to disable the device so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

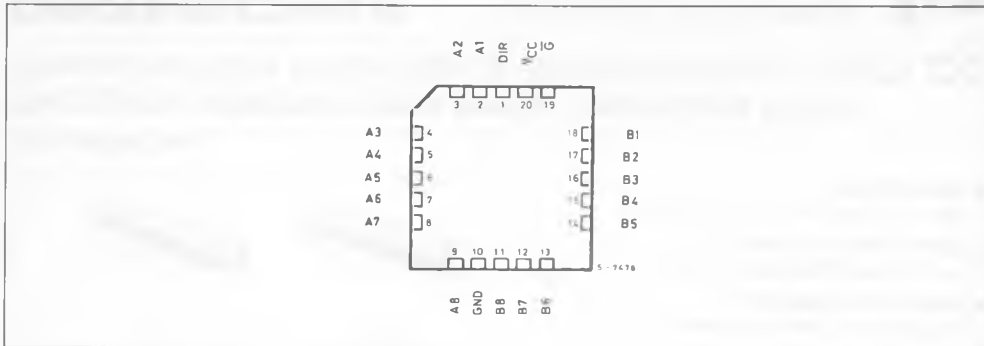
NOTICE FOR APPLICATION

IT IS PROHIBITED TO APPLY A SIGNAL TO A BUS TERMINAL WHEN IT IS IN OUTPUT MODE. AND WHEN A BUS TERMINAL IS FLOATING (HIGH IMPEDANCE STATE), IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

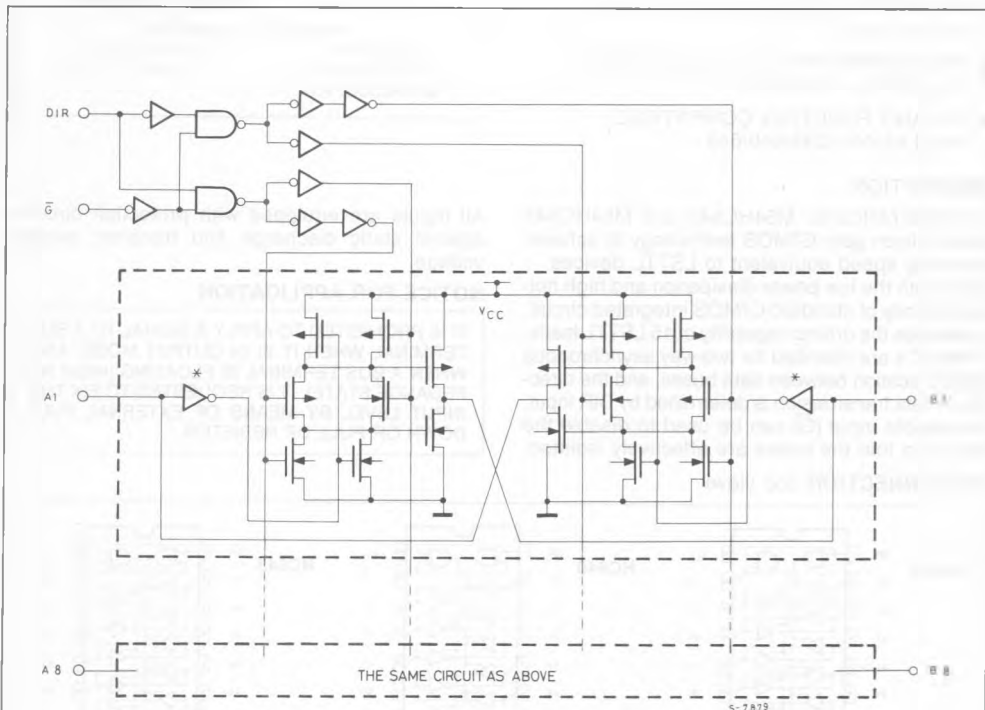
PIN CONNECTION (top view)



CHIP CARRIER



LOGIC DIAGRAM (HC640)



NOTE: IN CASE OF HC245 OR HC643, INPUT INVERTERS MARKED* AT A BUS AND B BUS OR AT B BUS ARE ELIMINATED RESPECTIVELY

TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HC245	HC640	HC643
L	L	OUTPUT	INPUT	A = B	A = $\overline{B}$	A = B
L	H	INPUT	OUTPUT	B = A	B = $\overline{A}$	B = $\overline{A}$
H	X	Z	Z	Z	Z	Z

X: "H" or "L" Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	- 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: $\cong$ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2 to 6	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _A	Operating Temperature 74HC Series 54HC Series	- 40 to 85 - 55 to 125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} $\begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	4.4	—	
		6.0	V _{IH} or V _{IL}	- 20 μA	5.9	6.0	—	5.9	—	5.9	—	
		4.5 6.0			- 6.0 mA - 7.8 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA		—	0.0	0.1	—	0.1	—	0.1
		4.5			—	0.0	0.1	—	0.1	—	0.1	—
		6.0	6.0 mA 7.8 mA	—	0.0	0.1	—	0.1	—	0.1	—	
		4.5 6.0		—	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40		
I _I	Input Leakage Current*	6.0	V _I = V _{CC} or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I _{OZ}	3-State Output Off-State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND		—	—	± 0.5	—	± 5.0	—	± 10	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND I _O = 0		—	—	4	—	40	—	80	μA

* Applicable only to DIR, G, $\overline{G}$ inputAC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transitio Time	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13	— — —	90 18 15	ns
t _{PLH} t _{PHL}	Propagation Delay Time (for HC245)	2.0 4.5 6.0		— — —	48 12 10	90 18 15	— — —	115 23 20	— — —	135 27 23	ns
t _{PLH} t _{PHL}	Propagation Delay Time (for HC640/643)	2.0 4.5 6.0		— — —	52 13 11	110 22 19	— — —	140 28 24	— — —	165 33 28	ns
t _{PZL} t _{PZH}	3 State Output Enable Time	2.0 4.5 6.0	R _L = 1kΩ	— — —	80 20 17	160 32 27	— — —	200 40 34	— — —	240 48 41	ns
t _{PLZ} t _{PHZ}	3 State Output Disable Time	2.0 4.5 6.0	R _L = 1kΩ	— — —	80 25 21	190 38 32	— — —	240 48 41	— — —	285 57 48	ns

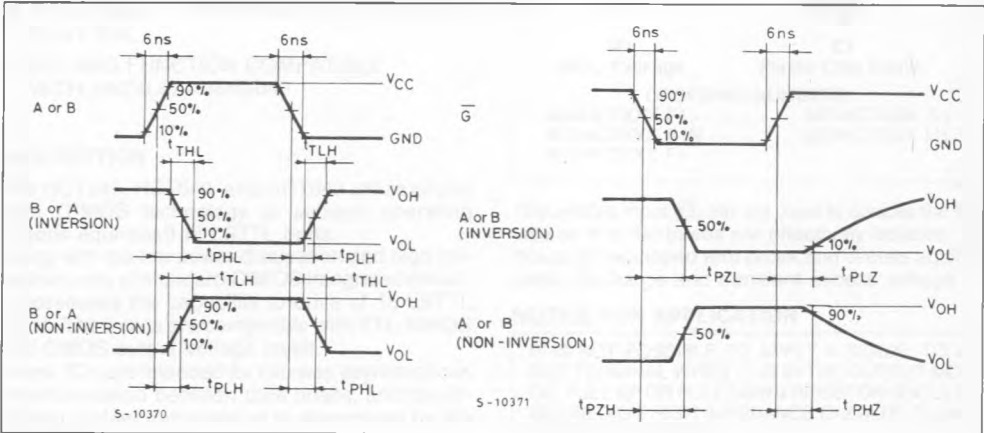
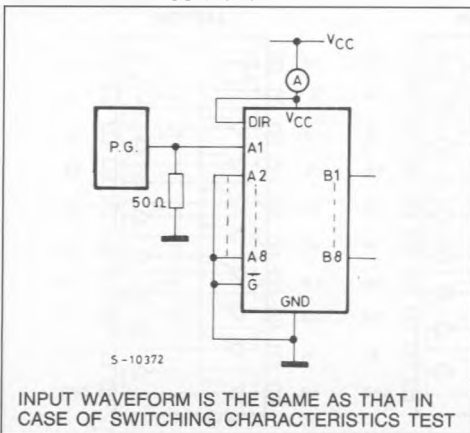
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C _{IN}	Input Capacitance		DIR, G, $\bar{G}$	—	5	10	—	10	—	10	pF
C _{I/O}	Bus Input Capacitance		A _n , B _n	—	13	—	—	—	—	—	pF
C _{PD} (*)	Power Dissipation Capacitance		HC245 HC640/643	—	33 40	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current is: I_{CC(opr)} = C_{PD} · V_{CC} · f_{IN} + I_{CC}/8 (per Circuit).

SWITCHING CHARACTERISTICS TEST WAVEFORM

TEST CIRCUIT I_{CC} (Opr.)C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC} \text{ (Opr.)}}{f_{IN} \cdot V_{CC}}$$