SGS-THOMSON MICROELECTRONICS

M54HC173
M74HC173

QUAD D-TYPE REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 52 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS173

B1N
Plastic Package

F1
Ceramic Frit Seal Package

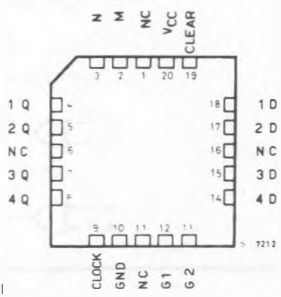
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCT173 F1
M74HCT173 B1N
M74HCT173 F1
M74HCT173 C1
M74HCT173 M1

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

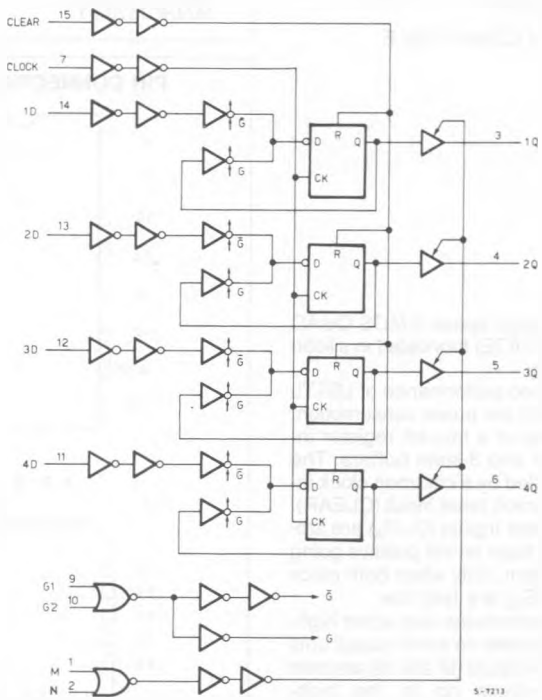
The M54/74HC173 is a high speed CMOS QUAD D-TYPE REGISTER (3-STATE) fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is composed of a four-bit register including D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common reset input (CLEAR). Signals applied to the data inputs (D_1-D_4) are stored at the respective flip-flops on the positive going transition of the clock input, only when both clock control inputs (G_1 and G_2) are held low.
The reset feature is asynchronous and active high. The stored data are provided on each output only when both output control inputs (M and N) are held low, otherwise the outputs go to the high-impedance state.
All inputs are equipped with protection circuits against static discharge and trasient excess voltage.

TRUTH TABLE

CLEAR	CLOCK	DATA ENABLE		Dn	OUTPUT CONTROL		Qn
		G1	G2		M	N	
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L	↓	X	X	X	L	L	Q0
L	↑	H	X	X	L	L	Q0
L	↑	X	H	X	L	L	Q0
L	↑	L	L	H	L	L	H
L	↑	L	L	L	L	L	L

X: DON'T CARE Z: HIGH IMPEDANCE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

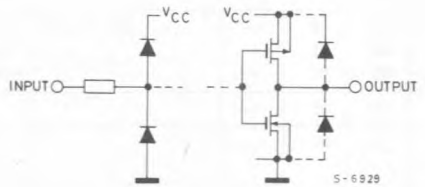
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5V	0 to 500	
			V_{CC} = 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.37	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.37	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1		±1	μA
I_{OZ}	3-State Output Off-State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40		80	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

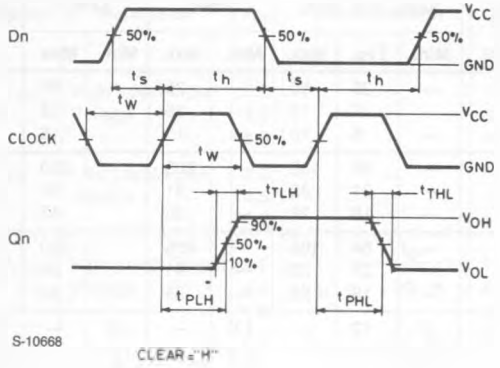
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75		90	ns
		4.5		—	7	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0		—	84	165	—	205		250	ns
		4.5		—	21	33	—	41		50	
		6.0		—	18	28	—	35		43	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR-Q)	2.0		—	84	165	—	205		250	ns
		4.5		—	21	33	—	41		50	
		6.0		—	18	28	—	35		43	
f_{MAX}	Maximum Clock Frequency	2.0		6	12	—	4.8	—	4.0	—	MHz
		4.5		30	50	—	24	—	20	—	
		6.0		35	59	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{REM}	Minimum Removal Time (CLEAR)	2.0		—	—	5	—	5		5	ns
		4.5		—	—	5	—	5		5	
		6.0		—	—	5	—	5		5	
t_s	Minimum Set-up Time (G_1, G_2)	2.0		—	40	100	—	125		150	ns
		4.5		—	10	20	—	25		30	
		6.0		—	9	17	—	21		26	
t_s	Minimum Set-up Time (D)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_h t_h	Minimum Hold Time (G_1,G_2,D)	2.0		—	—	0	—	0		0	ns
		4.5		—	—	0	—	0		0	
		6.0		—	—	0	—	0		0	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	R_L = 1 KΩ	—	65	120	—	150		180	ns
		4.5		—	13	24	—	30		36	
		6.0		—	11	20	—	26		31	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	R_L = 1 KΩ	—	84	150	—	190		225	ns
		4.5		—	21	30	—	38		45	
		6.0		—	18	26	—	33		38	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—			ns
C_{PD} (*)	Power Dissipation Capacitance			—	35	—	—	—			pF

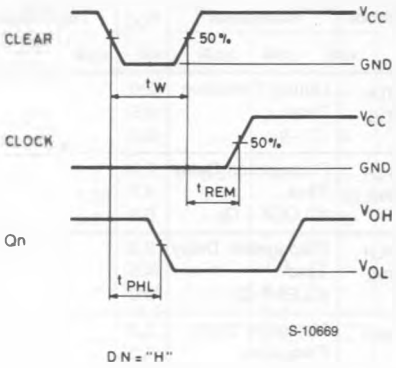
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

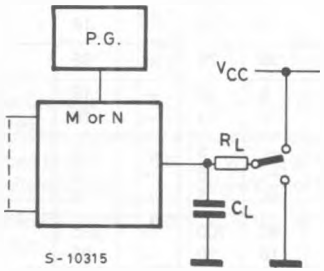
Average operating current can be obtained by the following equation.

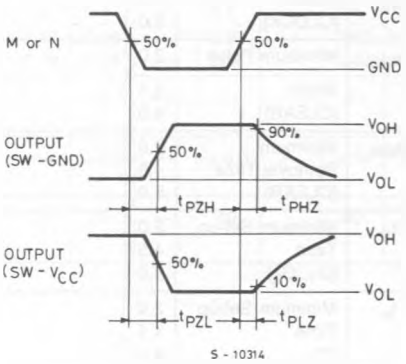
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM









EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

TEST CIRCUIT I_{CC} (Opr.)