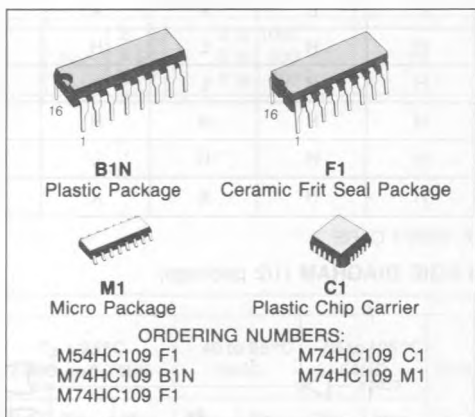


DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
 $f_{MAX} = 60 \text{ MHz (TYP.) at } V_{CC} = 5V$
- LOW POWER DISSIPATION
 $I_{CC} = 2 \mu A \text{ (MAX.) at } T_A = 25^\circ C$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = |I_{OL}| = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS109



DESCRIPTION

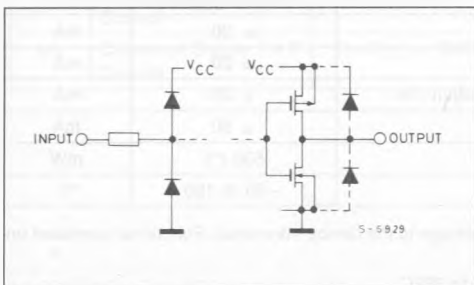
The M54/74HC109 is a high speed CMOS DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR fabricated in silicon gate CMOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

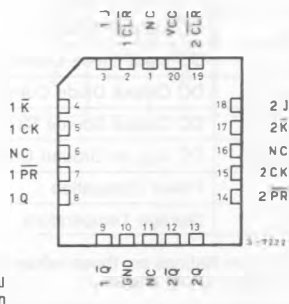
In accordance with the logic level on the J and K input is device changes state on positive going transitions of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



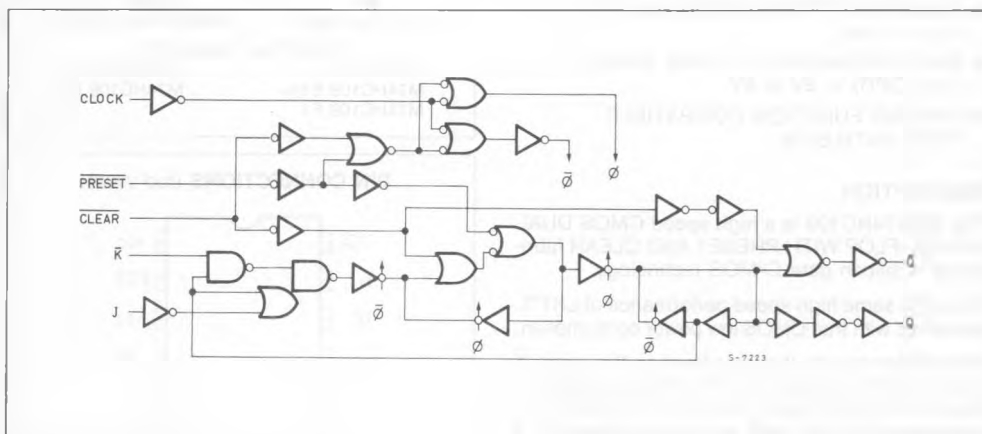
NC =
 No Internal
 Connection

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
CLR	PR	J	$\bar{K}$	CK	Q	$\bar{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	$\downarrow$	Qn	$\bar{Q}n$	NO CHANGE
H	H	L	L	$\downarrow$	L	H	
H	H	H	H	$\downarrow$	H	L	
H	H	H	L	$\downarrow$	$\bar{Q}n$	Qn	TOGGLE
H	H	X	X	$\downarrow$	Qn	$\bar{Q}n$	NO CHANGE

X: DON'T CARE

LOGIC DIAGRAM (1/2 package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to 150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: $\cong 65^{\circ}C$ derate to 300 mW by 10 mW/ $^{\circ}C$: $65^{\circ}C$ to $85^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	– 40 to 85 – 55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _I V _{IH} or V _{IL}	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		– 20 μA		4.4	4.5	—	4.4	—	4.4	—		
				5.9	6.0	—	5.9	—	5.9	—		
				4.5 6.0	– 4.0 mA – 5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND		—	—	±0.1	—	±1	—	±1	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\bar{Q}$)		18	29	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLR-Q, PR-Q, $\bar{Q}$)		21	33	ns
f_{MAX}	Maximum Clock Frequency	33	63		MHz

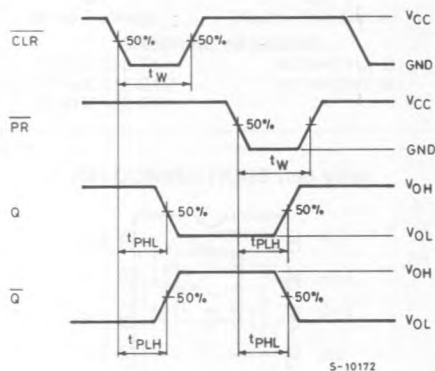
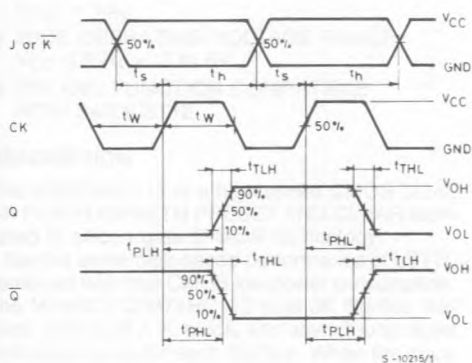
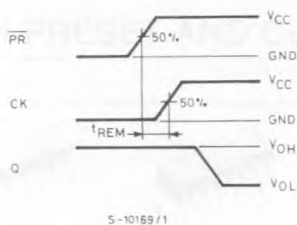
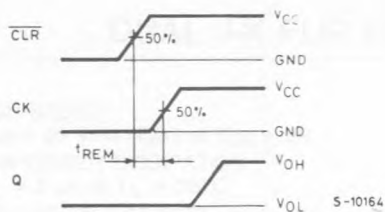
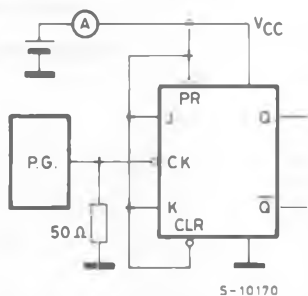
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ C$ 54HC and 74HC			- 40 to $85^\circ C$ 74HC		- 55 to $125^\circ C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\bar{Q}$)	2.0 4.5 6.0		— — —	80 21 18	165 33 28	— — —	205 41 35	— — —	250 50 43	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLR, PR-Q, $\bar{Q}$)	2.0 4.5 6.0		— — —	90 24 21	190 38 32	— — —	240 48 41	— — —	285 57 48	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	15 57 67	— — —	4.8 24 28	— — —	4 20 28	— — —	MHz
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width (CLR, PR)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-Up Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time (CLR, PR)	2.0 4.5 6.0		— — —	40 10 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	47	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation $I_{CC} (Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} \cdot I_{CC}/2$ (per FF)

SWITCHING CHARACTERISTICS TEST WAVEFORM

TEST CIRCUIT I_{CC} (Opr.)

INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.