M3493B2

CMOS 12 X 8 CROSSPOINT WITH CONTROL MEMORY

■ LOW ON RESISTANCE
  (typ. 60 Ω at V_{DD} = 10 V)
■ INTERNAL CONTROL LATCHES
■ ANALOG SIGNAL SWING CAPABILITY EQUAL
  TO POWER SUPPLY VOLTAGE APPLIED
■ LESS THAN 1 % TOTAL DISTORT. AT 0 dBm
■ LESS THAN – 95 dB CROSS-TALK
  AT 1 KHz 1 V_{PP}
■ VERY LOW POWER CONSUMPTION
■ PIN-TO-PIN COMPATIBLE WITH M093

DIP40

ORDERING NUMBER : M3493B2 (*)

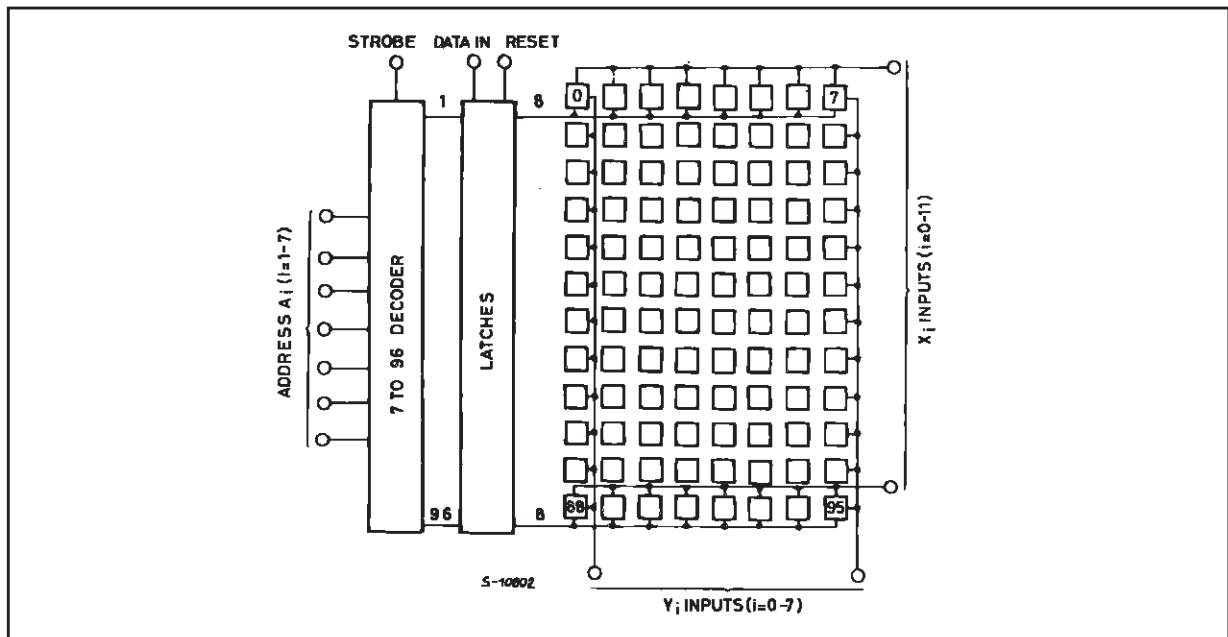(*) It substitutes the obsolete M3493B1.
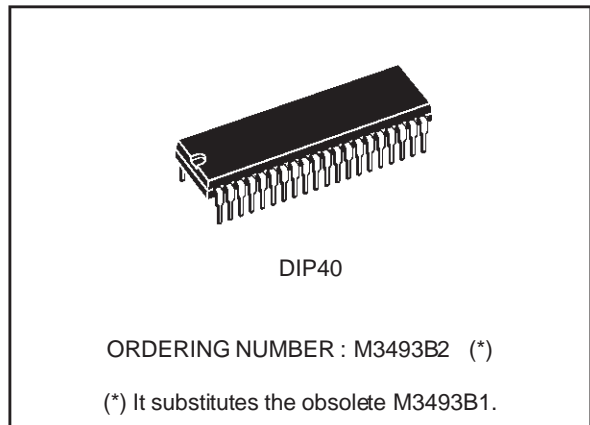
DESCRIPTION

The M3493 contains a 12 x 8 array of crosspoint together with a 7 to 96 line decoder and latch circuits. Anyone of the 96 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logi-
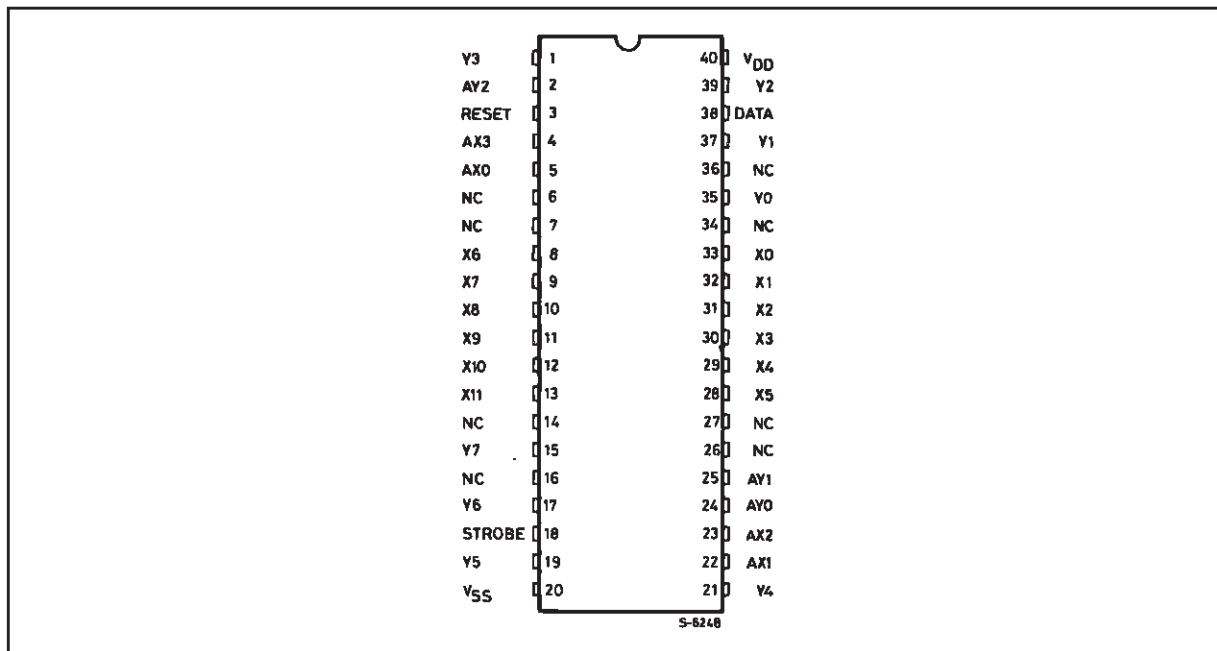
cal one. A reset signal can be used to turn off all the switches together when is switched at logical one.

M3493 is available in 40 lead dual in-line plastic package.

BLOCK DIAGRAM

PIN CONNECTION (top view)

```
           Y3    [ 1      40 ]  VDD
           AY2   [ 2      39 ]  Y2
          RESET  [ 3      38 ]  DATA
           AX3   [ 4      37 ]  Y1
           AX0   [ 5      36 ]  NC
            NC   [ 6      35 ]  Y0
            NC   [ 7      34 ]  NC
            X6   [ 8      33 ]  X0
            X7   [ 9      32 ]  X1
            X8   [ 10     31 ]  X2
            X9   [ 11     30 ]  X3
           X10   [ 12     29 ]  X4
           X11   [ 13     28 ]  X5
            NC   [ 14     27 ]  NC
            Y7   [ 15     26 ]  NC
            NC   [ 16     25 ]  AY1
            Y6   [ 17     24 ]  AY0
          STROBE [ 18     23 ]  AX2
            Y5   [ 19     22 ]  AX1
           VSS   [ 20     21 ]  Y4
                     S-6248
```

INPUT/OUTPUT DESCRIPTION

I/O	Symbol	Pin	Description
POWER			
I	V_{DD}	40	Positive Power Supply
I	V_{SS}	20	Negative Power Supply
ADDRESS			
I	AX0-AX3	4, 5, 22, 23	X Address Lines. These 4 pins are used to select one of the 12 rows of switches. Refer to the truth table for legal address.
I	AY0-AY2	2, 24, 25	Y Address Lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table for legal address.
CONTROL			
I	DATA	38	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
I	STROBE	18	This pin enables whatever action is selected by the ADDRESS and DATA pins. When the STROBE pin is held low, no switch openings or closings take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin)
I	RESET	3	Master Reset. This pin turns off (opens) all 96 switches. The states of the above control lines are irreleant. This pin is active high.
DATA			
I/O	X0-X11	8-13, 28-33	Analog Input/Outputs. These pins are connected to the Y0-Y7 pins in according to the truth table.
I/O	Y0-Y7	1,15,17,19,21 35,37,39	Analog Input/Outputs. These pins are connected to the X0-X15 pins in according to the truth table.

TRUTH TABLE

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
0*	1	1	0	0	0	0	No connection
1*	1	1	0	0	0	0	No connection
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
0*	1	1	1	0	0	0	No connection
1*	1	1	1	0	0	0	No connection
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ <0> ↓
1	0	1	1	1	0	0	X11 - Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	0	X11 - Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	0	X11 - Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	0	1	X11 - Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	1	X11 - Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	1	X11 - Y6

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC supply Voltage	- 0.5, 14	V
V_{IN}	Input Voltage Range	- 0.5, V_{DD} + 0.5	V
P_{tot}	Power Dissipation	1	W
T_{oper}	Operating Temperature Range	0, + 70	^{o}C
T_{stg}	Storage Temperature Range	- 50, + 125	^{o}C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	10	V
T_{oper}	Operating Temperature	0, + 70	^{o}C
V_{IN}	(Logic Signal)	0, V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{DD} = 10V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Supply Current	Reset = V_{DD}			1	mA
CROSSPOINT						
	On Resistance	V_{IDC} = 4.75V, V_{ODC} = 4.5V, See Figure 1		60	100	Ω
	On Resistance Variation			10	20	Ω
	Off-leakage *	All switches off V_{OS} = V_{IS} = 0 to V_{DD}			$\pm$ 3	μA
CONTROLS						
V_{IL}					0.8	V
V_{IH}			2.4			V
	Input Leakage *	V_{IN} = 0 to V_{DD}			$\pm$ 3	μA

* The device is guaranteed with such limits up to 70°C. At 25°C these limits become $\pm$ 100nA.

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, C_L = 50pF all input square wave rise and fall times = 10ns, V_{DD} = 10V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
CROSSPOINT							
t_{PHL}, t_{PLH}	Propagation Delay Time (switch on) Signal Input to Output	R_H = 1kΩ, V_{IS} = 2V_{PP}		30	100	ns	2
	Frequency Response (any switch on) 20 log (V_{OS}/V_{IS}) = -3dB	R_H = 81Ω, V_{IS} = 2V_{PP}, C_L = 3pF		50		MHz	
	Sine Wave Distortion	f_q = 1kHz, R_H = 0.6kΩ, V_{IS} = 8V_{PP}			1	%	
	Feed Through (any switches off)	f_q = 10kHz, R_H = 1kΩ, V_{IS} = 2V_{PP}	-80			dB	3
	Frequency for Signal Crosstalk Attenuation of 40dB Attenuation of 110dB	R_H = 1kΩ, V_{IS} = 2V_{PP}	1 5			MHz kHz	4
C	Capacitance Xn to Ground Vn to Ground Feed Through	f_q = 1MHz, V_{IS} = 0.1V_{PP}		15 15 0.4		pF	
C	Capacitance Logic Input to Ground	f_q = 1MHz, V_{IS} = 0.1V_{PP}		5		pF	
CONTROLS (t_r, t_f = 10ns)							
t_{PSN}	Propagation Delay Time Strobe to Output (switch turn-on to high level)			150	200	ns	5
t_{PZH}	Data-in to Output (turn-on to high level)			150	200	ns	6
t_{PAN}	Address to Output (turn-on to high level)			150	200	ns	7
t_{PSF}	Propagation Delay Time Strobe to Output (switch turn-off)			150	200	ns	5
t_{PZL}	Data-in to Output (turn-on to low level)			150	200	ns	6
t_{PAF}	Address to Output (turn-off)			150	200	ns	7
t_S	Set-up Time Data-in to Strobe	R_L = 1kΩ, C_L = 50pF	40			ns	5 10
t_H	Hold Time Data-in to Strobe		120			ns	5 10
t_O	Switching Frequency			1		MHz	
t_W	Strobe Pulse Width		100			ns	10
t_{WR}	Reset Pulse Width		150			ns	9
t_{PHZ}	Reset Turn-off to Output Delay			150	200	ns	9
t_{AS}	Address Set-up Time Address to Strobe		120			ns	10
t_{AH}	Address Hold Time Address to Strobe		120			ns	10
	Control Crosstalk Data-in, Address or Strobe to Output	Square wave input, V_{IN} = 3V, R_L = 10kΩ		75		mV	8

TEST CIRCUITS
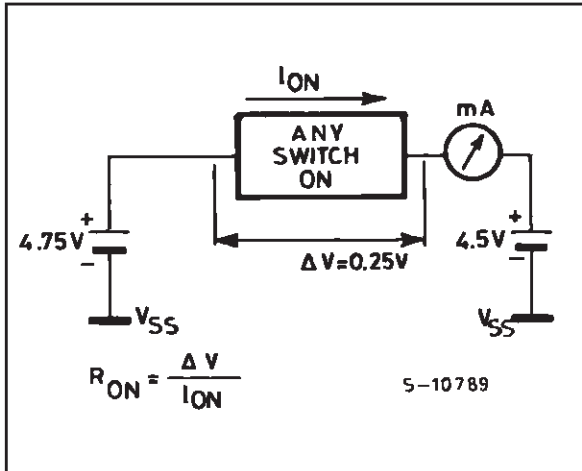
Figure 1 : R$_{ON}$ Measurement.

Figure 2 : Propagation Delay Time and Wave-
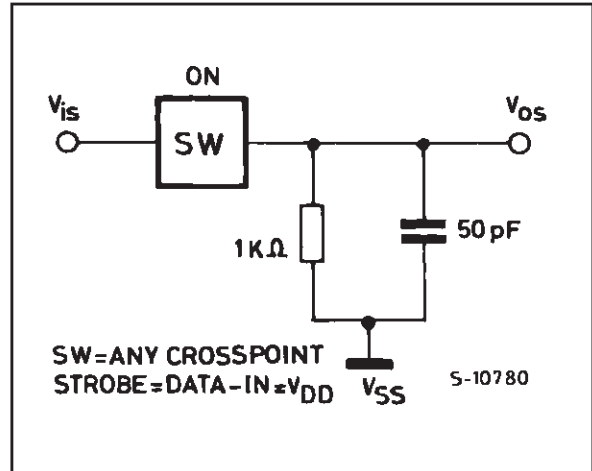forms (signal input to signal output
switch ON).

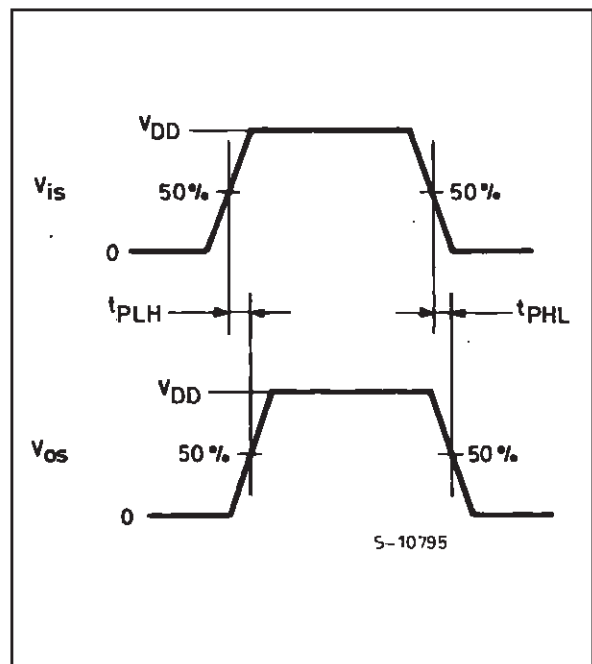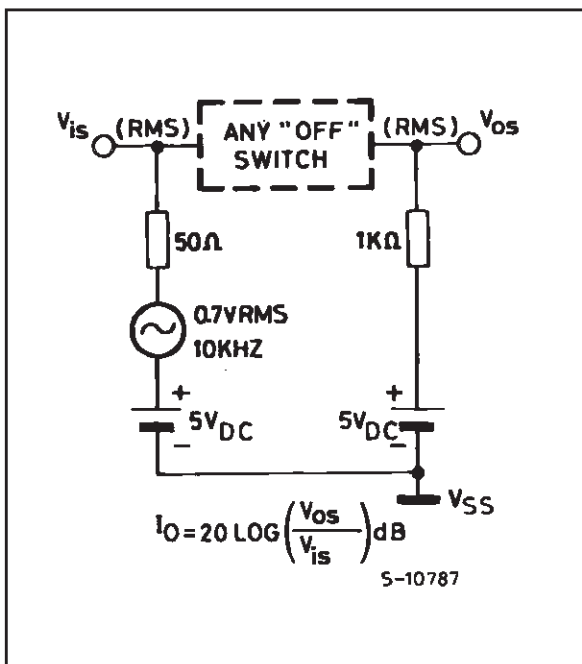Figure 3 : Off Isolation Measurement (Feed through).
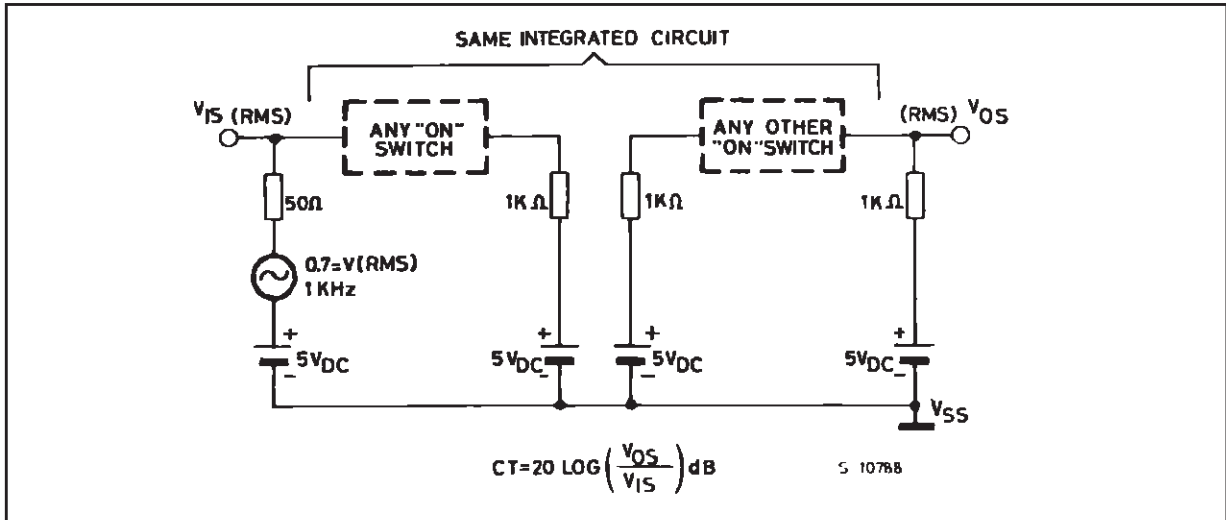
Figure 4 : Crosstalk Measurements.

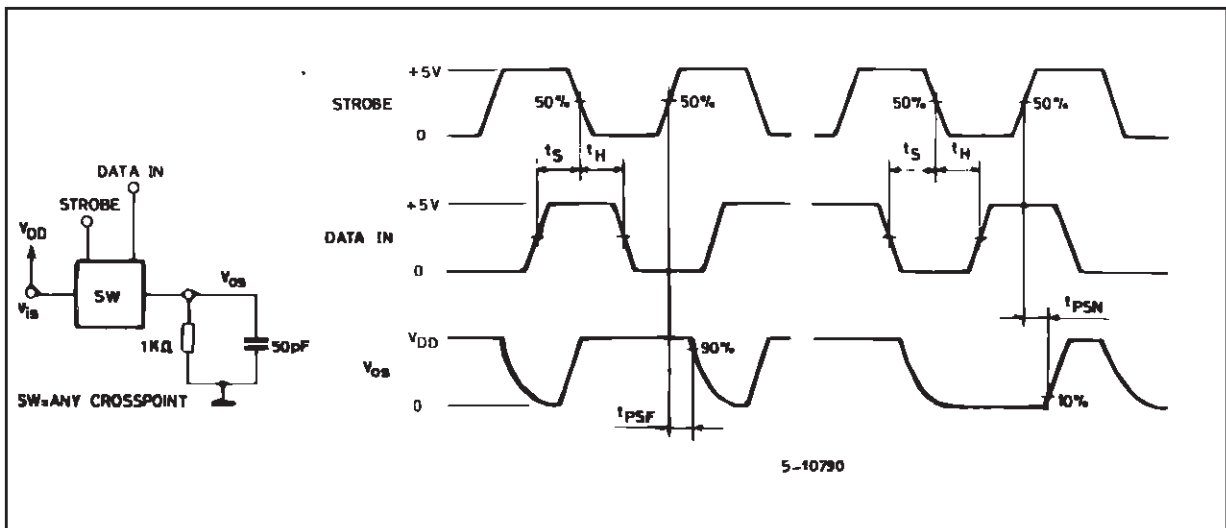Figure 5 : Propagation Delay Time and Waveforms (strobe to signal output switch Turn-ON or Turn-OFF).

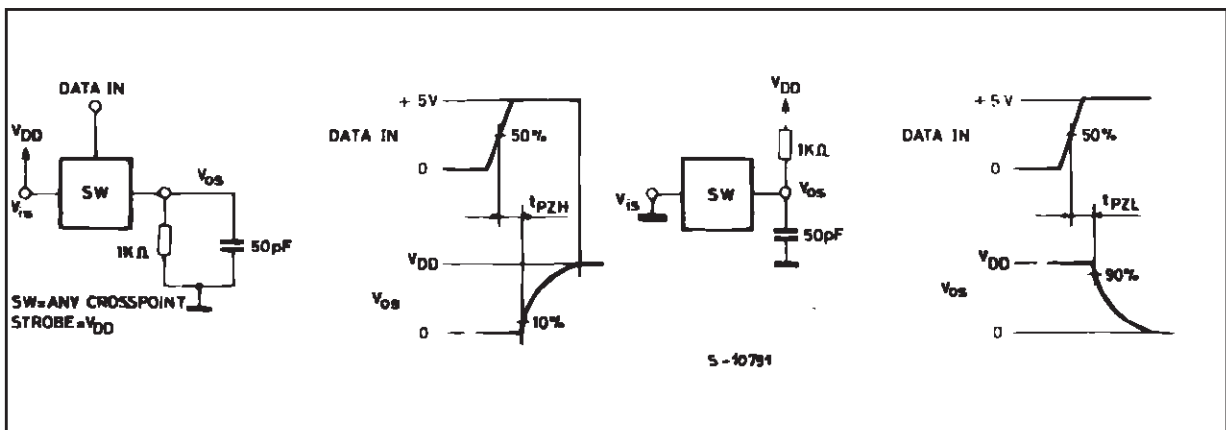Figure 6 : Propagation Delay Time and Waveforms (data-in signal output, switch Turn-ON to high or low level).

Figure 7 : Propagation Delay Time and Waveforms (address to signal output switch Turn-ON or Turn-OFF).
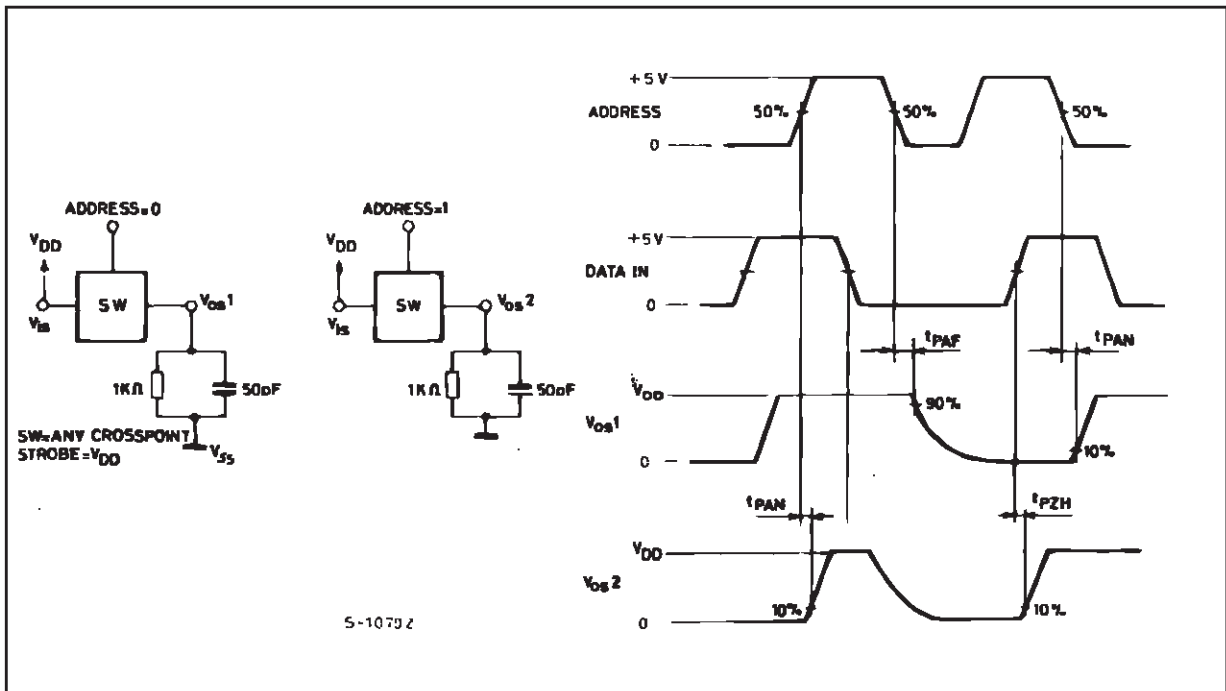
Figure 8 : Waveforms for Crosstalk (control input to signal output).
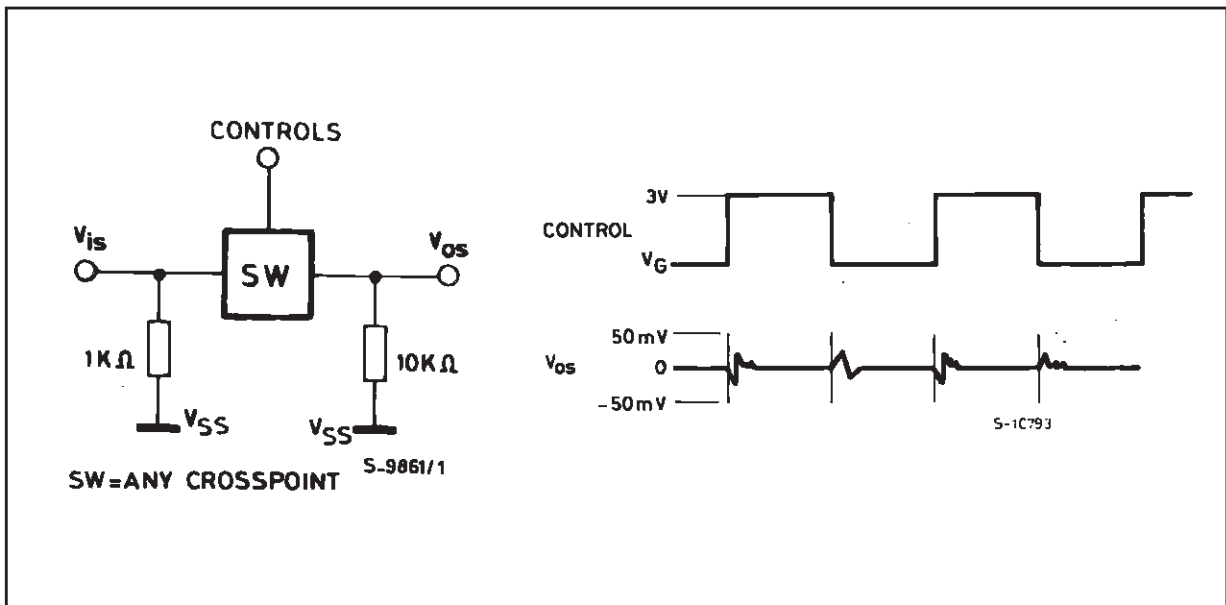
Figure 9 : Propagation Delay Time and Waveforms (reset to output delay).
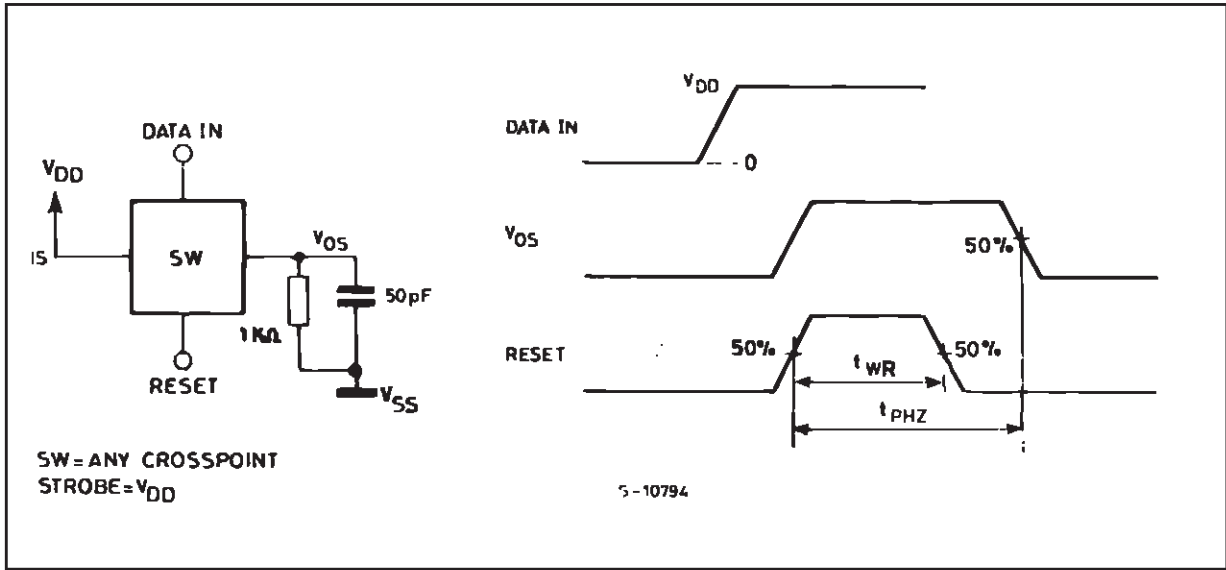
Figure 10 : Propagation Delay Time and Waveforms (Strobe and C/S to signal output switch).
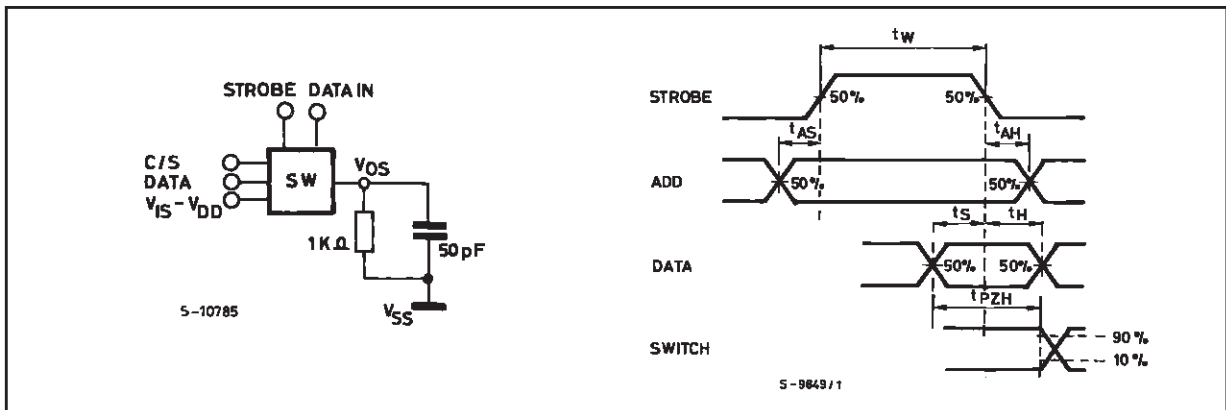
Figure 11 : Typical R$_{ON}$ versus V$_{is}$.
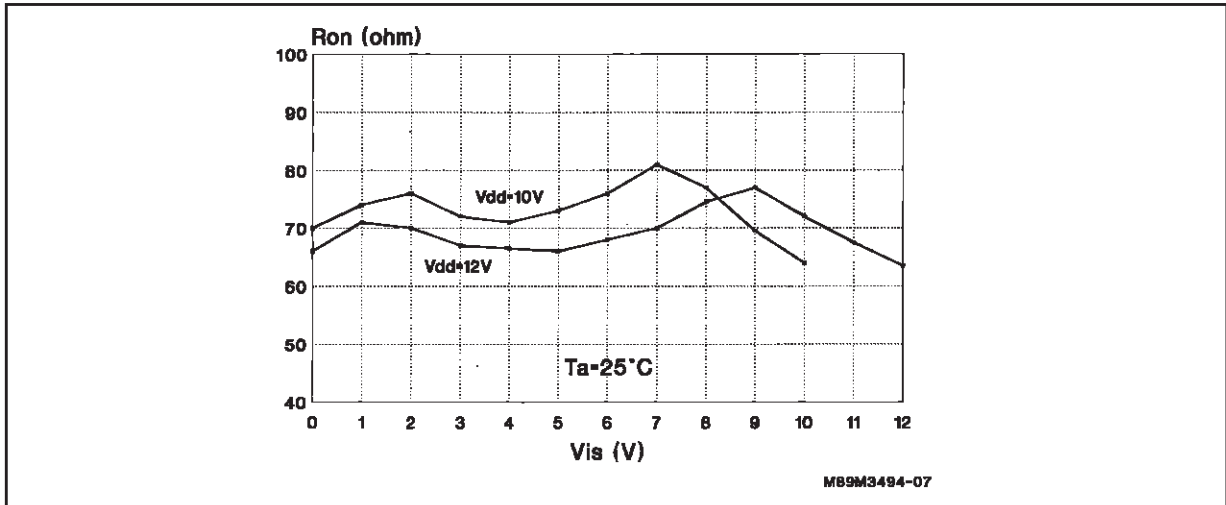
Figure 12 : Peak to Peak Voltage Capability versus Total Harmonic Distortion.
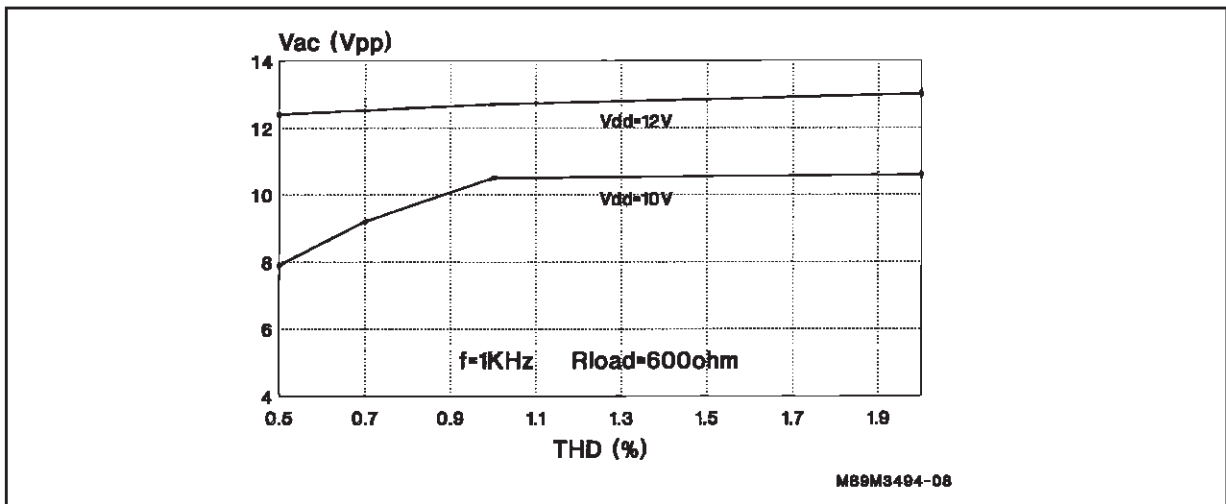
Figure 13 : V$_{RMS}$ Capability versus V$_{DD}$.
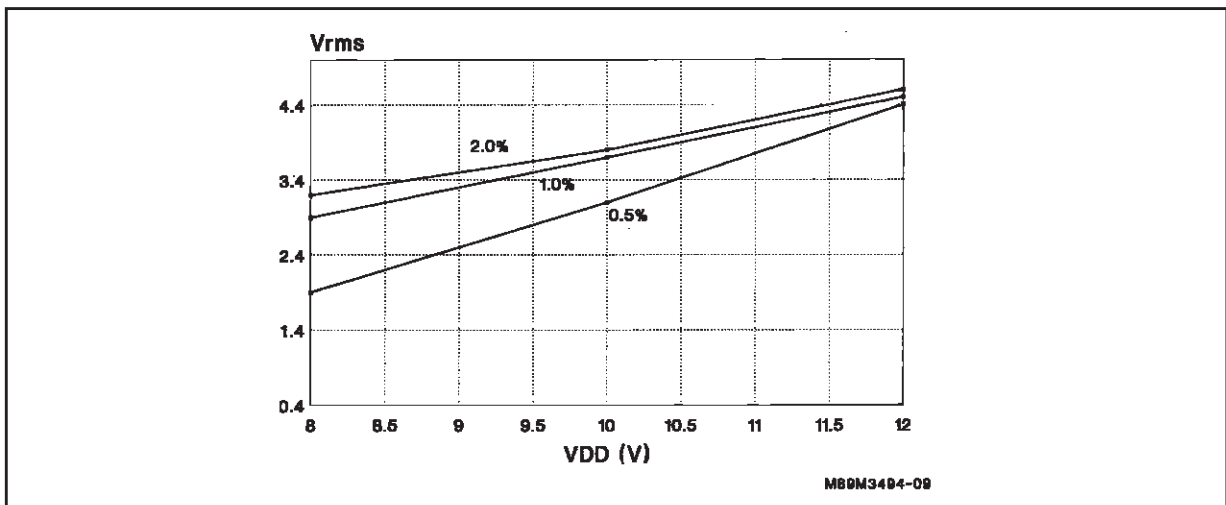
TYPICAL APPLICATIONS

The figures 14, 15 and 16 show the system configuration for expanded matrices (16 x 16, 8 x 64, 32 x 32).

Figure 14 : (16 x 16 non blocking matrix).
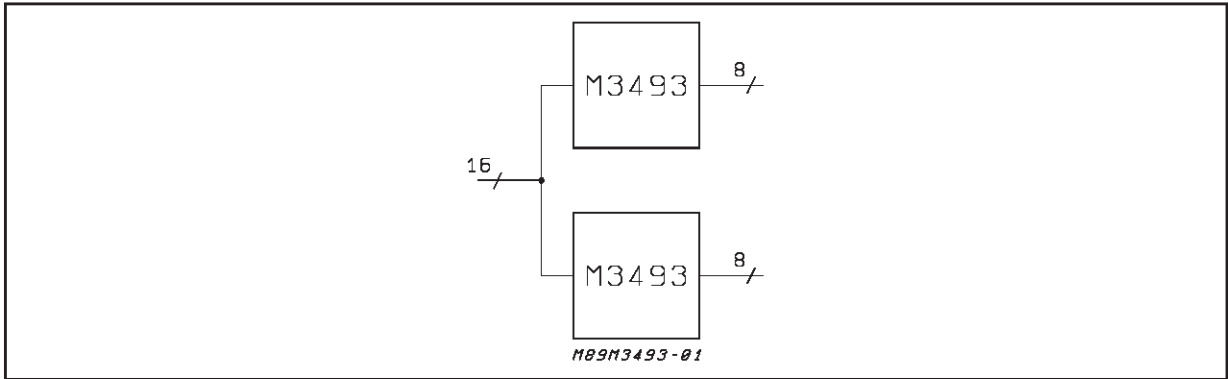
Figure 15 : (8 x 64 matrix).
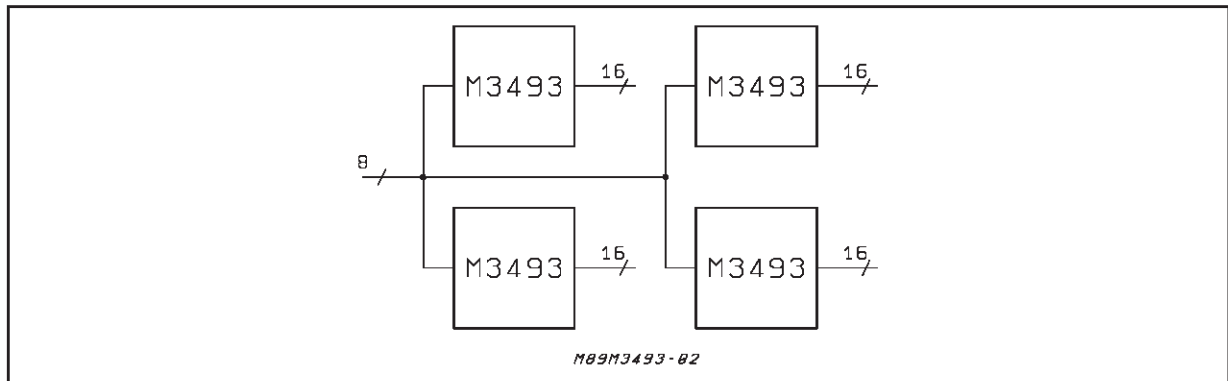
Figure 16 : (32 x 32 non blocking matrix).
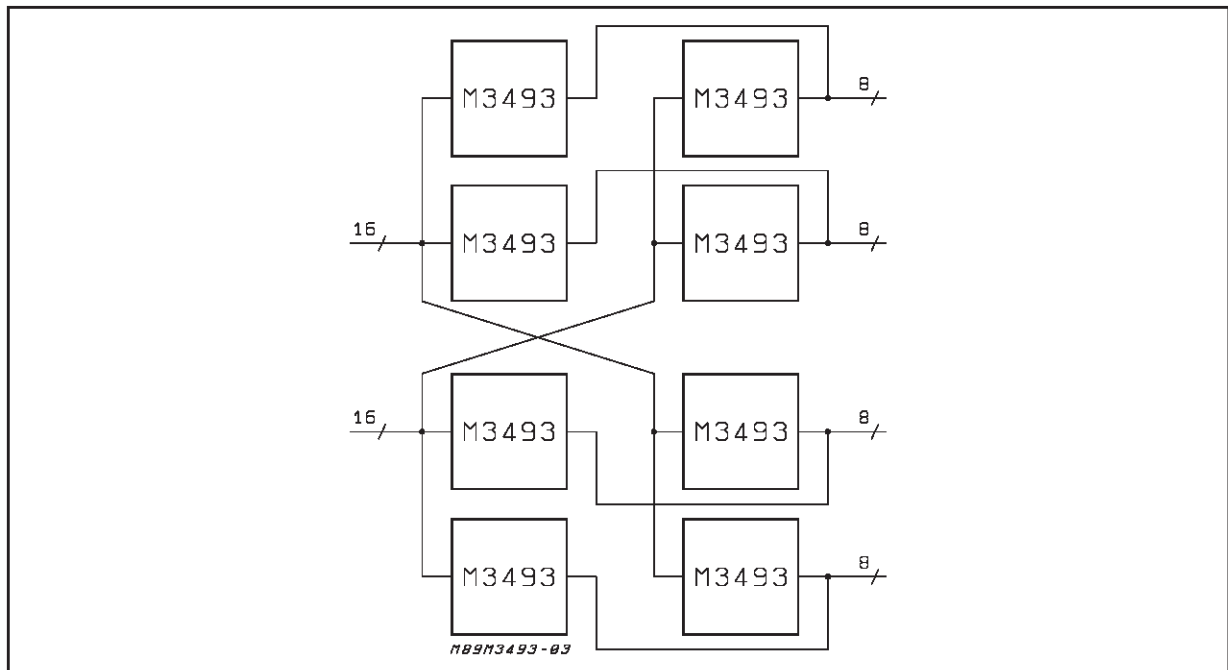
DIP40 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	