Ordering number : ENA1227A

SANYO Semiconductors
DATA SHEET

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CMOS IC

LV51130T — 2-Cell Lithium-Ion Secondary Battery Protection IC

Overview

The LV51130T is a protection IC for 2-cell lithium-ion secondary batteries.

Features

- Monitoring function for each cell: Detects overcharge and over-discharge conditions and controls the charging and discharging operation of each cell.
- High detection voltage accuracy: Over-charge detection accuracy ±25mV; Over-discharge detection accuracy ±100mV
- Hysteresis cancel function: The hysteresis of over-discharge detection voltage is cancelled by connection of a load after overcharging has been detected.
- Discharge current monitoring function: Detects over-currents, load shorting, and excessively high voltage of a charger.
- Low current consumption: Normal operation mode typ. 6.0µA; Stand by mode max. 0.2µA
- 0V cell charging function: Charging is enabled even when the cell voltage is 0V by giving a voltage between the V_{DD} pin and V^- pin.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
Power supply voltage		V_{DD}		-0.3 to +12	V
Input voltage Charger minus voltage		V^-		V_{DD}-28 to V_{DD}+0.3	V
Output voltage	Cout pin voltage	Vcout		V_{DD}-28 to V_{DD}+0.3	V
	Dout pin voltage	Vdout		V_{SS}-0.3 to V_{DD}+0.3	V
Allowable power dissipation		Pd max	Independent IC	170	mW
Operating ambient temperature		Topr		-30 to +85	°C
Storage temperature		Tstg		-40 to +125	°C

Electrical Characteristics at Ta = 25°C, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operation input voltage	Vcell	Voltage between V_{DD} and V_{SS}	1.5		10	V
0V cell charging minimum operation voltage	Vmin	Voltage between V_{DD}-V^- under V_{DD}-V_{SS} =0			1.5	V
Over-charge detection voltage	Vd1		4.325	4.350	4.375	V
		Ta=0 to 45°C *1	4.315	4.350	4.385	V
Over-charge release voltage	Vr1	$V^- \leq$ Vd3	4.100	4.150	4.200	V
		V^- > Vd3	4.250		4.360	V
Over-charge detection delay time	td1	V_{DD}-Vc=3.5V→4.5V, Vc-V_{SS}=3.5V	0.5	1.0	1.5	s
Over-charge release delay time	tr1	V_{DD}-Vc=4.5V→3.5V, Vc-V_{SS}=3.5V	20.0	40.0	60.0	ms
Over-discharge detection voltage	Vd2		2.20	2.30	2.40	V
Over-discharge release hysteresis voltage	Vh2		10.0	20.0	40.0	mV
Over-discharge detection delay time	td2	V_{DD}-Vc=3.5V→2.2V, Vc-V_{SS}=3.5V	50	100	150	ms
Over-discharge release delay time	tr2	V_{DD}-Vc=2.2V→3.5V, Vc-V_{SS}=3.5V	0.5	1.0	1.5	ms
Over-current detection voltage	Vd3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.28	0.30	0.32	V
Over-current release hysteresis voltage	Vh3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	5.0	10.0	20.0	mV
Over-current detection delay time	td3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	10.0	20.0	30.0	ms
Over-current release delay time	tr3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.5	1.0	1.5	ms
Short circuit detection voltage	Vd4	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	1.0	1.3	1.6	V
Short circuit detection delay time	td4	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.125	0.250	0.500	ms
Excessive charger detection voltage	Vd5	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V Voltage between V^- and V_{SS}	-0.60	-0.45	-0.30	V
Excessive charge detection release hysteresis voltage	Vh5	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	25.0	50.0	100.0	mV
Stand-by release voltage	Vstb	V_{DD}-Vc=2.0V, Vc-V_{SS}=2.0V Voltage between V^- and V_{SS}	V_{DD}×0.4	V_{DD}×0.5	V_{DD}×0.6	V
Excessive charger detection delay time	td5	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V *2	0.5	1.5	3.0	ms
Excessive charger release delay time	tr5	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.5	1.5	3.0	ms
Internal resistance (VM-V_{DD})	R_{DD}	After over-discharge is detected.	100	200	400	kΩ
Internal resistance (VM-V_{SS})	R_{SS}	After over-current or short-circuit is detected.	15	30	60	kΩ
Cout Nch ON voltage	$V_{OL}1$	I_{OL}=50μA, V_{DD}-Vc=4.4V, Vc-V_{SS}=4.4V			0.5	V
Cout Pch ON voltage	$V_{OH}1$	I_{OL}=50μA, V_{DD}-Vc=3.9V, Vc-V_{SS}=3.9V	V_{DD}-0.5			V
Dout Nch ON voltage	$V_{OL}2$	I_{OL}=50μA, V_{DD}-Vc=2.2V, Vc-V_{SS}=2.2V			0.5	V
Dout Pch ON voltage	$V_{OH}2$	I_{OL}=50μA, V_{DD}-Vc=3.9V, Vc-V_{SS}=3.9V	V_{DD}-0.5			V
Vc input current	Ivc	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V		0.0	1.0	μA
Current consumption	I_{DD}	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V		6.0	13.0	μA
Stand-by current	Istb	V_{DD}-Vc=2.2V, Vc-V_{SS}=3.5V			0.2	μA
T-terminal input ON voltage	Vtest	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	V_{DD}×0.4	V_{DD}×0.5	V_{DD}×0.6	V

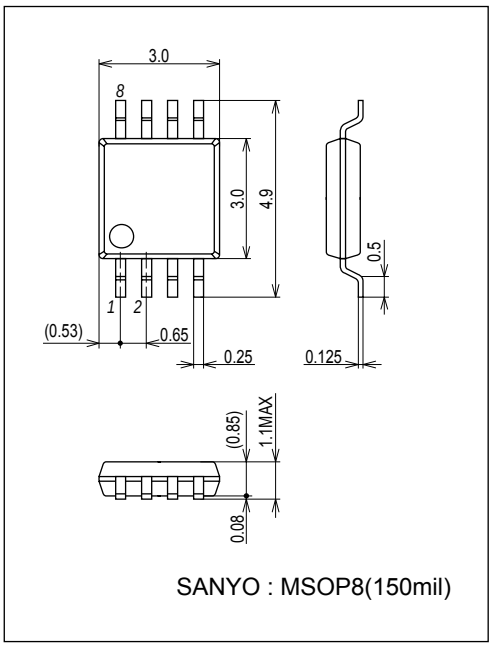
*1 The Ratings of the table above is a design targets and are not measured.

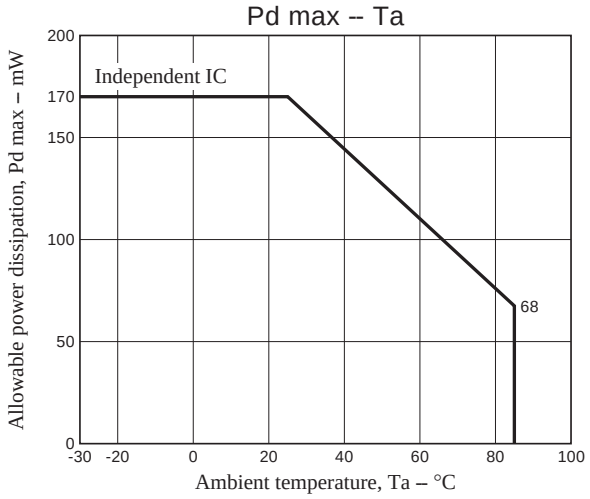
*2 Under over-discharge state, delay operation starts after release of over-discharge.

Package Dimensions

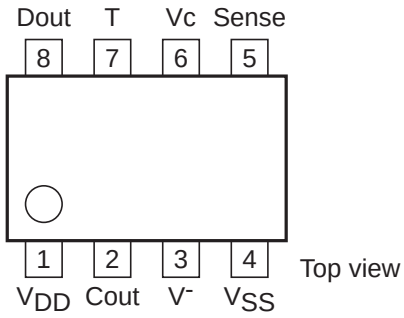
unit : mm (typ)

3245B





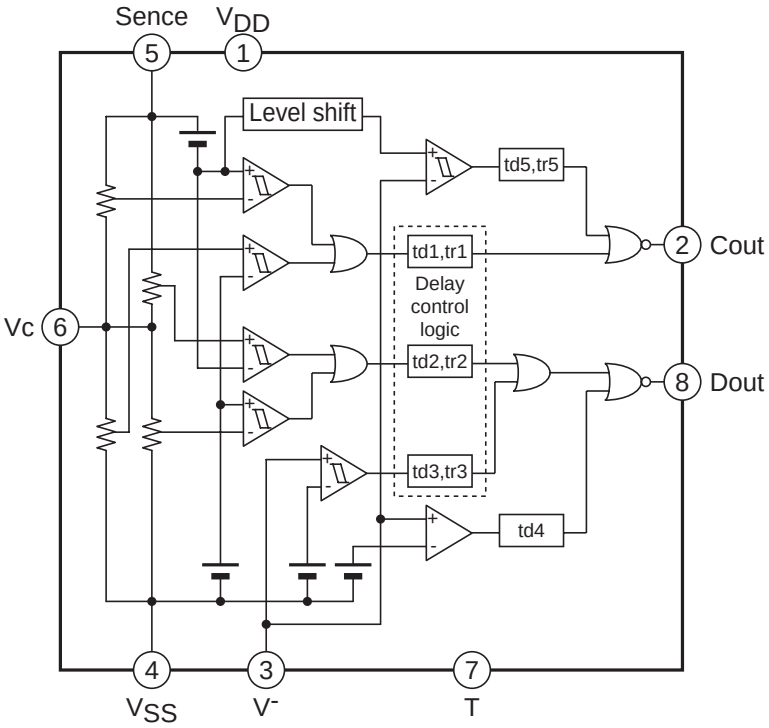
Pin Assignment



Pin Functions

Pin No.	Symbol	Description
1	V_{DD}	V_{DD} pin
2	Cout	Overcharge detection output pin
3	V^-	Charger minus voltage input pin
4	V_{SS}	V_{SS} pin
5	Sense	Sense pin
6	Vc	Intermediate between both cell voltage input pin
7	T	Pin to shorten detection time (“H”:Shortening mode, “L” or “Open”:Normal mode)
8	Dout	Overdischarge detection output pin

Block Diagram



Functional Description

Over-charge detection

If either of the cell voltage is equal to or more than the over-charge detection voltage, stop further charging by turning “L” the Cout pin and turning off external Nch MOS FET after the over-charge detection delay time. This delay time is set by the internal counter.

The over-charge detection comparator has the hysteresis function. Note that this hysteresis can be cancelled by connecting the load after detection of over-charge detection. and it becomes small hysteresis comparator has its own.

Once over-charge detection is made, over-current detection is not made to prevent incorrect operations. Note that short-circuit can be detected.

Over-charge release

If both cell voltages become equal to or less than the over-charge release voltage when VM voltage is equal to or less than Vd3, or when VM voltage is more than Vd3 with load connected, the Cout pin returns to “H” after the over-charge release delay time set by the internal counter.

When VM voltage is more than Vd3 with load connected and either cell or both cell voltages are equal to or more than the over-charge release voltage, the Cout pin does not return to “H”. But the load current flows through the parasitic diode of external Nch MOS FET on Cout, consequently each cell voltage becomes equal to or less than over-charge release voltage, the Cout pin returns to “H.” after the over-charge release delay time.

However, excessive voltage charger is connected as mentioned below, Cout pin does not return to “H” because excessive charger detection starts after over-charge release operation.

Over-discharge detection

When either cell voltage is equal to or less than over-discharge voltage, the IC stops further discharging by turning the Dout pin “L” and turning off external Nch MOS FET after the over-charge detection delay time.

The IC goes into stand-by mode after detecting over-discharge and its consumption current is kept at about 0A. After over-discharge detection, the V^- pin will be connected to V_{DD} pin via internal resistor (typ 200kΩ).

Over-discharge release

Release from over-discharge is made by only connecting charger. If the V^- pin voltage becomes equal to or lower than the stand-by release voltage by connecting charger after detecting over-discharge, The IC is released from the stand-by state to start cell voltage monitoring. While both cell voltages are equal to or less than over-discharge voltages, charging will be made through the parasitic diode of external Nch FET on Dout pin. If both cell voltages become equal to or more than the over-discharge detection voltage by charging, the Dout pin returns to “H” after the over-discharge release delay time set by the internal counter.

Over-current detection

When excessive current flows through the battery, the V^- pin voltage rises by the ON resister of external MOS FET and becomes equal to or more than the over-current detection voltage, the Dout pin turns to “L” after the over-current detection delay time and the external Nch MOS FET is turned off to prevent excessive current in the circuit. The detection delay time is set by the internal counter. After detection, the V^- pin will be connected to V_{SS} via internal resistor (typ. 30kΩ). It will not go into stand-by mode after detecting over-current.

Short circuit detection

If greater discharging current flows through the battery and the V^- pin voltage becomes equal to or more than the short-circuit detection voltage, it will go into short-circuit detection state after the short circuit delay time shorter than the over-current detection delay time. When short-circuit is detected, just like the time of over-current detection, the Dout pin turns to “L” and external Nch MOS FET is turned off to prevent high current in the circuit. The V^- pin will be connected to V_{SS} after detection via internal resistor (typ. 30kΩ). It will not go into stand-by mode after detecting short circuit.

Over-current/short-detection release

After detecting over-current or short circuit, the internal resistor (typ. 30kΩ) between V^- pin and V_{SS} pin becomes effective. If the load resistor is removed, the V^- pin voltage will be pulled down to the V_{SS} level. Thereafter, the IC will be released from the over-current/short-circuit detection state when the V^- pin voltage becomes equal to or less than the over-current detection voltage, and the Dout pin returns to “H” after over-current release delay time set by the internal counter.

Excessive charger detection/release

If the voltage between V^- pin and V_{SS} pin becomes equal to or less than the excessive charger detection voltage by connecting a charger, no charging can be made by turning the Cout pin "L" after delay time and turning off the external Nch MOS FET. If that voltage returns to equal to or more than the excessive charger detection voltage during detection delay time, the excessive charger detection will be stopped. If the voltage between V^- pin and V_{SS} pin becomes equal to or more than the excessive charger detection voltage after excessive charger detection, the Cout returns to "H" after delay time. The detection/return delay time is set internally.

If Dout pin is "L", charging will be made through the parasitic diode of external Nch FET on Dout pin. In that case, the voltage between V^- pin and V_{SS} pin is nearly -Vf which is less than the excessive-charger detection voltage, therefore no excessive charger detection will be made during over-discharge, over-current and short-circuit detection. Furthermore, if excessive voltage charger is connected to the over-discharged battery, no excessive charger detection is made while the Dout pin is "L". But the battery is continued charging through the parasitic diode. If the battery voltage rises to the over-discharge detection voltage and the voltage between V^- pin and V_{SS} pin remains equal to or less than the excessive charger detection voltage, the delay operation will be started after Dout pin turns to "H."

0V cell charging operation

If voltage between V_{DD} and V becomes equal to or more than the 0V cell charging lowest operation voltage when the cell voltage is 0V, the Cout pin turns to "H" and charging is enabled.

Shorten the test time

By turning T pin to the V_{DD} , the delay times set by the internal counter can be cut. If T pin is "open", "L" the delay times are normal. Delay time not set by the counter just like as short circuit detection delay cannot be controlled by this pin.

In some circuit-board layout, an excessive current at the load short might cause this IC be in miss operation like as in standby mode due to V_{SS} line impedance. Therefore we recommend that the T pin is connected to the V_{SS} pin.

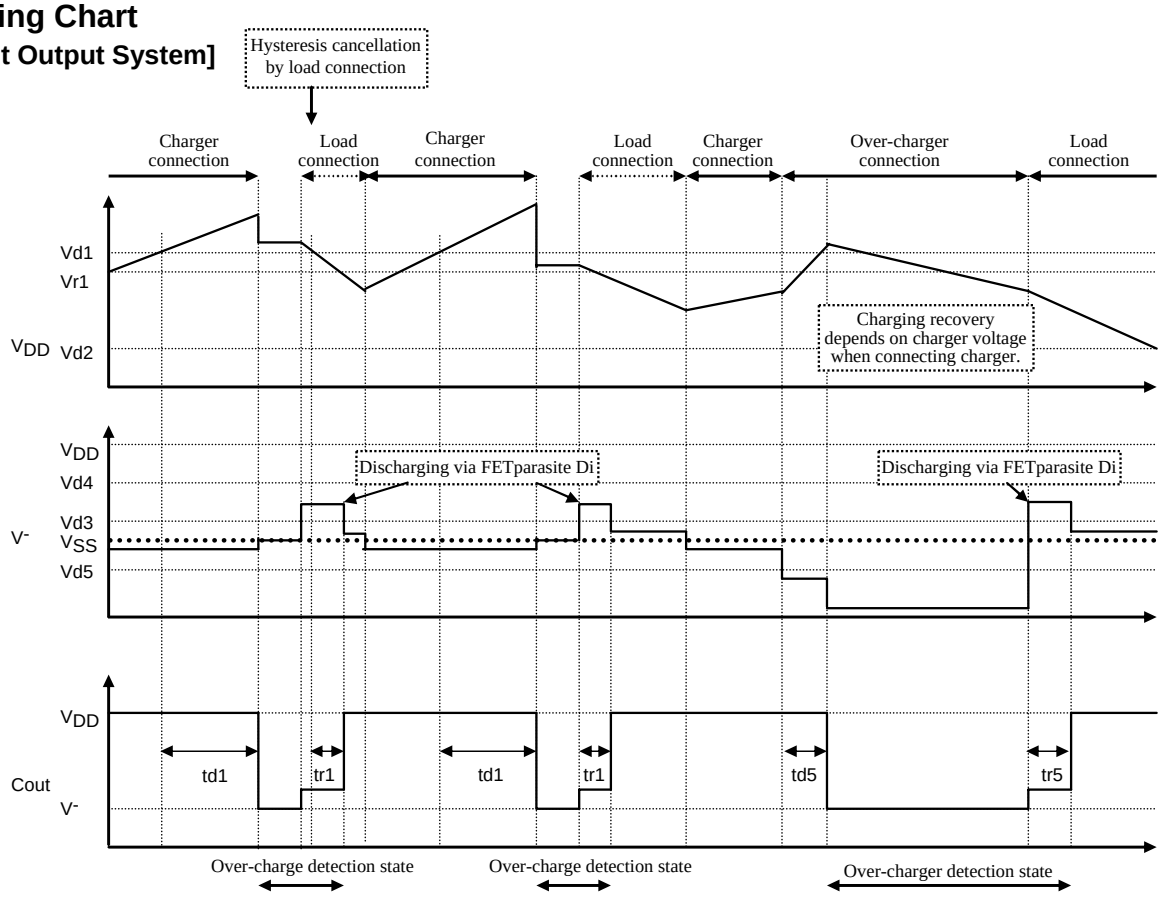
Operation in case of detection overlap

Overlap state		Operation in case of detection overlap	State after detection
During over-charge detection	Over-discharge detection is made	Over-charge detection is preferred. If over-discharge state continues even after over-charge detection, over-discharge detection is resumed.	When over-charge state is made first, V^- is released. When over-discharge is detected after over-charge state is made, the IC does not go into the stand-by mode. Note that V^- is connected to V_{DD} via 200kΩ.
	Over-current detection is made	(*1) Both detections can be made in parallel. Over-charge detection continues even when the over-current state is made first. If the over-charge state is made first, over-current detection is interrupted.	(*2) When over-current state is made first, V^- is connected to V_{SS} via 30kΩ. When over-charge state is made first, V^- is released.
During over-discharge detection	Over-charge detection is made	Over-discharge detection is interrupted and over-charge detection is preferred. When over-discharge state continues even after over-charge state is made, over-discharge detection is resumed.	The IC does not go into the stand-by mode when over-discharge state is made after over-charge detection. Note that V^- is connected to V_{DD} via 200kΩ.
	Over-current detection is made	(*3) Both detections can be made in parallel. Over-discharge detection continues even when the over-current state is made first. But over-current detection is interrupted when the over-discharge state is made first.	(*4) If over-current state is made first, V^- will be connected to V_{SS} via 30kΩ. If over-discharge detection is made next, V^- will be disconnected from V_{SS} and connected to V_{DD} via 200kΩ to get into stand-by mode. If over-discharge state is made first, V^- will be connected to V_{DD} via 200kΩ to get into standby state.
During over-current detection	Over-charge detection is made	(*1)	(*2)
	Over-discharge detection is made	(*3)	(*4)

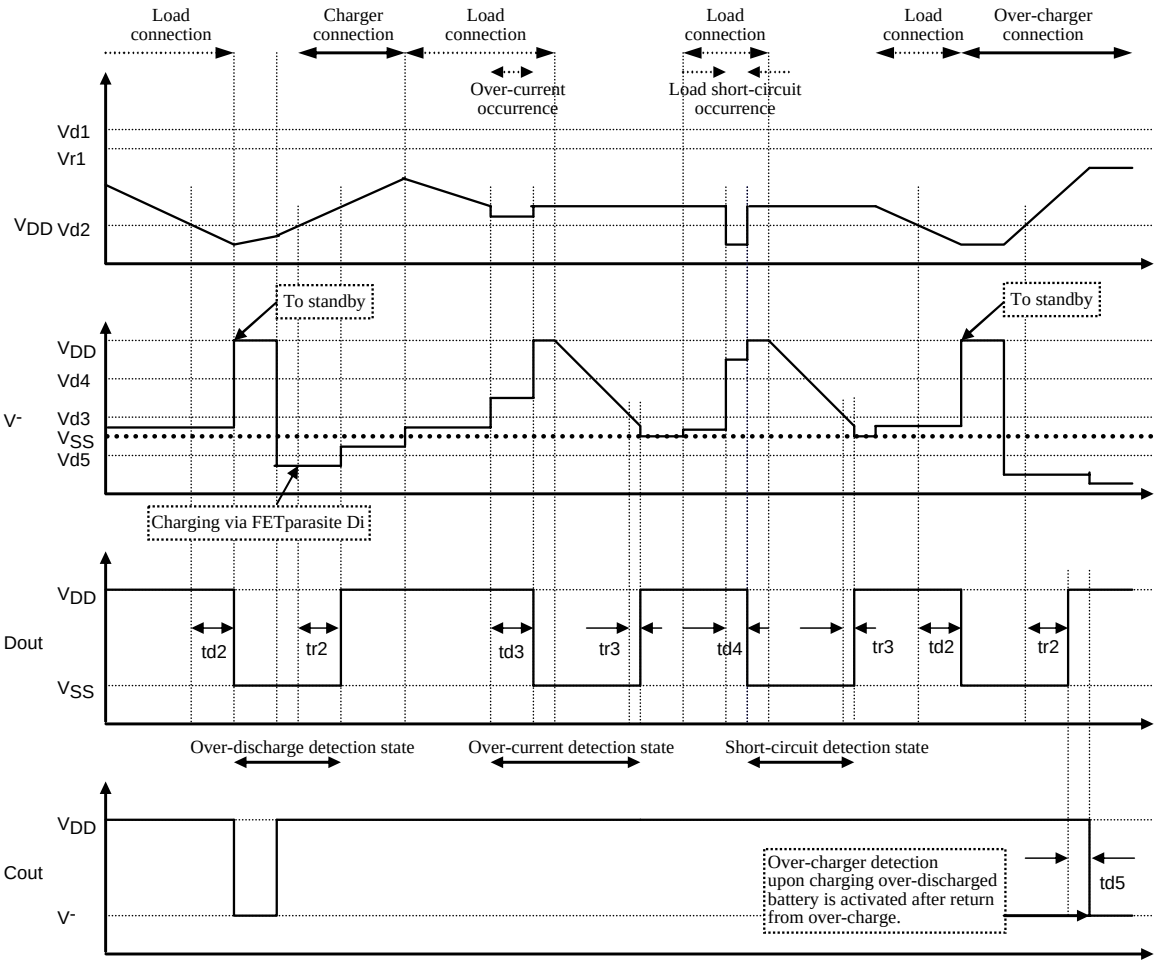
(Note) Short-circuit detection can be made independently.
Excessive charger detection cannot be made during over-discharge, over-current and short-circuit detection. And its delay time starts after the Dout pin returns to "H".

Timing Chart

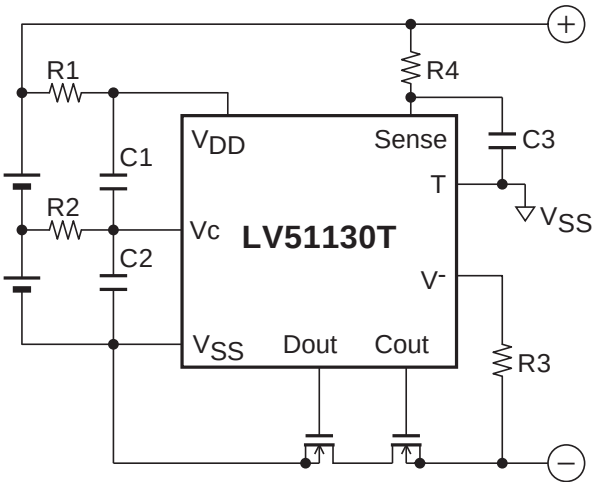
[Cout Output System]



[Dout Output System]



Application Circuit Example



Components	Recommended value	max	unit
R1, R2	100	500	Ω
R3	2k	4k	Ω
R4	100	1k	Ω
C1, C2, C3	0.1μ	1μ	F

* These numbers don't mean to guarantee the characteristic of the IC.
* In addition to the components in the upper diagram, it is necessary to insert a capacitor with enough capacity between V_{DD} and V_{SS} of the IC as near as possible to stabilize the power supply voltage to the IC.
* It is advisable to connect the T pin with the V_{SS} pin. There is no problem even if the T pin is left open.