Ordering number : ENA1823

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LV0221CS — Monolithic Linear IC For Optical Pickups Front Monitor OE-IC

Overview

The LV0221CS is a front monitor optoelectronic IC for optical pickups that has a built-in photo diode compatible with three waveforms. LV0221CS is small size and type CSP packages.

Functions

- PIN photodiode compatible with three wavelengths incorporated.
- Gain adjustment (-6dB to +6dB in 256 steps) through serial communication.
- Amplifier to amplify differential output.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}		6	V
Allowable power dissipation	Pd1	Glass epoxy one-side substrate 55mm × 45mm × 0.8mm Copper foil area (about 80%), Ta=75˚C	136	mW
	Pd2	Glass epoxy one-side substrate 55mm × 45mm × 0.8mm Copper foil area (head: about 85% Tail: about 90%), Ta=75˚C	100	mW
Operating temperature	Topr		-20 to +85	˚C
Storage temperature	Tstg		-40 to +100	˚C

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	V_{CC}		4.5	5	5.5	V
Output load capacitance	C_O		12	20	33	pF
Output load resistance	Z_O		3			kΩ

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, RL=6kΩ, CL=20pF

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current dissipation	I_{CC}			18	23.4	mA
Sleep current	Islp				1	mA
Output voltage when shielded	V_C	At shielding	1.8	2.0	2.2	V
Output offset voltage	Vofs	At shielding, voltage between VOP-VON	-30	0	30	mV
Temperature dependence of offset voltage *1	Vofs	Ta=-10 to +85˚C	-60	0	60	μV/˚C
Optical output voltage *1 Voltage between VOP-VON	VLC	Low Gain, λ=780nm, G=0dB	0.21	0.262	0.31	mV/μW
	VLD	Low Gain, λ=650nm, G=0dB	0.22	0.275	0.33	mV/μW
	VLB	Low Gain, λ=405nm, G=0dB	0.14	0.172	0.21	mV/μW
	VMC	Middle Gain, λ=780nm, G=0dB	0.66	0.83	0.99	mV/μW
	VMD	Middle Gain, λ=650nm, G=0dB	0.70	0.87	1.05	mV/μW
	VMB	Middle Gain, λ=405nm, G=0dB	0.43	0.54	0.65	mV/μW
	VHC	High Gain, λ=780nm, G=0dB	1.97	2.46	2.95	mV/μW
	VHD	High Gain, λ=650nm, G=0dB	2.07	2.58	3.10	mV/μW
	VHB	High Gain, λ=405nm, G=0dB	1.29	1.62	1.94	mV/μW
Light output voltage adjustment range *1	G	G=0dB reference, absolute value of adjustment width	5.5	6.0	6.5	dB
D range *1	VoD	Voltage between VOP-VON	1700	2200		mV
Frequency characteristics *1, *2	FcC	-3dB(1MHz reference), λ=780nm Light input = 40μW(DC) + 20μW(AC)	50	75		MHz
	FcD	-3dB(1MHz reference), λ=650nm Light input = 40μW(DC) + 20μW(AC)	60	85		MHz
	FcB	-3dB(1MHz reference), λ=405nm Light input = 40μW(DC) + 20μW(AC)	60	85		MHz
Settling time *1	Tset			15		ns
Response time *1	Tr, Tf	Vo=0.9Vp-p, output level 10 to 90% fc=10MHz, duty=50%			10	ns
Overshoot *1	Ovst	Vo=0.9Vp-p			15	%
Undershoot *1	Unst	Vo=0.9Vp-p			15	%
Linearity *1	Lin	At output voltage 0.5V and 1.0V (Between VOP-VON)	-1	0	1	%
Light-output voltage temperature dependence Voltage between VOP-VON *1, *3	TC	λ=780nm, 25˚C reference	10	13	16	%
	TD	λ=650nm, 25˚C reference	0	3	6	%
	TB	λ=405nm, 25˚C reference	0	3	6	%
Light-output voltage spectral sensitivity Voltage between VOP-VON *1	Vf	λ=785nm ±10nm	-0.8		0.1	%/nm
		λ=660nm ±10nm	-0.4		0.4	%/nm
		λ=405nm ±10nm	0		1.2	%/nm
Step-step voltage ratio *1	DG	(Vn-Vn-1) / Vn *100 *4 Deviation from the ideal curve of above equation	-3	0	3	%

Item with *1 mark indicate the design reference value.

Item with *2 mark indicate the frequency characteristics when VOP and VON are applied individually.

The frequency characteristics are for the case of High / Middle / Low gain and for the case when the output voltage adjustment range is -6 to +6dB

Item with *3 mark indicates the temperature dependence for the case of High / Middle / Low gain and for the case when the temperature is 25 to 85˚C for the output voltage adjustment range of -6 to +6dB

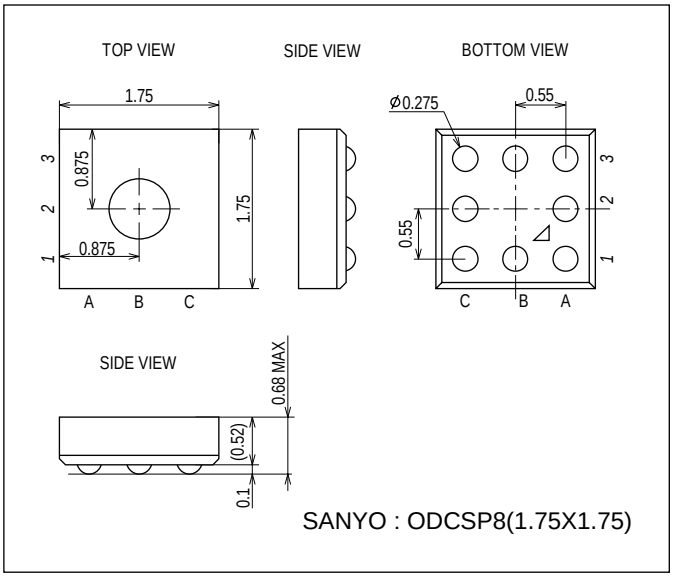
Vn in Item with *4 mark is Vn = (sensitivity / 2) × 5400 / (5400-16 × GCAstep) × light intensity (μW)

GCA = Gain Control Amplifier

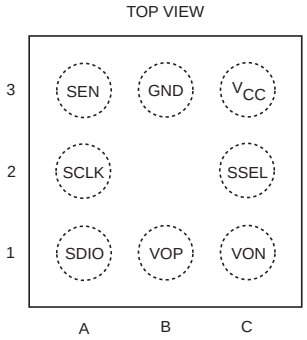
Package Dimensions

unit : mm (typ)

3402

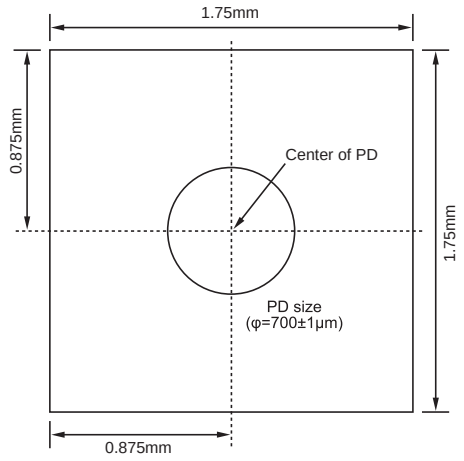


Pin Assignment



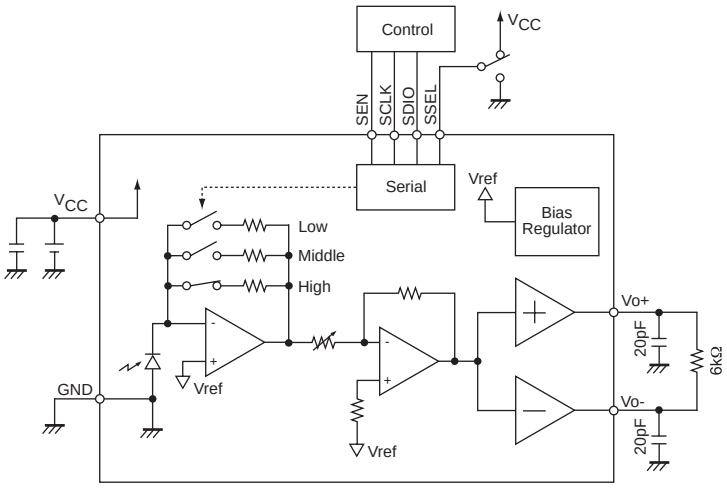
Pin No.	Pin name	Function
1A	SDIO	Serial communication Data pin
1B	VOP	Positive side output pin
1C	VON	Negative side output pin
2A	SCLK	Serial communication Clock pin
2C	SSEL	Register selection pin SSEL = Low, Open : Address 00 to 0Fh used SSEL = High : Address 10 to 1Fh used
3A	SEN	Serial communication Enable pin
3B	GND	GND pin
3C	V_{CC}	Power supply voltage pin

PD assignment



*PD size for reference to be used for design

Block diagram and Test circuit diagram



Resister table

Enable selection of the register group from the SSEL pin.

SSEL = Low, Open

	Address	7	6	5	4	3	2	1	0
Name	00h	**POWER**		**IV GAIN SEL**		**GAIN SEL**			
Default		00		00		00		x	x
Value		11: Power on 00 01 10: Sleep		00 01: High 10: Middle 11: Low		00 01: BD 10: DVD 11: CD			
Name	01h	**BD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	02h	**DVD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	03h	**CD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	0Eh	**TEST1 (*1)**							
Name	0Fh	**TEST2 (*1)**							

SSEL = High

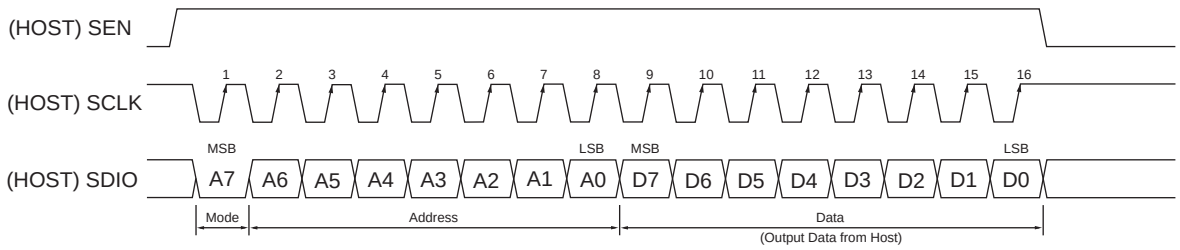
	Address	7	6	5	4	3	2	1	0
Name	10h	**POWER**		**IV GAIN SEL**		**GAIN SEL**			
Default		00		00		00		x	x
Value		11: Power on 00 01 10: Sleep		00 01: High 10: Middle 11: Low		00 01: BD 10: DVD 11: CD			
Name	11h	**BD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	12h	**DVD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	13h	**CD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	1Eh	**TEST1 (*1)**							
Name	1Fh	**TEST2 (*1)**							

*1 TEST1 and TEST2 are either the time when power is applied or “00000000” is set. Do not attempt to change “00000000” during operation.
“00000000” is returned when reading is made.

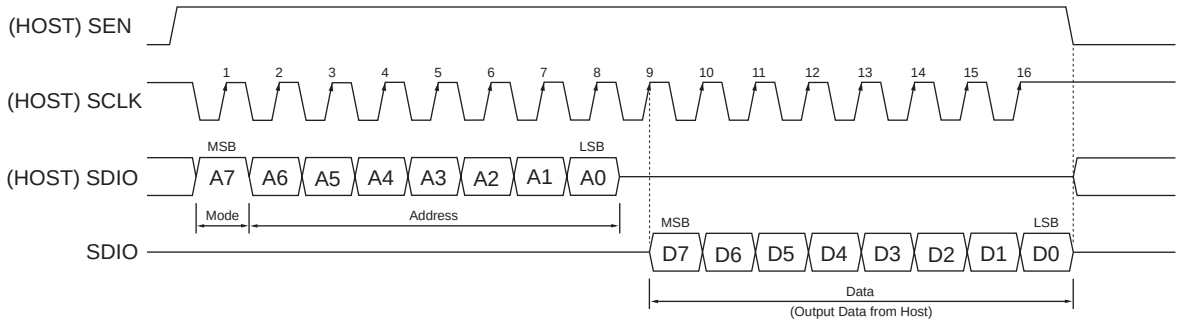
*2 No problem in terms of operation occurs even when writing is made to the address 04h to 0Dh and 14h to 1Dh.
“00000000” is returned when this address is read.

Serial protocol

WRITE timing chart



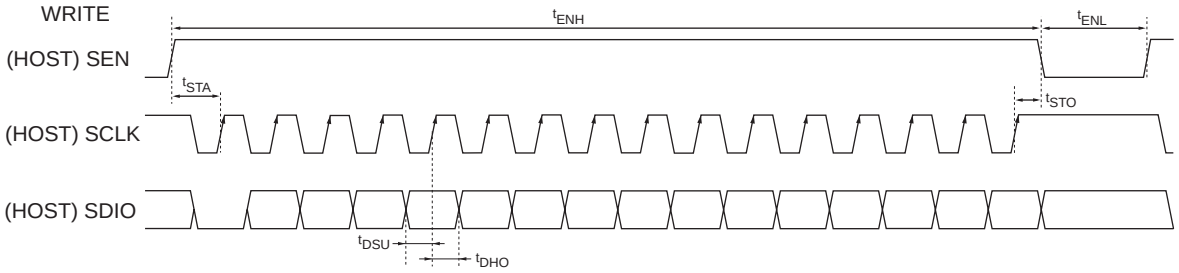
READ timing chart



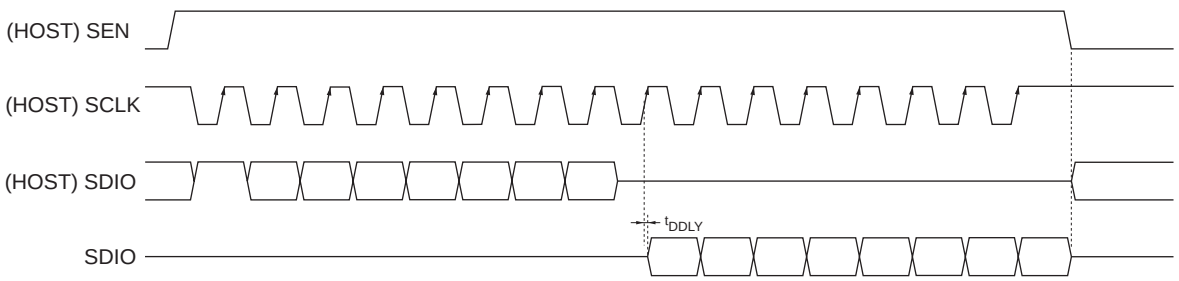
SDIO pin load / CL=20pF (The table below shows the design reference value.)

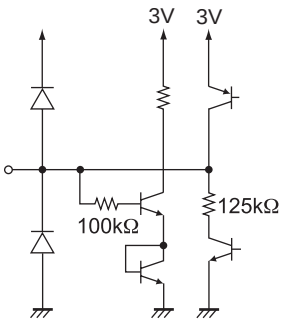
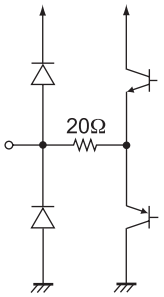
Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency Write	f_{SCL}	0		10	MHz
SCL clock frequency Read	f_{SCL}	0		4	MHz
SDIO data setup time	t_{DSU}	50			ns
SDIO data hold time	t_{DHO}	50			ns
SDIO output delay	t_{DDLY}		10	80	ns
SEN “H” period	t_{ENH}	1.6			μs
SEN “L” period	t_{ENL}	200			ns
SCL rise time after SEN rise	t_{STA}	60			ns
SEN fall time after final SCL rise	t_{STO}	100			ns
Serial input “H” voltage	V_IH	2.4			V
Serial input “L” voltage	V_IL			0.6	V
SDIO output “H” voltage	V_OH	2.5	2.9	3.3	V
SDIO output “L” voltage	V_OL	0	0.3	0.8	V

WRITE



READ



Pin	Type	Equivalent circuit diagram
SDIO	Input Output	
VOP VON	Output	
SCLK SSEL SEN	Input