Dual 12-Bit Rail-to-Rail Micropower DAC

FEATURES

- **SO-8 Package**
- 12-Bit Resolution
- **Buffered True Rail-to-Rail Voltage Output**
- External Reference Input Can Be Tied to V_{CC}
- Output Swings from 0V to V_{REF}
- 3V and 5V Supply Operation
- Schmitt Trigger on Clock Input Allows Direct Optocoupler Interface
- Power-On Reset Clears DACs to 0V
- 3-Wire Serial Interface
- **Maximum DNL Error: 0.5LSB**
- Low Cost

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

DESCRIPTION

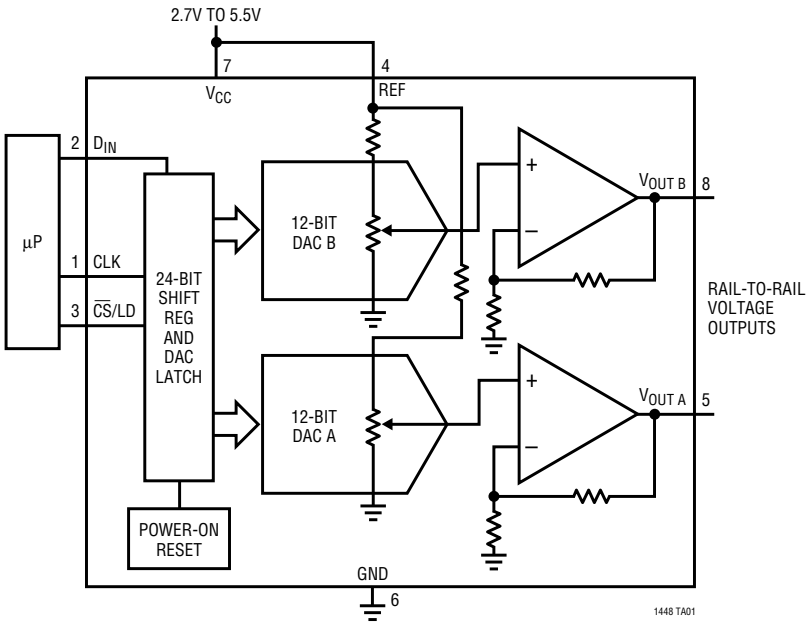
The LTC®1448 is a dual rail-to-rail voltage output, 12-bit digital-to-analog converter (DAC). It includes rail-to-rail output buffer amplifiers and an easy-to-use 3-wire serial interface. It is available in 8-pin SO and PDIP packages and provides the smallest footprint of any dual 12-bit DAC.

The LTC1448 has an external reference input pin (REF) and its outputs swing from 0V to REF. The REF input can be tied to V_{CC} providing rail-to-rail operation from supplies of 2.7V to 5.5V. (For devices with internal reference see the LTC1446 data sheet.) The LTC1448 dissipates 2.5mW from a 5V supply.

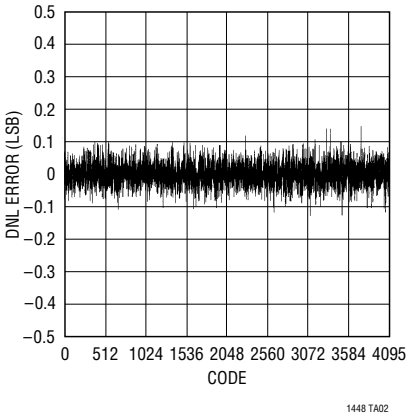
The low power supply current and the small SO-8 package make the LTC1448 ideal for battery-powered applications.

TYPICAL APPLICATION

Functional Block Diagram: 12-Bit Rail-to-Rail Dual DAC



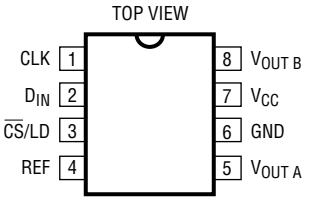
Differential Nonlinearity vs Input Code



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... –0.5V to 7.5V
Logic Inputs to GND ..... –0.5V to 7.5V
$V_{OUT\ A}$, $V_{OUT\ B}$, REF to GND ..... –0.5V to V_{CC} + 0.5V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
LTC1448C ..... 0°C to 70°C
LTC1448I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LTC1448CN8 LTC1448IN8 LTC1448CS8 LTC1448IS8
S8 PART MARKING
1448 1448I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V to 5.5V, $V_{OUT\ A}$ and $V_{OUT\ B}$ unloaded, REF ≤ V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	12			Bits
	Monotonicity		●	12			Bits
DNL	Differential Nonlinearity	$V_{REF} \le V_{CC}$ – 0.1V (Note 1)	●		±0.2	±0.5	LSB
INL	Integral Nonlinearity	$V_{REF} \le V_{CC}$ – 0.1V (Note 1), T_A = 25°C $V_{REF} \le V_{CC}$ – 0.1V (Note 1)	 ●			±5.0 ±5.5	LSB LSB
V_{OS}	Offset Error	Measured at Code 20, T_A = 25°C Measured at Code 20	 ●			±10 ±15	mV mV
$V_{OS}TC$	Offset Error Temperature Coefficient				±15		µV/°C
V_{FS}	Full-Scale Voltage	V_{REF} = 4.096V, T_A = 25°C V_{REF} = 4.096V	 ●	4.070 4.060	4.095 4.095	4.120 4.130	V V
$V_{FS}TC$	Full-Scale Voltage Temperature Coefficient				10		ppm/°C
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	(Note 4)	●		450	700	µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●		55	120	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●		65	120	mA
	Output Impedance to GND	Input Code = 0	●		30	120	Ω
	Output Line Regulation	Input Code = 4095. V_{CC} = 4.5V to 5.5V, V_{REF} = 4.096V	●		0.2	1.5	LSB/V

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V to 5.5V, $V_{OUT\ A}$ and $V_{OUT\ B}$ unloaded, REF ≤ V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Performance							
	Voltage Output Slew Rate		●	0.5	1.0		V/µs
	Voltage Output Settling Time	(Notes 2, 3) to ±0.5LSB			14		µs
	Digital Feedthrough				0.3		nV•s
Reference Input							
R_{IN}	REF Input Resistance		●	7.5	12.5	18	kΩ
REF	REF Input Range	(Notes 5, 6)	●	0		V_{CC}	V
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 5V V_{CC} = 3V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 5V V_{CC} = 3V	● ●			0.8 0.6	V V
I_{LEAK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 6)	●			10	pF
Switching (V_{CC} = 4.5V to 5.5V)							
t_1	D_{IN} Valid to CLK Setup		●	40			ns
t_2	D_{IN} Valid to CLK Hold		●	0			ns
t_3	CLK High Time	(Note 6)	●	40			ns
t_4	CLK Low Time	(Note 6)	●	40			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	50			ns
t_6	LSB CLK to $\overline{CS}$/LD	(Note 6)	●	40			ns
t_7	$\overline{CS}$/LD Low to CLK	(Note 6)	●	20			ns
t_8	CLK Low to $\overline{CS}$/LD Low	(Note 6)	●	20			ns
Switching (V_{CC} = 2.7V to 5.5V)							
t_1	D_{IN} Valid to CLK Setup		●	60			ns
t_2	D_{IN} Valid to CLK Hold		●	0			ns
t_3	CLK High Time	(Note 6)	●	60			ns
t_4	CLK Low Time	(Note 6)	●	60			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	80			ns
t_6	LSB CLK to $\overline{CS}$/LD	(Note 6)	●	60			ns
t_7	$\overline{CS}$/LD Low to CLK	(Note 6)	●	30			ns
t_8	CLK Low to $\overline{CS}$/LD Low	(Note 6)	●	30			ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Nonlinearity is defined from code 20 to code 4095 (full scale). See Applications Information.

Note 2: Load is 5k in parallel with 100pF.

Note 3: DAC switched between all 1s and the code corresponding to V_{OS} for the part.

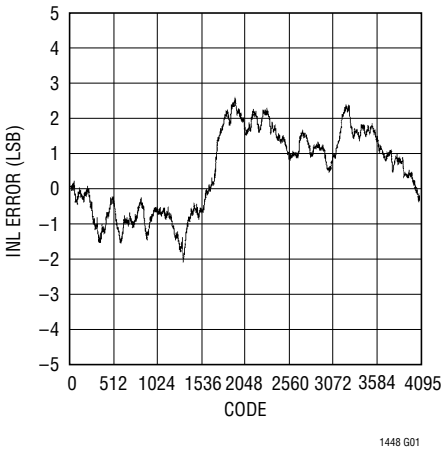
Note 4: Digital inputs at 0V or V_{CC}.

Note 5: V_{OUT} can only swing from (GND + $|V_{OS}|$) to (V_{CC} – $|V_{OS}|$) when output is unloaded.

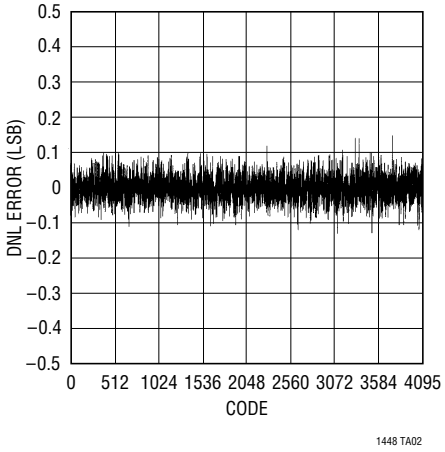
Note 6. Guaranteed by design, not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

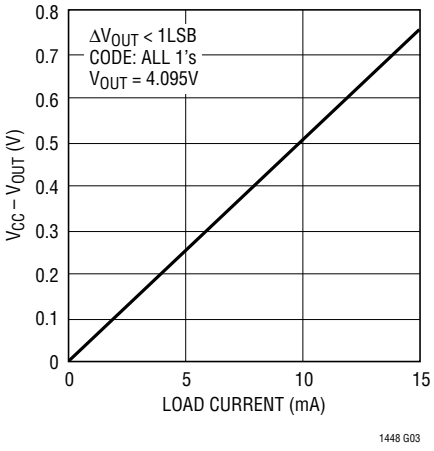
Integral Nonlinearity (INL)



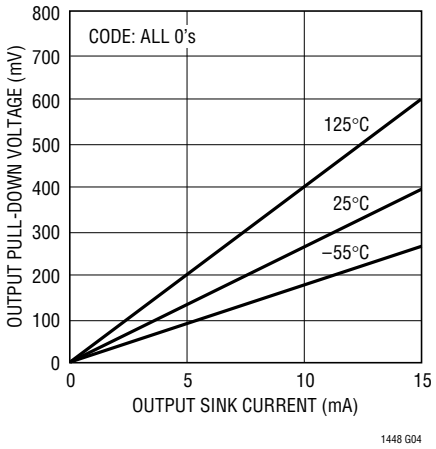
Differential Nonlinearity (DNL)



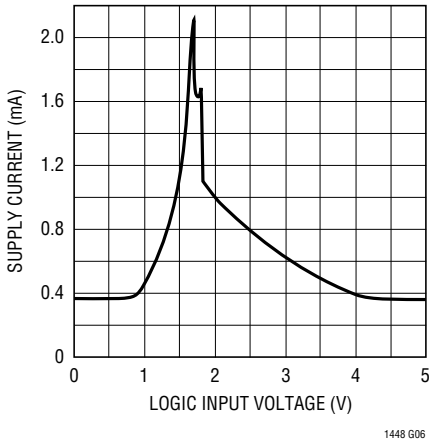
Minimum Supply Headroom for Full Output Swing vs Load Current



Minimum Output Voltage vs Output Sink Current



Supply Current vs Logic Input Voltage



PIN FUNCTIONS

CLK (Pin 1): Serial Interface Clock. Internal Schmitt trigger on this input allows direct optocoupler interface.

D_{IN} (Pin 2): Serial Interface Data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock.

$\overline{CS}$/LD (Pin 3): Serial Interface Enable and Load Control. When $\overline{CS}$/LD is low the CLK signal is enabled, so the data can be clocked in. When $\overline{CS}$/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output and the CLK is disabled internally.

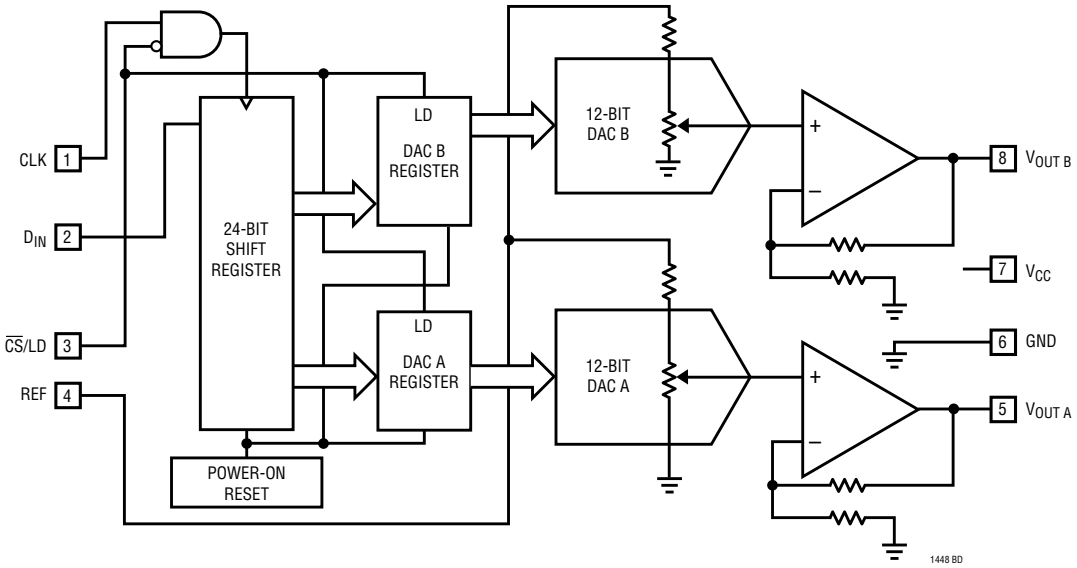
REF (Pin 4): Reference Input for Both DACs. This pin can be tied to V_{CC}. The output will swing from 0V to REF. The typical input resistance is 12.5k.

$V_{OUT\ A}$, $V_{OUT\ B}$ (Pins 5, 8): Buffered DAC Outputs.

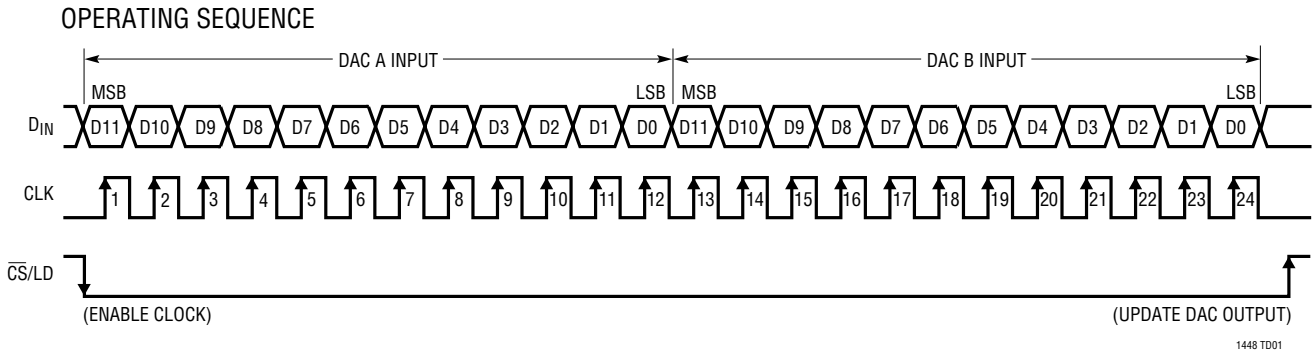
GND (Pin 6): Ground.

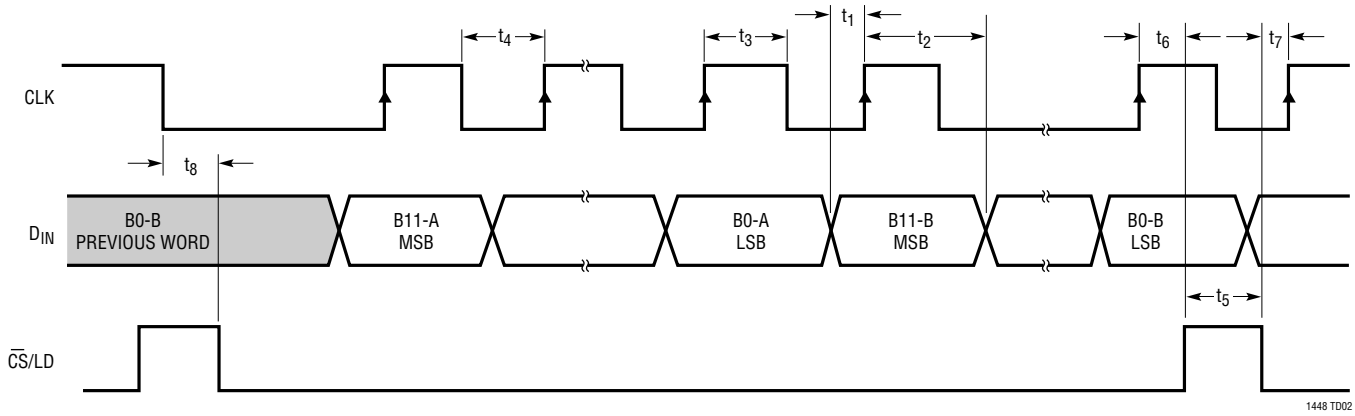
V_{CC} (Pin 7): Positive Supply Input. 2.7V ≤ V_{CC} ≤ 5.5V. Requires a bypass capacitor to ground.

BLOCK DIAGRAM



TIMING DIAGRAMS





DEFINITIONS

Differential Nonlinearity (DNL): The differerence between the measured change and the ideal 1LSB change for any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

where ΔV_{OUT} is the measured voltage difference between two adjacent codes.

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

Full-Scale Error (FSE): The deviation of the actual full-scale voltage from ideal. FSE includes the effects of offset and gain errors (see Applications Information).

Integral Nonlinearity (INL): The deviation from a straight line passing through the endpoints of the DAC transfer curve (Endpoint INL). Because the output cannot go below zero, the linearity is measured between full scale and the lowest code which guarantees the output will be greater than zero. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)]/LSB$$

where V_{OUT} is the output voltage of the DAC measured at the given input code.

Least Significant Bit (LSB): The ideal voltage difference between two successive codes.

$$LSB = V_{REF}/4096$$

Resolution (n): Defines the number of DAC output states (2^n) that divide the full-scale range. Resolution does not imply linearity.

Voltage Offset Error (V_{OS}): Nominally, the voltage at the output when the DAC is loaded with all zeros. A single supply DAC can have a true negative offset, but the output cannot go below zero (see Applications Information).

For this reason, single supply DAC offset is measured at the lowest code that guarantees the output will be greater than zero.

OPERATION

Serial Interface

The data on the DIN input is loaded into the shift register on the rising edge of the clock. Data is loaded as one 24-bit word where the first 12 bits are for DAC A and the second 12 are for DAC B. For each 12-bit segment the MSB is loaded first. Data from the shift register is loaded into the DAC register when $\overline{CS}$/LD is pulled high. The clock is disabled internally when $\overline{CS}$/LD is high. Note: CLK must be low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse.

Voltage Output

The LTC1448's rail-to-rail buffered outputs can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 30Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

The output swings from 0V to the voltage at the REF pin, i.e., there is a gain of 1 from the REF to V_{OUT}. Please note if REF is tied to V_{CC} the output can only swing to ($V_{CC} - V_{OS}$). See Applications Information.

APPLICATIONS INFORMATION

Rail-to-Rail Output Considerations

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 1b.

Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 1c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

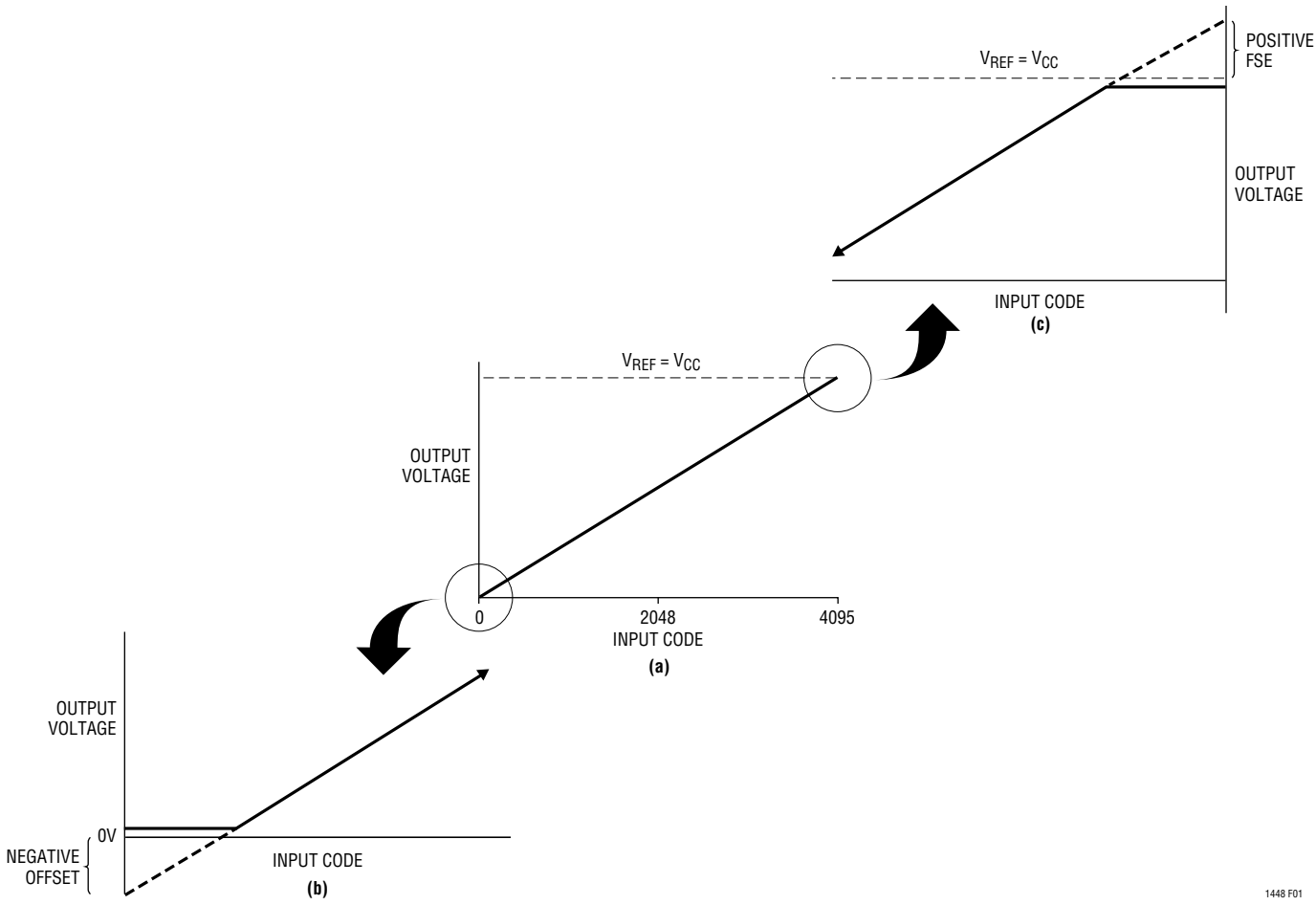
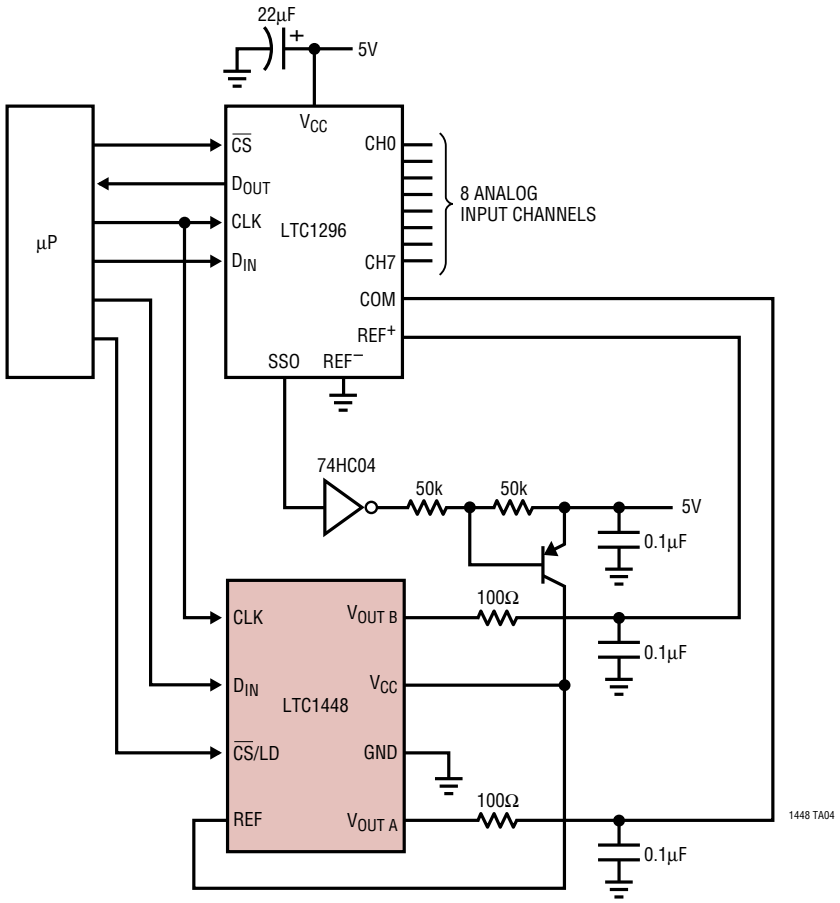


Figure 1. Effects of Rail-to-Rail Operation on a DAC Transfer Curve: (a) Overall Transfer Function, (b) Effect of Negative Offset for Codes Near Zero Scale, (c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When $V_{REF} = V_{CC}$

TYPICAL APPLICATIONS

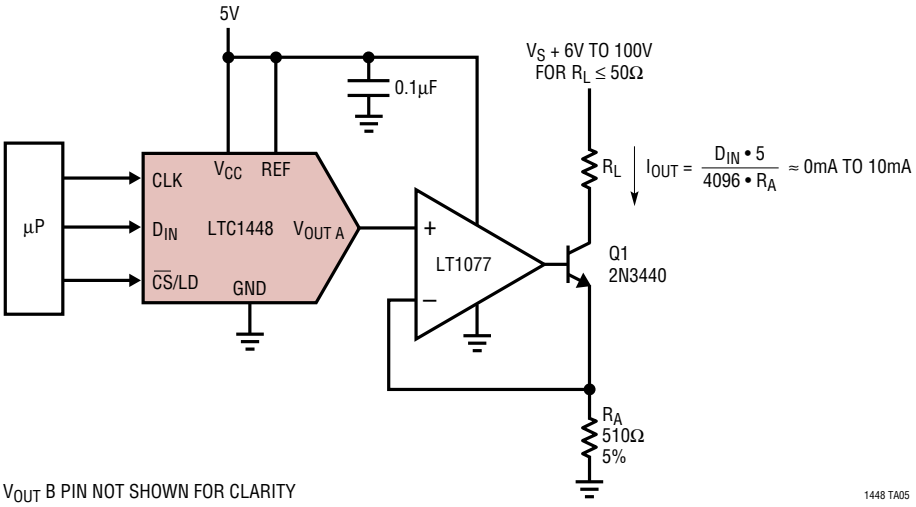
This circuit shows how to use one LTC1448 to make an autoranging ADC. The microprocessor sets the reference span and the Common pin for the analog input by loading the appropriate digital code into the LTC1448. $V_{OUT\ A}$ controls the Common pin for the analog inputs to the LTC1296 and $V_{OUT\ B}$ controls the reference span by setting the REF^+ pin on the LTC1296. The LTC1296 has a Shutdown pin that goes low in shutdown mode. This will turn off the PNP transistor supplying power to the LTC1448. The resistor and capacitor on the LTC1448 outputs act as a lowpass filter for noise.

An Autoranging 8-Channel ADC with Shutdown



TYPICAL APPLICATIONS

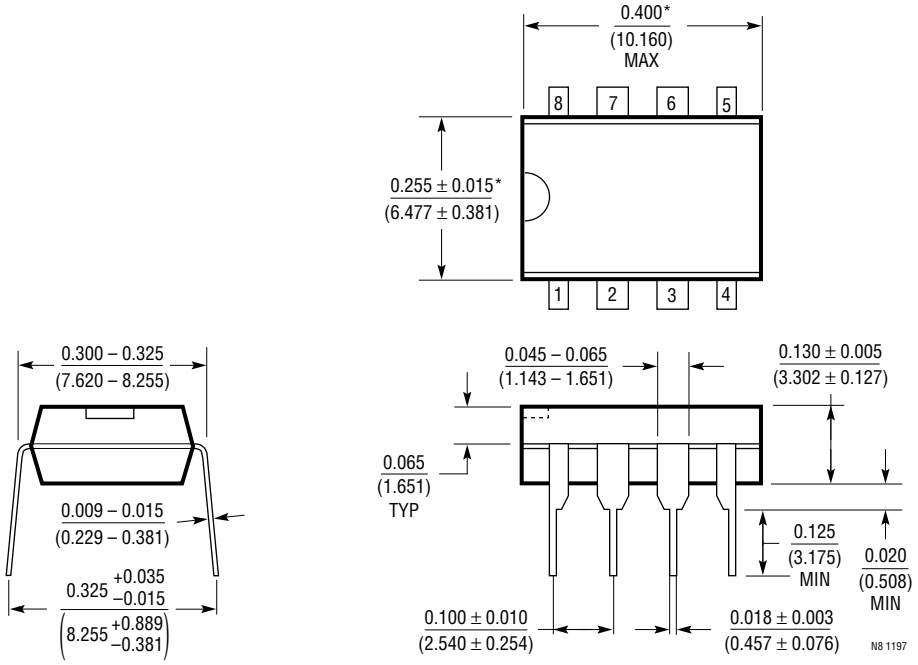
Digitally Programmable Current Source



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

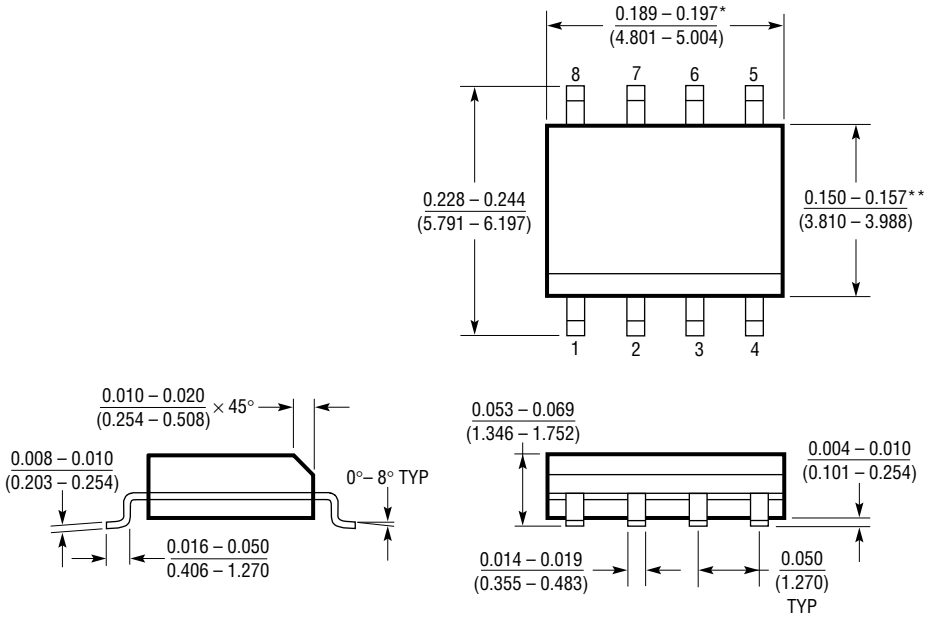


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



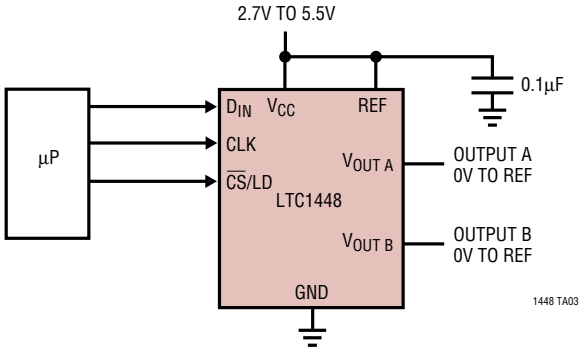
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 0996

TYPICAL APPLICATION

12-Bit, 3V to 5V Supply, Dual Voltage Output DAC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Single 12-Bit V_{OUT} DAC, Full Scale: 2.048V, V_{CC}: 4.75V to 15.75V, Reference Can Be Overdriven Up to 12V, i.e., FS_{MAX} = 12V	5V to 15V Single Supply, Complete V_{OUT} DAC in SO-8 Package
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package with Internal Reference	LTC1446: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1450/LTC1450L	Single 12-Bit V_{OUT} DACs with Parallel Interface	LTC1450: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1450L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1451	Single Rail-to-Rail 12-Bit DAC, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V, Internal 2.048V Reference Brought Out to Pin	5V Low Power, Complete V_{OUT} DAC in SO-8 Package
LTC1452	Single Rail-to-Rail 12-Bit V_{OUT} Multiplying DAC, V_{CC}: 2.7V to 5.5V	Low Power, Multiplying V_{OUT} DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package
LTC1453	Single Rail-to-Rail 12-Bit V_{OUT} DAC, Full Scale: 2.5V, V_{CC}: 2.7V to 5.5V	3V, Low Power, Complete V_{OUT} DAC in SO-8 Package
LTC1454/LTC1454L	Dual 12-Bit V_{OUT} DACs in SO-16 Package with Added Functionality	LTC1454: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1454L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1456	Single Rail-to-Rail Output 12-Bit DAC with Clear Pin, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V	Low Power, Complete V_{OUT} DAC in SO-8 Package with Clear Pin
LTC1458/LTC1458L	Quad 12 Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1659	Single Rail-to-Rail 12-Bit V_{OUT} DAC in MSOP-8 Package, V_{CC}: 2.7V to 5.5V	Low Power Multiplying V_{OUT} DAC in MSOP-8 Package. Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417• (408)432-1900
FAX: (408) 434-0507• TELEX: 499-3977• www.linear-tech.com
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