Quad 3mA, 100MHz, 750V/μs Operational Amplifier

March 2001

FEATURES

- **100MHz Gain Bandwidth**
- **750V/μs Slew Rate**
- **3.6mA Maximum Supply Current per Amplifier**
- 8nV/√Hz Input Noise Voltage
- Unity-Gain Stable with C_{LOAD} Up to 1000pF
- 1.5mV Maximum Input Offset Voltage
- 4μA Maximum Input Bias Current
- 400nA Maximum Input Offset Current
- 40mA Minimum Output Current, $V_{OUT} = \pm 3V$
- ±3.5V Minimum Input CMR, $V_S = \pm 5V$
- 30ns Settling Time to 0.1%, 5V Step
- Specified at ±5V, Single 5V Supplies
- Operating Temperature Range: –40°C to 85°C

APPLICATIONS

- Active Filters
- Wideband Amplifiers
- Buffers
- Video Amplification
- Communication Receivers
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

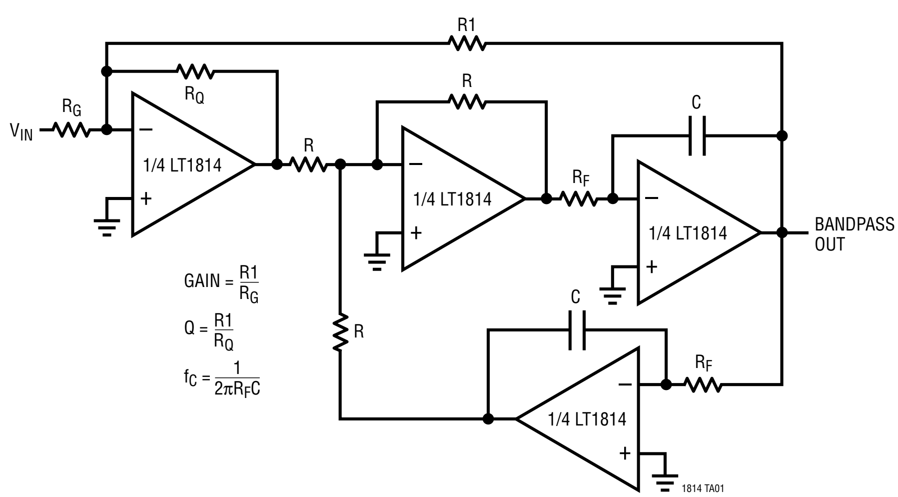
The LT®1814 is a quad, low power, high speed, very high slew rate operational amplifier with excellent DC performance. The LT1814 features reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than other devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier.

The output drives a 100Ω load to ±3.5V with ±5V supplies. On a single 5V supply, the output swings from 1.1V to 3.9V with a 100Ω load connected to 2.5V. The amplifiers are stable with a 1000pF capacitive load making them useful in buffer and cable driver applications.

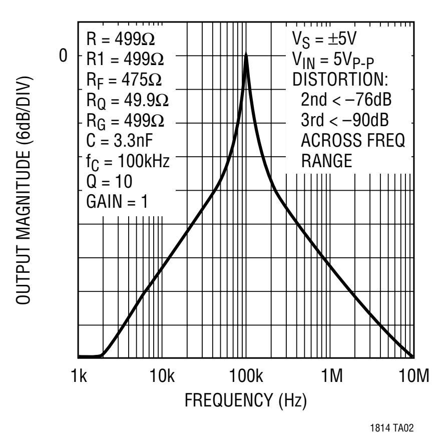
The LT1814 is manufactured on Linear Technology's advanced low voltage complementary bipolar process. The single and dual versions are the LT1812 and LT1813.

TYPICAL APPLICATION

Bandpass Filter with Independently Settable Gain, Q and f_C



Filter Frequency Response

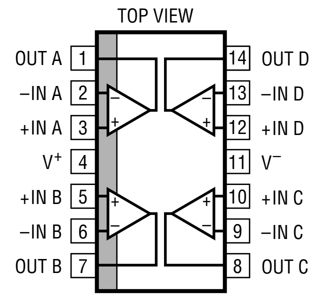


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Differential Input Voltage (Transient Only, Note 2) .. ±3V
Input Voltage ....$\pm V_S$
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range .... –40°C to 85°C
Specified Temperature Range (Note 8) .. –40°C to 85°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART MARKING
LT1814CS LT1814IS

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, V_{CM} = 0V, unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			0.5	1.5	mV
		T_A = 0°C to 70°C	●			2	mV
		T_A = –40°C to 85°C	●			3	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift	T_A = 0°C to 70°C (Note 7)	●		10	15	µV/°C
		T_A = –40°C to 85°C (Note 7)	●		10	30	µV/°C
I_{OS}	Input Offset Current				50	400	nA
		T_A = 0°C to 70°C	●			500	nA
		T_A = –40°C to 85°C	●			600	nA
I_B	Input Bias Current				–0.9	±4	µA
		T_A = 0°C to 70°C	●			±5	µA
		T_A = –40°C to 85°C	●			±6	µA
e_n	Input Noise Voltage Density	f = 10kHz			8		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz			1		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	$V_{CM} = V^- + 1.5V$ to $V^+ - 1.5V$		3	10		MΩ
		Differential			1.5		MΩ
C_{IN}	Input Capacitance				2		pF
V_{CM}	Input Voltage Range	Guaranteed by CMRR		±3.5	±4.2		V
		T_A = –40°C to 85°C	●	±3.5			V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V		75	85		dB
		T_A = 0°C to 70°C	●	73			dB
		T_A = –40°C to 85°C	●	72			dB
	Minimum Supply Voltage	Guaranteed by PSRR			±1.25	±2	V
		T_A = –40°C to 85°C	●			±2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, V_{CM} = 0V, unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±5.5V		78	97		dB
		T_A = 0°C to 70°C	●	76			dB
		T_A = –40°C to 85°C	●	75			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±3V, R_L = 500Ω		1.5	3		V/mV
		T_A = 0°C to 70°C	●	1.0			V/mV
		T_A = –40°C to 85°C	●	0.8			V/mV
		V_{OUT} = ±3V, R_L = 100Ω		1.0	2.5		V/mV
		T_A = 0°C to 70°C	●	0.7			V/mV
		T_A = –40°C to 85°C	●	0.6			V/mV
V_{OUT}	Maximum Output Swing (Positive/Negative)	R_L = 500Ω, 30mV Overdrive		±3.8	±4		V
		T_A = 0°C to 70°C	●	±3.7			V
		T_A = –40°C to 85°C	●	±3.6			V
		R_L = 100Ω, 30mV Overdrive		±3.35	±3.5		V
		T_A = 0°C to 70°C	●	±3.25			V
		T_A = –40°C to 85°C	●	±3.15			V
I_{OUT}	Maximum Output Current	V_{OUT} = ±3V, 30mV Overdrive		±40	±60		mA
		T_A = 0°C to 70°C	●	±35			mA
		T_A = –40°C to 85°C	●	±30			mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, 1V Overdrive (Note 3)		±75	±100		mA
		T_A = 0°C to 70°C	●	±60			mA
		T_A = –40°C to 85°C	●	±55			mA
SR	Slew Rate	A_V = –1 (Note 5)		500	750		V/µs
		T_A = 0°C to 70°C	●	400			V/µs
		T_A = –40°C to 85°C	●	350			V/µs
FPBW	Full Power Bandwidth	3V Peak (Note 6)			40		MHz
GBW	Gain Bandwidth Product	f = 200kHz, R_L = 500Ω		75	100		MHz
		T_A = 0°C to 70°C	●	65			MHz
		T_A = –40°C to 85°C	●	60			MHz
–3dB BW	–3dB Bandwidth	A_V = 1, R_L = 500Ω			200		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, 0.1V, R_L = 100Ω			2		ns
t_{PD}	Propagation Delay	A_V = 1, 50% to 50%, 0.1V, R_L = 100Ω			2.8		ns
OS	Overshoot	A_V = 1, 0.1V, R_L = 100Ω			25		%
t_S	Settling Time	A_V = –1, 0.1%, 5V			30		ns
THD	Total Harmonic Distortion	A_V = 2, f = 1MHz, V_{OUT} = $2V_{P-P}$, R_L = 500Ω			–76		dB
dG	Differential Gain	A_V = 2, V_{OUT} = $2V_{P-P}$, R_L = 150Ω			0.12		%
dP	Differential Phase	A_V = 2, V_{OUT} = $2V_{P-P}$, R_L = 150Ω			0.07		DEG
R_{OUT}	Output Resistance	A_V = 1, f = 1MHz			0.4		Ω
	Channel Separation	V_{OUT} = ±3V, R_L = 100Ω		82			dB
		T_A = 0°C to 70°C	●	81			dB
		T_A = –40°C to 85°C	●	80			dB
I_S	Supply Current	Per Amplifier			3	3.6	mA
		T_A = 0°C to 70°C	●			4.5	mA
		T_A = –40°C to 85°C	●			5.0	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, V_{CM} = 2.5V, R_L to 2.5V, unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			0.7	2.0	mV
		T_A = 0°C to 70°C	●			2.5	mV
		T_A = –40°C to 85°C	●			3.5	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift	T_A = 0°C to 70°C (Note 7)	●		10	15	µV/°C
		T_A = –40°C to 85°C (Note 7)	●		10	30	µV/°C
I_{OS}	Input Offset Current				50	400	nA
		T_A = 0°C to 70°C	●			500	nA
		T_A = –40°C to 85°C	●			600	nA
I_B	Input Bias Current				–1	±4	µA
		T_A = 0°C to 70°C	●			±5	µA
		T_A = –40°C to 85°C	●			±6	µA
e_n	Input Noise Voltage Density	f = 10kHz			8		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz			1		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	$V_{CM} = V^- + 1.5V$ to $V^+ - 1.5V$		3	10		MΩ
		Differential			1.5		MΩ
C_{IN}	Input Capacitance				2		pF
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR		3.5	4.2		V
		T_A = –40°C to 85°C	●	3.5			V
	Input Voltage Range (Negative)	Guaranteed by CMRR			0.8	1.5	V
		T_A = –40°C to 85°C	●			1.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.5V to 3.5V		73	82		dB
		T_A = 0°C to 70°C	●	71			dB
		T_A = –40°C to 85°C	●	70			dB
	Minimum Supply Voltage	Guaranteed by PSRR			±1.25	±2	V
		T_A = –40°C to 85°C	●			±2	V
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω		1.0	2		V/mV
		T_A = 0°C to 70°C	●	0.7			V/mV
		T_A = –40°C to 85°C	●	0.6			V/mV
		V_{OUT} = 1.5V to 3.5V, R_L = 100Ω		0.7	1.5		V/mV
		T_A = 0°C to 70°C	●	0.5			V/mV
		T_A = –40°C to 85°C	●	0.4			V/mV
V_{OUT}	Maximum Output Swing (Positive)	R_L = 500Ω, 30mV Overdrive		3.9	4.1		V
		T_A = 0°C to 70°C	●	3.8			V
		T_A = –40°C to 85°C	●	3.7			V
		R_L = 100Ω, 30mV Overdrive		3.7	3.9		V
		T_A = 0°C to 70°C	●	3.6			V
		T_A = –40°C to 85°C	●	3.5			V
	Maximum Output Swing (Negative)	R_L = 500Ω, 30mV Overdrive			0.9	1.1	V
		T_A = 0°C to 70°C	●			1.2	V
		T_A = –40°C to 85°C	●			1.3	V
		R_L = 100Ω, 30mV Overdrive			1.1	1.3	V
		T_A = 0°C to 70°C	●			1.4	V
		T_A = –40°C to 85°C	●			1.5	V
I_{OUT}	Maximum Output Current	V_{OUT} = 1.5V or 3.5V, 30mV Overdrive		±25	±35		mA
		T_A = 0°C to 70°C	●	±20			mA
		T_A = –40°C to 85°C	●	±17			mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 2.5V, 1V Overdrive (Note 3)		±55	±75		mA
		T_A = 0°C to 70°C	●	±45			mA
		T_A = –40°C to 85°C	●	±40			mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, V_{CM} = 2.5V, R_L to 2.5V, unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SR	Slew Rate	A_V = –1 (Note 5)		200	350		V/µs
		T_A = 0°C to 70°C	●	150			V/µs
		T_A = –40°C to 85°C	●	125			V/µs
FPBW	Full Power Bandwidth	1V Peak (Note 6)			55		MHz
GBW	Gain Bandwidth Product	f = 200kHz, R_L = 500Ω		65	94		MHz
		T_A = 0°C to 70°C	●	55			MHz
		T_A = –40°C to 85°C	●	50			MHz
–3dB BW	–3dB Bandwidth	A_V = 1, R_L = 500Ω			180		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, 0.1V, R_L = 100Ω			2.1		ns
t_{PD}	Propagation Delay	A_V = 1, 50% to 50%, 0.1V, R_L = 100Ω			3		ns
OS	Overshoot	A_V = 1, 0.1V, R_L = 100Ω			25		%
t_S	Settling Time	A_V = –1, 0.1%, 2V			30		ns
THD	Total Harmonic Distortion	A_V = 2, f = 1MHz, V_{OUT} = $2V_{P-P}$, R_L = 500Ω			–75		dB
dG	Differential Gain	A_V = 2, V_{OUT} = $2V_{P-P}$, R_L = 150Ω			0.22		%
dP	Differential Phase	A_V = 2, V_{OUT} = $2V_{P-P}$, R_L = 150Ω			0.21		DEG
R_{OUT}	Output Resistance	A_V = 1, f = 1MHz			0.45		Ω
	Channel Separation	V_{OUT} = 1.5V to 3.5V, R_L = 100Ω		81			dB
		T_A = 0°C to 70°C	●	80			dB
		T_A = –40°C to 85°C	●	79			dB
I_S	Supply Current	Per Amplifier			2.9	4.0	mA
		T_A = 0°C to 70°C	●			5.0	mA
		T_A = –40°C to 85°C	●			5.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Differential inputs of ±3V are appropriate for transient operation only, such as during slewing. Large sustained differential inputs can cause excessive power dissipation and may damage the part.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 5: Slew rate is measured between ±2V at the output with ±3V input for ±5V supplies and $2V_{P-P}$ at the output with a $3V_{P-P}$ input for single 5V supplies.

Note 6: Full power bandwidth is calculated from the slew rate:

FPBW = $SR/2\pi V_P$

Note 7: This parameter is not 100% tested

Note 8: The LT1814C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet the extended temperature limits, but is not tested at –40°C and 85°C. The LT1814I is guaranteed to meet the extended temperature limits.

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1814 amplifier is more tolerant of less than ideal board layouts than other high speed amplifiers. For optimum performance, a ground plane is recommended and trace lengths should be minimized, especially on the negative input lead.

Low ESL/ESR bypass capacitors should be placed directly at the positive and negative supply pins (0.01µF ceramics are recommended). For high drive current applications, additional 1µF to 10µF tantalums should be added.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole that can cause peaking or even oscillations. If feedback resistors greater than 1k are used, a parallel capacitor of value:

$$C_F > R_G \bullet C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is 1 and a large feedback resistor is used, C_F should be greater than or equal to C_{IN}. An example would be an I-to-V converter.

Input Considerations

The inputs of the LT1814 amplifiers are connected to the base of an NPN and PNP bipolar transistor in parallel. The base currents are of opposite polarity and provide first order bias current cancellation. Due to variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current, however, does not depend on beta matching and is tightly controlled. Therefore, the use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. For example, with a 100Ω source resistance at each input, the 400nA maximum offset current results in only 40µV of extra offset, while without balance the 4µA maximum input bias current could result in a 0.4mV offset contribution.

The inputs can withstand differential input voltages of up to 6V without damage and without needing clamping or series resistance for protection. This differential input voltage generates a large internal current (up to 40mA), which results in the high slew rate. In normal transient closed-loop operation, this does not increase power dissipation significantly because of the low duty cycle of the transient inputs. Sustained differential inputs, however, will result in excessive power dissipation and therefore **this device should not be used as a comparator.**

Capacitive Loading

The LT1814 is stable with capacitive loads from 0pF to 1000pF, which is outstanding for a 100MHz amplifier. The internal compensation circuitry accomplishes this by sensing the load induced output pole and adding compensation at the amplifier gain node as needed. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and ringing in the transient response. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (e.g., 75Ω) should be placed in series with the output. The receiving end of the cable should be terminated with the same value resistance to ground.

Slew Rate

The slew rate of the LT1814 is proportional to the differential input voltage. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 5V output step in a gain of 10 has a 0.5V input step, whereas in unity gain there is a 5V input step. The LT1814 is tested for a slew rate in a gain of –1. Lower slew rates occur in higher gain configurations.

Power Dissipation

The LT1814 combines four amplifiers with high speed and large output drive in a small package. It is possible to exceed the maximum junction temperature specification under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

Power dissipation is composed of two parts. The first is due to the quiescent supply current and the second is due to on-chip dissipation caused by the load current. The

APPLICATIONS INFORMATION

worst-case load induced power occurs when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 the supply voltage). Therefore P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-) \bullet (I_{SMAX}) + (V^+/2)^2/R_L \text{ or}$$

$$P_{DMAX} = (V^+ - V^-) \bullet (I_{SMAX}) + (V^+ - V_{OMAX}) \bullet (V_{OMAX}/R_L)$$

Example: LT1814S at 70°C, $V_S = \pm5V$, $R_L = 100\Omega$

$$P_{DMAX} = (10V) \bullet (4.5mA) + (2.5V)^2/100\Omega = 108mW$$

$$T_{JMAX} = 70°C + (4 \bullet 108mW) \bullet (100°C/W) = 113°C$$

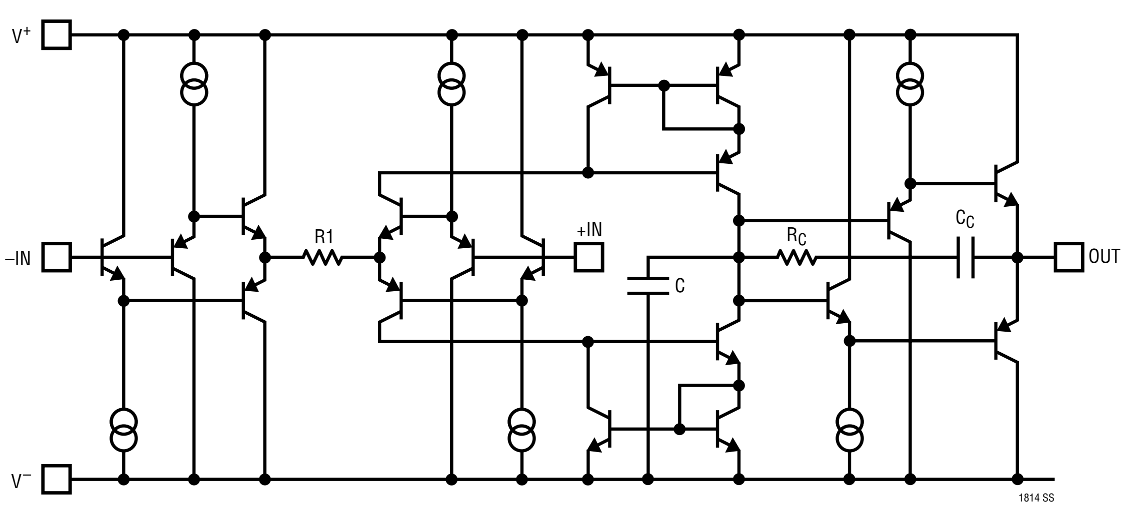
Circuit Operation

The LT1814 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the Simplified Schematic. Complementary NPN and PNP emitter followers buffer the inputs and drive an internal resistor. The input voltage appears across the resistor, generating current that is mirrored into the high impedance node.

Complementary followers form an output stage that buffers the gain node from the load. The input resistor, input stage transconductance, and the capacitor on the high impedance node determine the bandwidth. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input step. Highest slew rates are therefore seen in the lowest gain configurations.

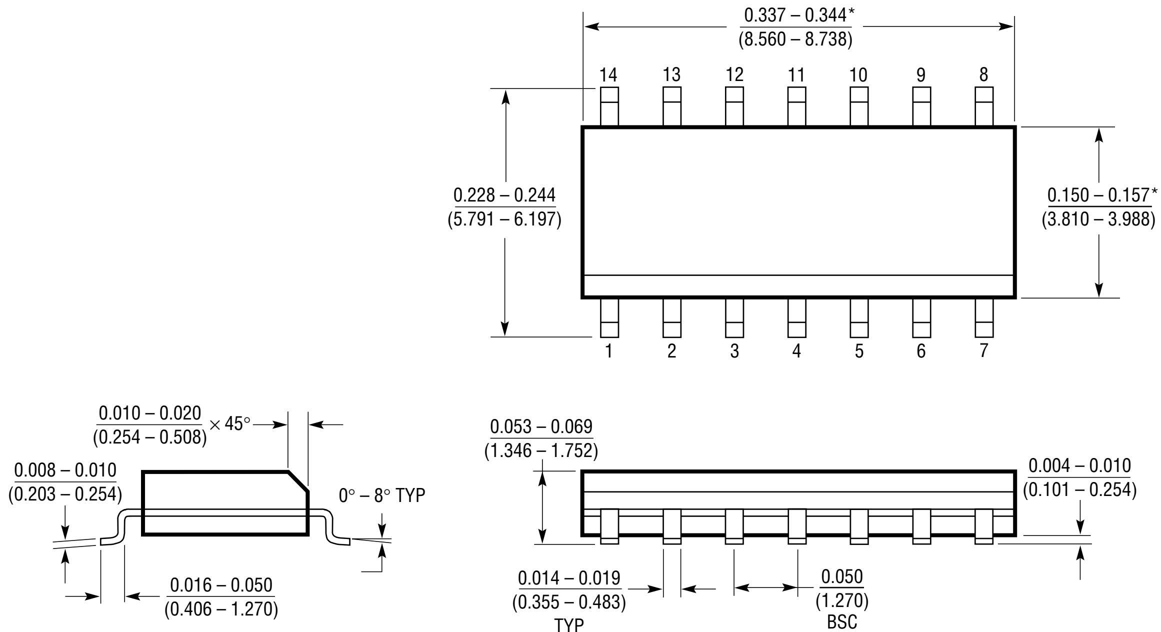
The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When a heavy load (capacitive or resistive) is driven, the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance moves the unity-gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that the total phase lag does not exceed 180° (zero phase margin), and the amplifier remains stable. In this way, the LT1814 is stable with up to 1000pF capacitive loads in unity gain, and even higher capacitive loads in higher closed-loop gain configurations.

SIMPLIFIED SCHEMATIC (one amplifier)



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S Package
14-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1363/LT1364/LT1365	Single/Dual/Quad 70MHz, 1000V/µs, C-Load™ Op Amps	±2.5V to ±15V
LT1395/LT1396/LT1397	Single/Dual/Quad 400MHz Current Feedback Amplifiers	4.6mA Supply Current, 800V/µs, 80mA Output Current
LT1806/LT1807	Single/Dual 325MHz, 140V/µs Rail-to-Rail I/O Op Amps	Low Noise 3.5nV/√Hz
LT1809/LT1810	Single/Dual 180MHz, 350V/µs Rail-to-Rail I/O Op Amps	Low Distortion –90dBc at 5MHz
LT1812/LT1813	Single/Dual 3mA, 100MHz, 750V/µs Op Amps	Single/Dual Version of LT1814
LT1815	Single 220MHz, 1500V/µs Op Amp	6.5mA Supply Current, 6nV/√Hz Input Noise

C-Load is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
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