

## Dual, Matched Picoampere, Microvolt Input, Low Noise Op Amp

### FEATURES

- *Guaranteed* Offset Voltage 50 $\mu$ V Max.
- *Guaranteed* Bias Current 120pA Max.  
     25°C 700pA Max.  
     –55°C to 125°C 1.5 $\mu$ V/°C Max.
- *Guaranteed* Drift 0.5 $\mu$ Vp-p
- Low Noise, 0.1Hz to 10Hz 600 $\mu$ A Max.
- *Guaranteed* Supply Current 112dB Min.
- *Guaranteed* CMRR 112dB Min.
- *Guaranteed* PSRR
- *Guaranteed* Voltage Gain with 5mA Load Current
- *Guaranteed* Matching Characteristics

### APPLICATIONS

- Strain Gauge Signal Conditioner
- Dual Limit Precision Threshold Detection
- Charge Integrators
- Wide Dynamic Range Logarithmic Amplifiers
- Light Meters
- Low Frequency Active Filters
- Standard Cell Buffers
- Thermocouple Amplifiers

### DESCRIPTION

The LT1024 dual, matched internally compensated universal precision operational amplifier can be used in practically all precision applications requiring multiple op amps. The LT1024 combines picoampere bias currents (which are maintained over the full –55°C to 125°C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, practically immeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of a million round out the LT1024's superb precision specifications.

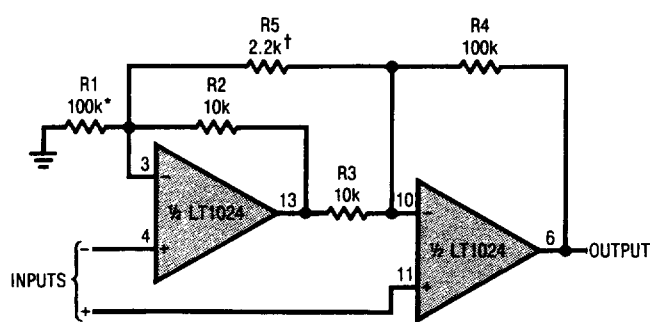
Tight matching is guaranteed on offset voltage, non-inverting bias currents and common-mode and power supply rejections.

The all-around excellence of the LT1024 eliminates the necessity of the time-consuming error analysis procedure of precision system design in many dual applications; the LT1024 can be stocked as the universal dual op amp in the 14-pin DIP configuration.

For a single op amp with similar specifications, see the LT1012 data sheet; for a single supply dual precision op amp in the 8-pin configuration, see the LT1013 data sheet.

**2**

Two Op Amp Instrumentation Amplifier

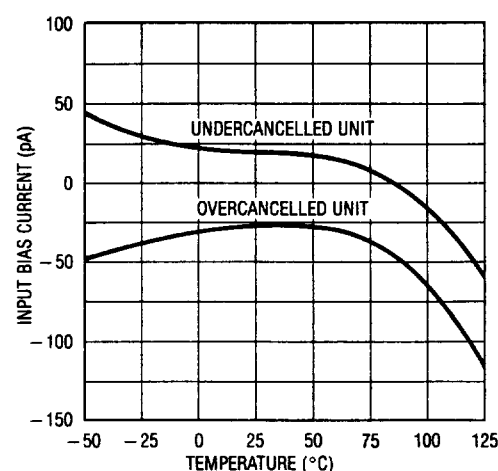


$$\text{GAIN} = \frac{R_4}{R_3} \left[ 1 + \frac{1}{2} \left( \frac{R_2}{R_1} + \frac{R_3}{R_4} \right) + \frac{R_2 + R_3}{R_5} \right] \approx 100$$

\*TRIM FOR COMMON-MODE REJECTION  
 †TRIM FOR GAIN

TYPICAL PERFORMANCE:  
 OFFSET VOLTAGE = 20 $\mu$ V  
 BIAS CURRENT =  $\pm$  30pA  
 OFFSET CURRENT = 30pA

Input Bias Current vs  
Temperature



# LT1024

## ABSOLUTE MAXIMUM RATINGS

|                                       |                |
|---------------------------------------|----------------|
| Supply Voltage                        | ± 20V          |
| Differential Input Current (Note 1)   | ± 10mA         |
| Input Voltage                         | ± 20V          |
| Output Short Circuit Duration         | Indefinite     |
| Operating Temperature Range           |                |
| LT1024AM/LT1024M                      | −55°C to 125°C |
| LT1024AC/LT1024C                      | 0°C to 70°C    |
| Storage Temperature Range             |                |
| All Devices                           | −65°C to 150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C          |

## PACKAGE/ORDER INFORMATION

D PACKAGE  
14 PIN HERMETIC  
(SIDEBRAZED)

N PACKAGE  
14 PIN PLASTIC

NOTE: DEVICE MAY BE OPERATED EVEN IF INSERTION IS REVERSED; THIS IS DUE TO INHERENT SYMMETRY OF PIN LOCATIONS OF AMPLIFIERS A AND B (NOTE 2).

ORDER PART NUMBER

LT1024AMD  
LT1024MD  
LT1024ACN  
LT1024CN

## ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$ , $V_{CM} = 0V$ , $T_A = 25^\circ C$ unless otherwise noted

### Individual Amplifiers

| SYMBOL    | PARAMETER                                | CONDITIONS                                 | LT1024AM/LT1024AC |        |       | LT1024M/LT1024C |        |       | UNITS          |
|-----------|--|--|-------------------|--------|-------|-----------------|--------|-------|----------------|
|           |  |  | MIN               | TYP    | MAX   | MIN             | TYP    | MAX   |                |
| $V_{OS}$  | Input Offset Voltage                     |  |                   | 15     | 50    |                 | 20     | 100   | $\mu V$        |
|           | Long Term Input Offset Voltage Stability |  |                   | 0.3    |       |                 | 0.3    |       | $\mu V/month$  |
| $I_{OS}$  | Input Offset Current                     |  |                   | 20     | 100   |                 | 25     | 180   | pA             |
| $I_B$     | Input Bias Current                       |  |                   | ± 25   | ± 120 |                 | ± 30   | ± 200 | pA             |
| $e_n$     | Input Noise Voltage                      | 0.1Hz to 10Hz                              |                   | 0.5    |       |                 | 0.5    |       | $\mu Vp-p$     |
| $e_n$     | Input Noise Voltage Density              | $f_0 = 10Hz$ (Note 3)                      |                   | 17     | 33    |                 | 17     | 33    | $nV/\sqrt{Hz}$ |
|           |  | $f_0 = 1000Hz$ (Note 3)                    |                   | 14     | 24    |                 | 14     | 24    | $nV/\sqrt{Hz}$ |
| $i_n$     | Input Noise Current Density              | $f_0 = 10Hz$                               |                   | 20     |       |                 | 20     |       | $fA/\sqrt{Hz}$ |
| $A_{VOL}$ | Large Signal Voltage Gain                | $V_{OUT} = \pm 12V$ , $R_L \geq 10k\Omega$ | 250               | 2000   |       | 180             | 2000   |       | V/mV           |
|           |  | $V_{OUT} = \pm 10V$ , $R_L \geq 2k\Omega$  | 150               | 1000   |       | 100             | 1000   |       | V/mV           |
| CMRR      | Common-Mode Rejection Ratio              | $V_{CM} = \pm 13.5V$                       | 112               | 132    |       | 108             | 132    |       | dB             |
| PSRR      | Power Supply Rejection Ratio             | $V_S = \pm 2V$ to $\pm 20V$                | 112               | 132    |       | 108             | 132    |       | dB             |
|           | Input Voltage Range                      |  | ± 13.5            | ± 14.0 |       | ± 13.5          | ± 14.0 |       | V              |
| $V_{OUT}$ | Output Voltage Swing                     | $R_L = 10k\Omega$                          | ± 13              | ± 14   |       | ± 13            | ± 14   |       | V              |
|           | Slew Rate                                |  | 0.1               | 0.2    |       | 0.1             | 0.2    |       | V/ $\mu s$     |
| $I_S$     | Supply Current per Amplifier             |  |                   | 380    | 600   |                 | 380    | 700   | $\mu A$        |

### Matching Specifications

| SYMBOL        | PARAMETER                          | CONDITIONS              | LT1024AM/LT1024AC |      |       | LT1024M/LT1024C |      |       | UNITS   |
|---------------|------------------------------------|-------------------------|-------------------|------|-------|-----------------|------|-------|---------|
|               |                                    |                         | MIN               | TYP  | MAX   | MIN             | TYP  | MAX   |         |
|               | Input Offset Voltage Match         |                         | —                 | 20   | 75    | —               | 25   | 150   | $\mu V$ |
| $I_B^+$       | Average Non-Inverting Bias Current |                         | —                 | ± 30 | ± 150 | —               | ± 40 | ± 250 | pA      |
| $I_{OS}^+$    | Non-Inverting Offset Current       |                         | —                 | 30   | 150   | —               | 30   | 300   | pA      |
| $\Delta CMRR$ | Common Mode Rejection Ratio Match  | $V_{CM} = \pm 13.5V$    | 110               | 132  | —     | 106             | 132  | —     | dB      |
| $\Delta PSRR$ | Power Supply Rejection Ratio Match | $V_S = \pm 2V$ to $20V$ | 110               | 132  | —     | 106             | 132  | —     | dB      |
|               | Channel Separation                 | $f \leq 10Hz$ (Note 3)  | 134               | 150  | —     | 134             | 150  | —     | dB      |

## ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $0^\circ C \leq T_A \leq 70^\circ C$  for the LT1024AC and LT1024C;  
 $-55^\circ C \leq T_A \leq 125^\circ C$  for the LT1024AM and LT1024M unless otherwise noted

### Individual Amplifiers

| SYMBOL    | PARAMETER   | CONDITIONS  | LT1024AM/LT1024AC |            |           | LT1024M/LT1024C |            |            | UNITS            |
|-----------|---|---|-------------------|------------|-----------|-----------------|------------|------------|------------------|
|           |   |   | MIN               | TYP        | MAX       | MIN             | TYP        | MAX        |                  |
| $V_{OS}$  | Input Offset Voltage                                    | $0^\circ C$ to $70^\circ C$<br>$-55^\circ C$ to $125^\circ C$ | ●                 | 30         | 120       | ●               | 35         | 200        | $\mu V$          |
|           |   |   | ●                 | 40         | 200       | ●               | 50         | 300        | $\mu V$          |
|           | Average Temperature Coefficient of Input Offset Voltage |   | ●                 | 0.25       | 1.5       | ●               | 0.3        | 2.0        | $\mu V/^\circ C$ |
| $I_{OS}$  | Input Offset Current                                    | $0^\circ C$ to $70^\circ C$<br>$-55^\circ C$ to $125^\circ C$ | ●                 | 40         | 250       | ●               | 50         | 300        | pA               |
|           |   |   | ●                 | 80         | 350       | ●               | 100        | 500        | pA               |
|           | Average Temperature Coefficient of Input Offset Current |   | ●                 | 0.5        | 2.5       | ●               | 0.7        | 3          | $pA/^\circ C$    |
| $I_B$     | Input Bias Current                                      | $0^\circ C$ to $70^\circ C$<br>$-55^\circ C$ to $125^\circ C$ | ●                 | $\pm 40$   | $\pm 250$ | ●               | $\pm 50$   | $\pm 400$  | pA               |
|           |   |   | ●                 | $\pm 100$  | $\pm 700$ | ●               | $\pm 200$  | $\pm 1300$ | pA               |
|           | Average Temperature Coefficient of Input Bias Current   | $0^\circ C$ to $70^\circ C$<br>$-55^\circ C$ to $125^\circ C$ | ●                 | 0.4        | 3         | ●               | 0.5        | 4          | $pA/^\circ C$    |
|           |   |   | ●                 | 1          | 6         | ●               | 2          | 12         | $pA/^\circ C$    |
| $A_{VOL}$ | Large Signal Voltage Gain                               | $V_{OUT} = \pm 12V$ , $R_L \geq 10k\Omega$                    | ●                 | 150        | 1000      | ●               | 150        | 1000       | V/mV             |
|           |   | $V_{OUT} = \pm 10V$ , $R_L \geq 2k\Omega$                     | ●                 | 100        | 600       | ●               | 100        | 600        | V/mV             |
| CMRR      | Common-Mode Rejection Ratio                             | $V_{CM} = \pm 13.5V$  | ●                 | 108        | 128       | ●               | 106        | 128        | dB               |
| PSRR      | Power Supply Rejection Ratio                            | $V_S = \pm 2.5V$ to $\pm 18V$                                 | ●                 | 108        | 128       | ●               | 106        | 128        | dB               |
|           | Input Voltage Range                                     |   | ●                 | $\pm 13.5$ |           | ●               | $\pm 13.5$ |            | V                |
| $V_{OUT}$ | Output Voltage Swing                                    | $R_L = 10k\Omega$   | ●                 | $\pm 13$   | $\pm 14$  | ●               | $\pm 13$   | $\pm 14$   | V                |
| $I_S$     | Supply Current  |   | ●                 | 400        | 800       | ●               | 400        | 900        | $\mu A$          |

2

### Matching Specifications

| SYMBOL        | PARAMETER                          | CONDITIONS  | LT1024AM/LT1024AC |           |           | LT1024M/LT1024C |           |            | UNITS   |      |
|---------------|------------------------------------|---|-------------------|-----------|-----------|-----------------|-----------|------------|---------|------|
|               |                                    |   | MIN               | TYP       | MAX       | MIN             | TYP       | MAX        |         |      |
|               | Input Offset Voltage Match         | $0^\circ C$ to $70^\circ C$<br>$-55^\circ C$ to $125^\circ C$ | ●                 | 35        | 170       | ●               | 45        | 300        | $\mu V$ |      |
|               |                                    |   | ●                 | —         | 50        | 280             | ●         | 70         | 500     |      |
|               | Input Offset Voltage Tracking      |   | ●                 | —         | 0.3       | 2.0             | ●         | —          | 0.4     | 3.5  |
| $I_B^+$       | Average Non-Inverting Bias Current | $0^\circ C$ to $70^\circ C$<br>$-55^\circ C$ to $125^\circ C$ | ●                 | $\pm 40$  | $\pm 300$ | ●               | $\pm 50$  | $\pm 500$  | pA      |      |
|               |                                    |   | ●                 | $\pm 100$ | $\pm 800$ | ●               | $\pm 200$ | $\pm 1400$ | pA      |      |
| $I_{OS}^+$    | Non-Inverting Offset Current       | $0^\circ C$ to $70^\circ C$<br>$-55^\circ C$ to $125^\circ C$ | ●                 | —         | 40        | 300             | ●         | —          | 50      | 500  |
|               |                                    |   | ●                 | —         | 80        | 800             | ●         | —          | 150     | 1500 |
| $\Delta CMRR$ | Common-Mode Rejection Ratio Match  | $V_{CM} = \pm 13.5V$  | ●                 | 106       | 128       | —               | 104       | 128        | —       |      |
| $\Delta PSRR$ | Power Supply Rejection Ratio Match | $V_S = \pm 2.5V$ to $\pm 18V$                                 | ●                 | 106       | 128       | —               | 104       | 128        | —       |      |

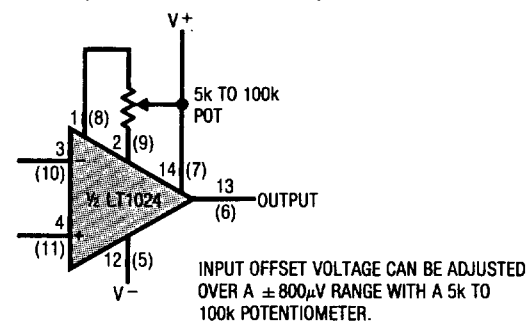
The ● denotes the specifications which apply over the full operating temperature range.

**Note 1:** Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

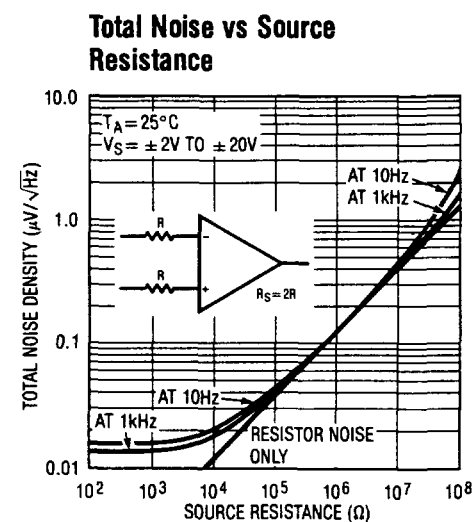
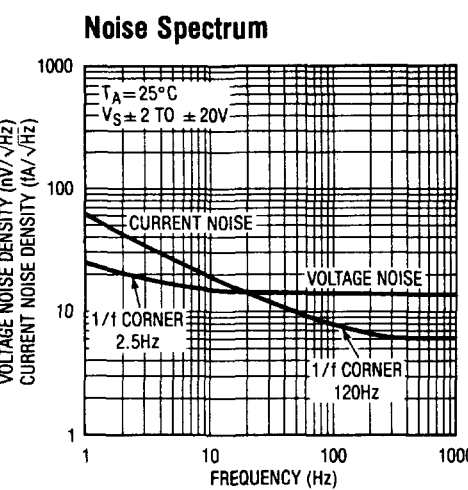
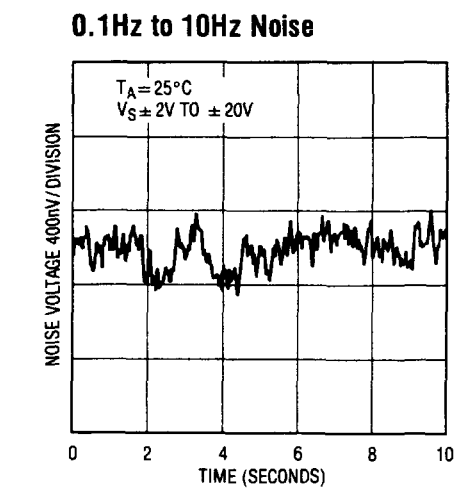
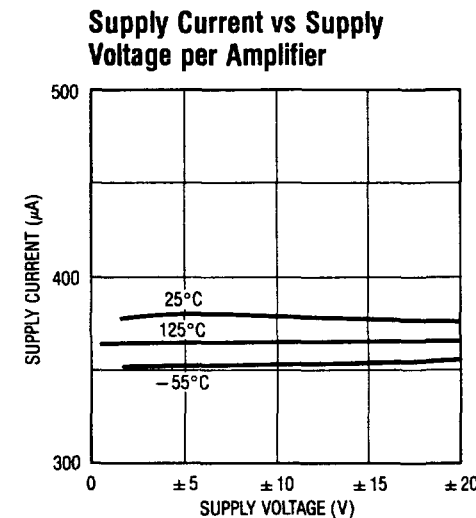
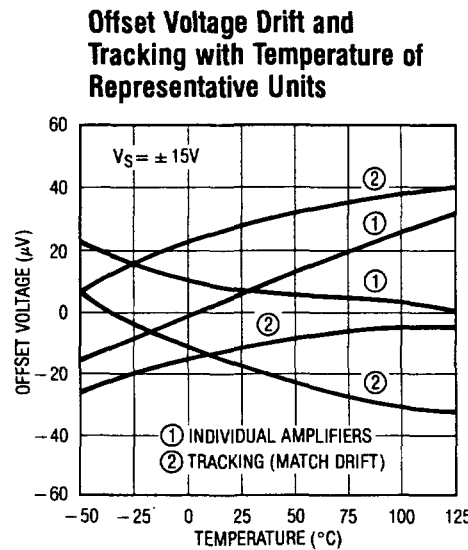
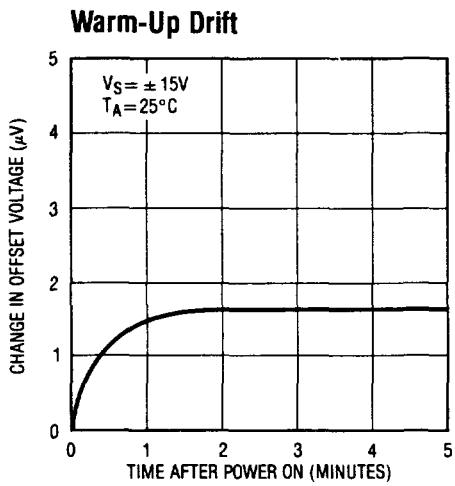
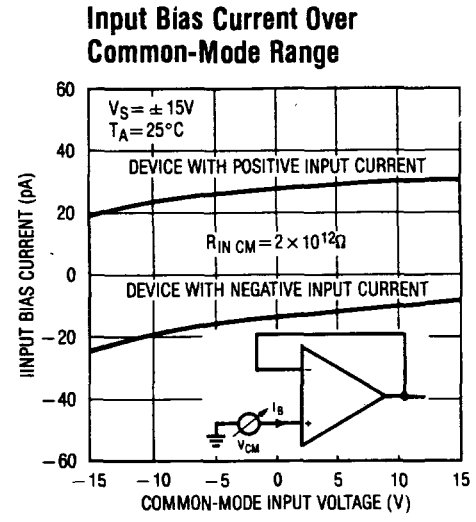
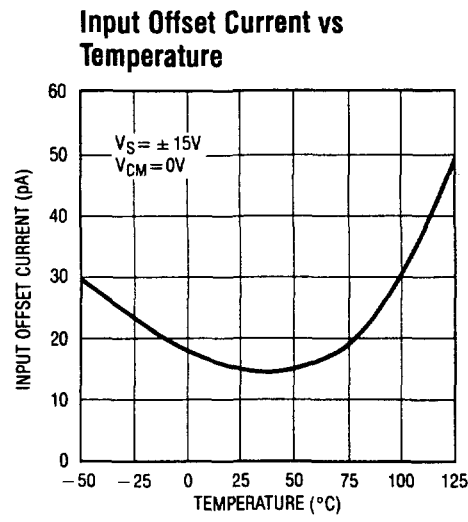
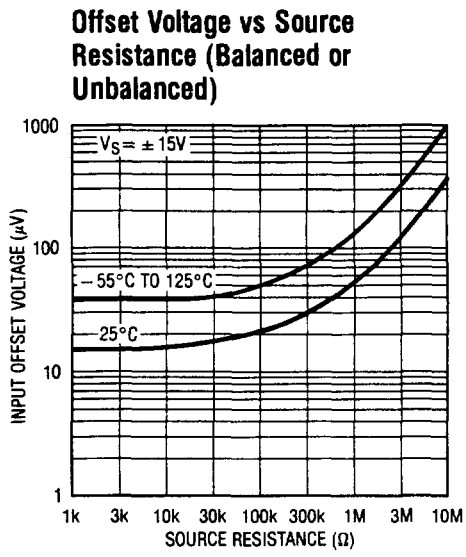
**Note 2:** The  $V^+$  supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The  $V^-$  supply terminals are both connected to the common substrate and must be tied to the same voltage. Both  $V^-$  pins should be used.

**Note 3:** This parameter is tested on a sample basis only.

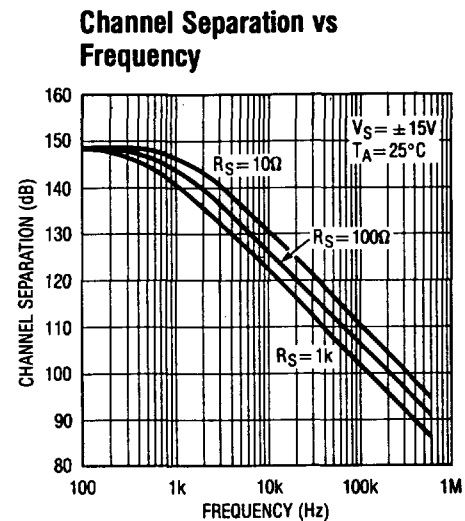
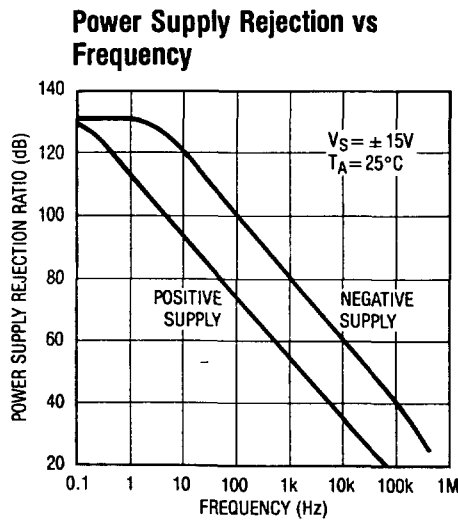
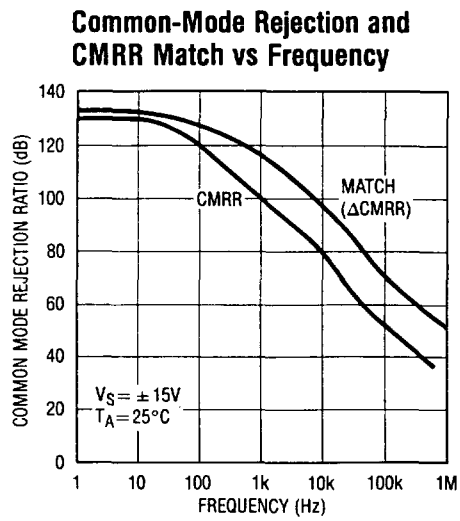
### Optional Offset Nulling Circuit



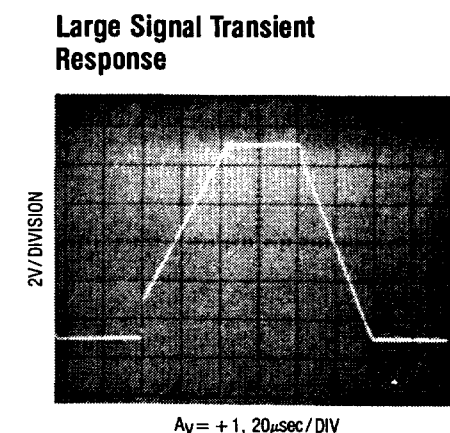
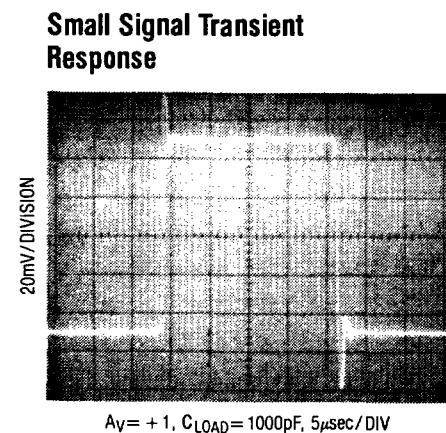
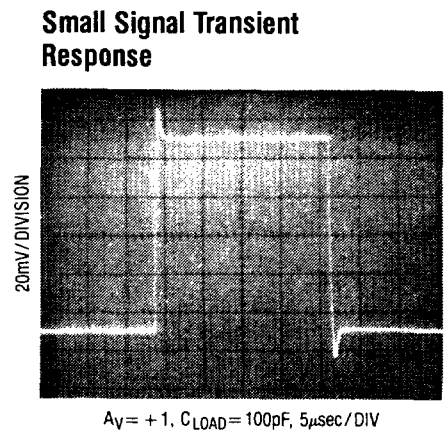
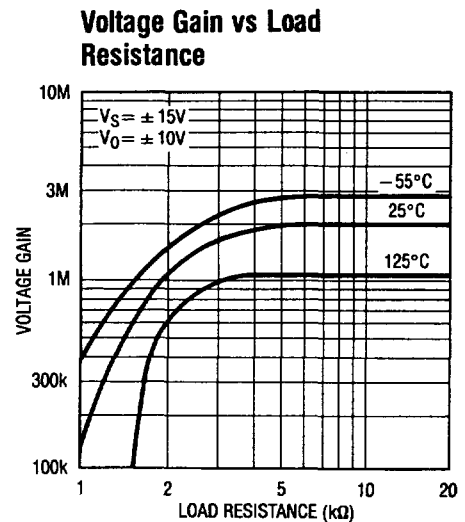
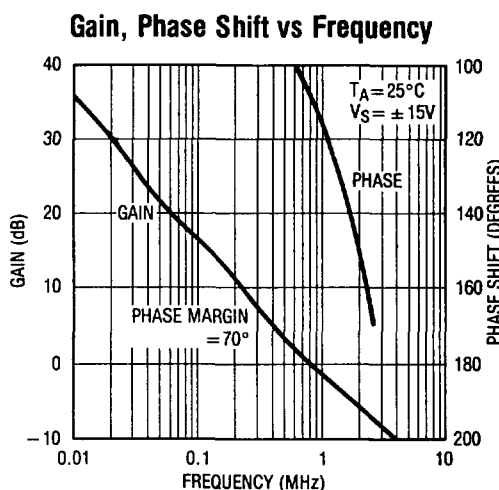
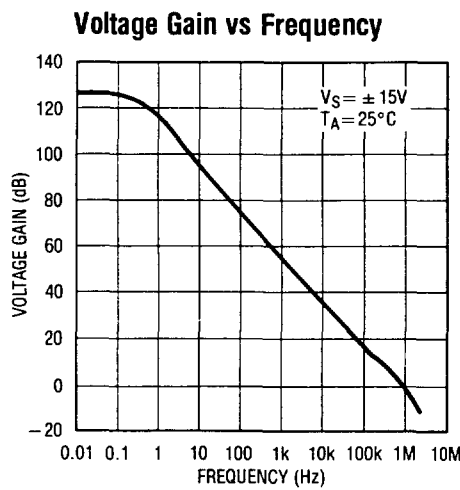
**TYPICAL PERFORMANCE CHARACTERISTICS**



**TYPICAL PERFORMANCE CHARACTERISTICS**



2



## LT1024

### APPLICATIONS INFORMATION

The LT1024 may be inserted directly into OP-10, OP-207 or OP227 sockets with or without removal of external nulling components.

The LT1024 is specified over a wide range of power supply voltages from  $\pm 2V$  to  $\pm 18V$ . Operation with lower supplies is possible down to  $\pm 1.2V$  (two NiCad batteries).

#### Advantages of Matched Dual Op Amps

In many applications, the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references, and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1024. This error cancellation principle holds for a considerable number of input-referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two non-inverting input currents ( $I_B^+$ ). The difference between these two cur-

rents ( $I_{OS}^+$ ) is the offset current of the instrumentation amplifier. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common-mode and power supply rejection ratio match ( $\Delta CMRR$  and  $\Delta PSRR$ ) are best demonstrated with a numerical example:

Assume  $CMRR_A = +1.0\mu V/V$  or 120dB  
and  $CMRR_B = +0.5\mu V/V$  or 126dB,  
then  $\Delta CMRR = 0.5\mu V/V$  or 126dB  
if  $CMRR_B = -0.5\mu V/V$ , which is still 126dB,  
then  $\Delta CMRR = 1.5\mu V/V$  or 116.5dB.

Typical performance of the instrumentation amplifier:

Input offset voltage = 25 $\mu V$ .

Input bias current = 30pA.

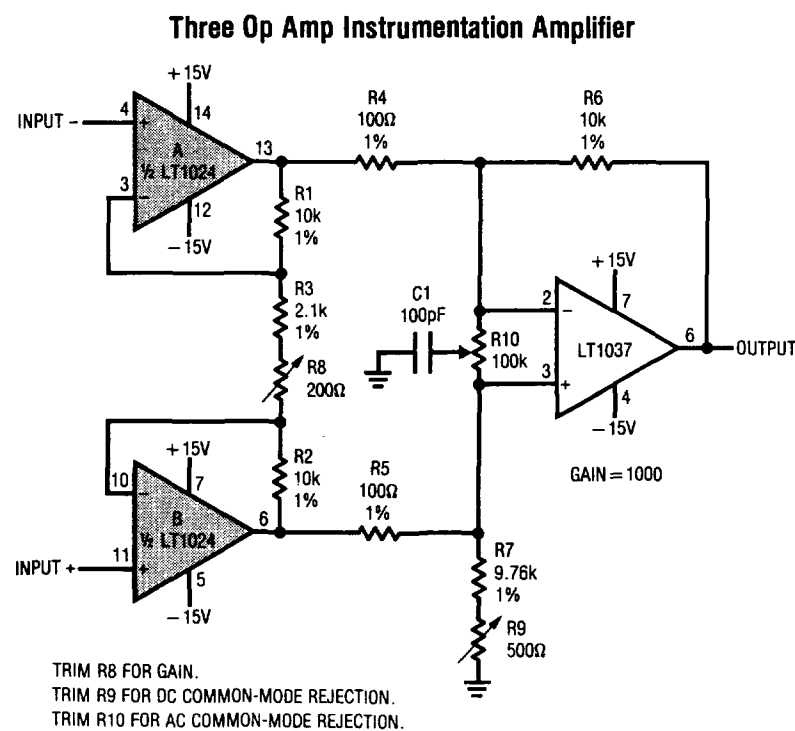
Input resistance =  $10^{12}\Omega$ .

Input offset current = 30pA.

Input noise = 0.7 $\mu V$ p-p.

Power bandwidth ( $V_0 = \pm 10V$ ) = 80kHz.

Clearly, the LT1024, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.



## APPLICATIONS INFORMATION

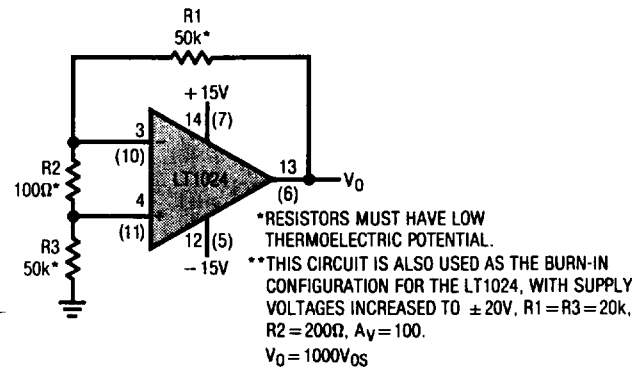
### Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1024, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations, the guard ring should be tied to ground, in non-inverting connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the offset trim terminals can affect offset voltage and drift with temperature.

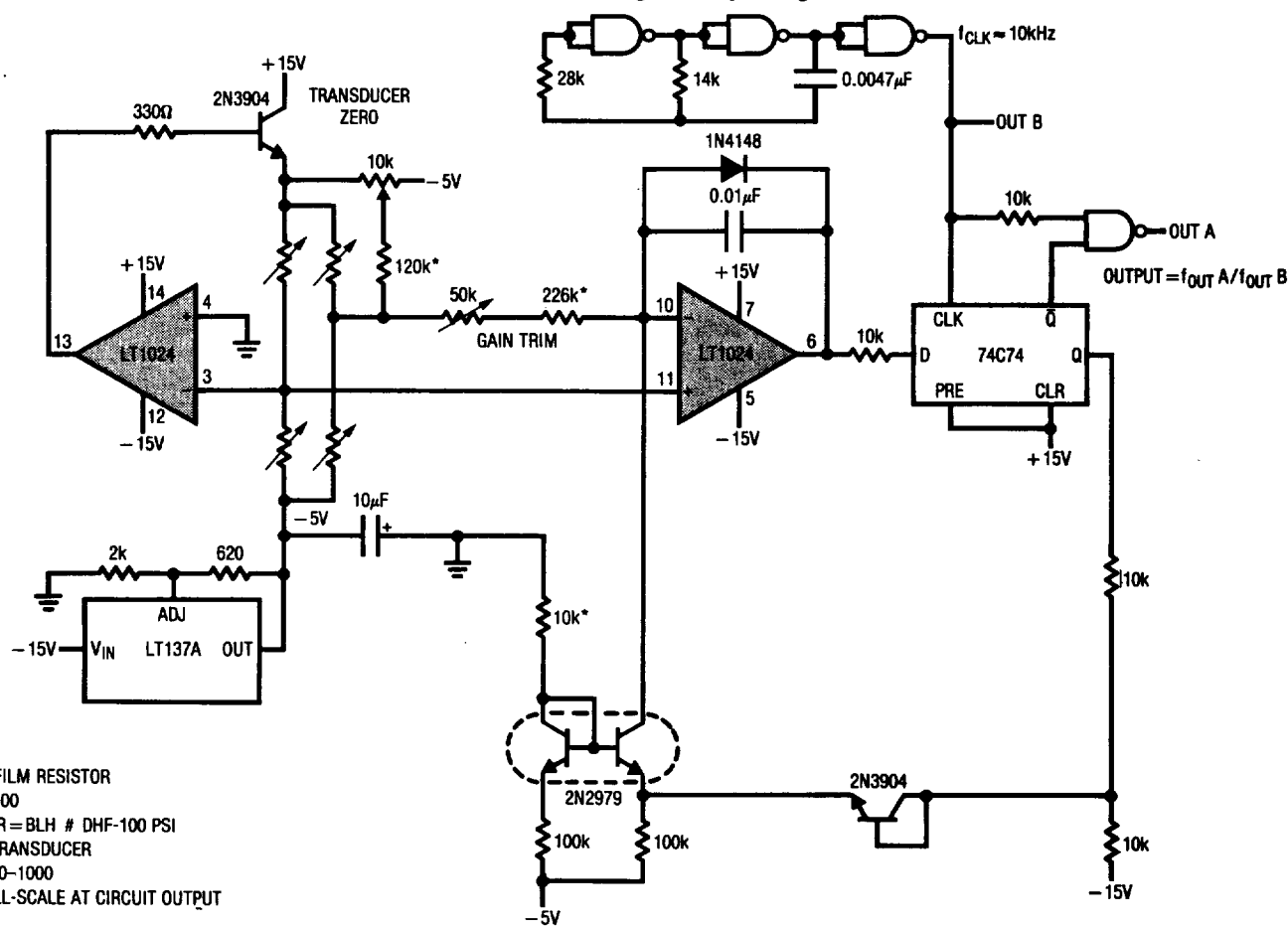
Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

### Test Circuit for Offset Voltage and its Drift with Temperature



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### Direct Pressure Transducer to Digital Output Signal Conditioner

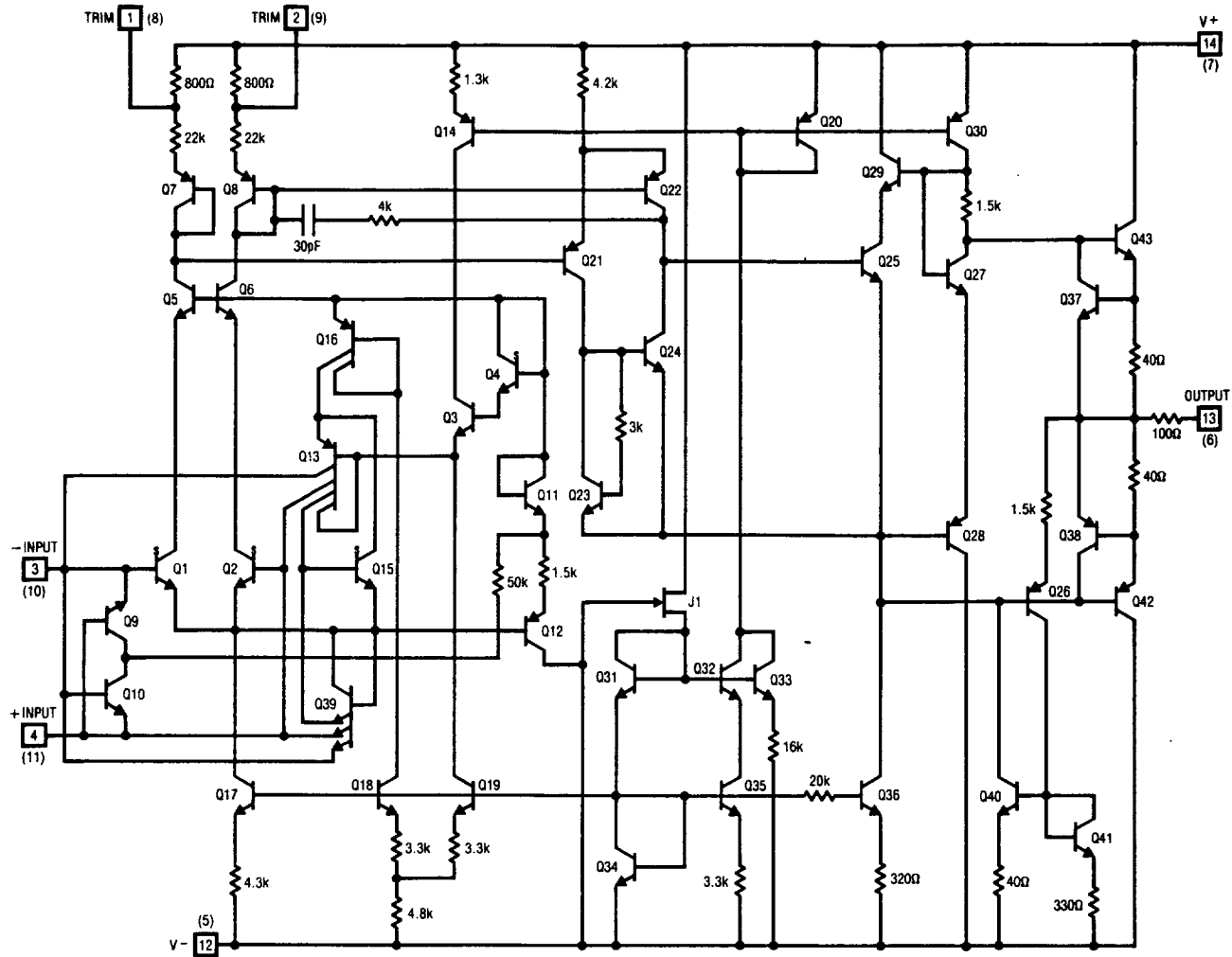


\*1% METAL FILM RESISTOR  
 GATES = 74C00  
 TRANSDUCER = BLH # DHF-100 PSI  
 PRESSURE TRANSDUCER  
 0-100 PSI = 0-1000  
 COUNTS FULL-SCALE AT CIRCUIT OUTPUT

# LT1024

## SCHEMATIC DIAGRAM

1/2 LT1024



## PACKAGE DESCRIPTION

D14 Package 14-Lead Hermetic DIP (Sidebrazed)

N14 Package 14-Lead Plastic

