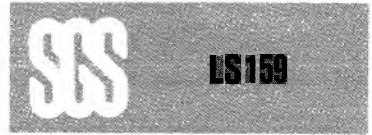


# LINEAR INTEGRATED CIRCUIT



## HIGH RELIABILITY TRANSISTOR ARRAY

The LS159 is an array of 5 NPN transistors on a common monolithic substrate in an SO-14 (14-lead plastic micropackage). This package is easily mounted on thick and thin film hybrid circuits. Two transistors are internally connected to form a differential amplifier. The transistors of the LS159 are well suited to low noise general purposes and to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete components in conventional circuits; in addition they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The device is also available with a hermetic goldchip (LS8159M) that is particularly suitable for professional and telecom applications, wherever very high MTBF are required. This performance is guaranteed by silicon nitride sealing of chip surface and Ti-Pt-Au metallization, protected with a double passivated layer, providing resistance against contamination, electrolytic corrosion and electromigration.

### ABSOLUTE MAXIMUM RATINGS

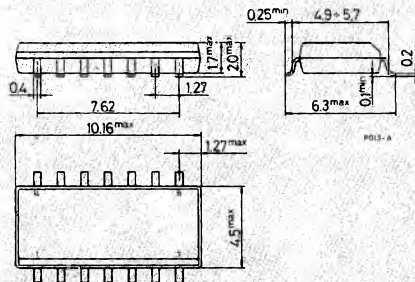
		Each transistor	Total package
$V_{CBO}$	Collector-base voltage ( $I_E = 0$ )	20 V	—
$V_{CEO}^*$	Collector-emitter voltage ( $I_B = 0$ )	15 V	—
$V_{CSS}^*$	Collector-substrate voltage	20 V	—
$V_{EBO}$	Emitter-base voltage ( $I_C = 0$ )	5 V	—
$I_C$	Collector current	50 mA	—
$P_{tot}$	Total power dissipation at $T_{amb} = 25^\circ C$	250 mW	500 mW
$T_{stg}, T_J$	Storage, and junction temperature	-55 to 150 °C	
	Soldering dip or wave at 5 s	260 °C	
	11 s	235 °C	

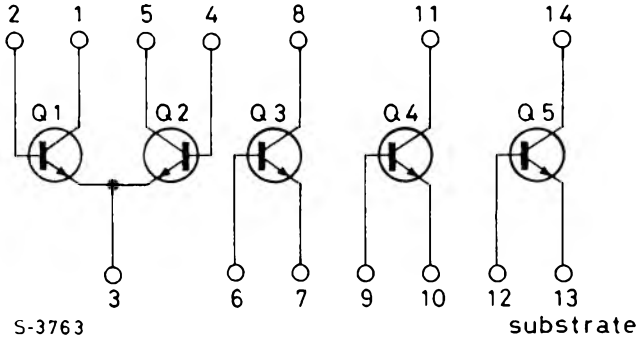
\*) The collector of each transistor of the LS159 is isolated from the substrate by an integrated diode. The substrate (pin 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

ORDERING NUMBERS: LS 159M – LS 8159M

### MECHANICAL DATA

Dimensions in mm



**SCHEMATIC DIAGRAM**

**THERMAL DATA**

$R_{th\ j-amb}$ Thermal resistance junction-ambient	max 250 °C/W
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**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$  unless otherwise specified)

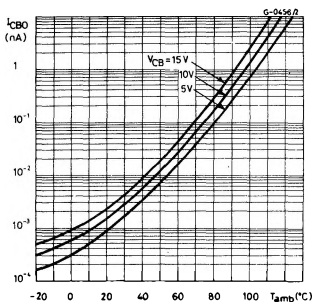
Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
$I_{CBO}$ Collector cutoff current ( $I_E = 0$ )	$V_{CB} = 10\text{V}$		0.002	40	nA	1
$I_{CEO}$ Collector cutoff current ( $I_B = 0$ )	$V_{CE} = 10\text{V}$		see curve	0.5	$\mu\text{A}$	2
$ I_{B1} - I_{B2} $ Input offset current	$I_C = 1\text{mA}$ $V_{CE} = 3\text{V}$		0.3	2	$\mu\text{A}$	7
$V_{CBO}$ Collector-base voltage ( $I_E = 0$ )	$I_C = 10\ \mu\text{A}$	20	60		V	—
$V_{CEO}$ Collector-emitter voltage ( $I_B = 0$ )	$I_C = 1\text{mA}$	15	24		V	—
$V_{CSS}$ Collector-substrate voltage ( $I_{CSS} = 0$ )	$I_C = 10\ \mu\text{A}$	20	60		V	—
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_C = 10\text{mA}$ $I_B = 1\text{mA}$		0.23		V	—



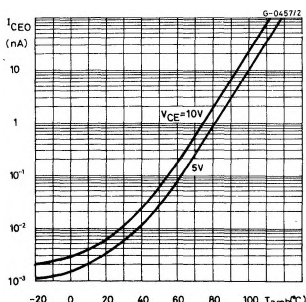
**ELECTRICAL CHARACTERISTICS** (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
$V_{EBO}$	Emitter-base voltage ( $I_C = 0$ )	$I_E = 10 \mu A$	5	7		V	—
$V_{BE}$	Base-emitter voltage	$I_E = 1 \text{ mA}$ $V_{CE} = 3V$ $I_E = 10 \text{ mA}$ $V_{CE} = 3V$		0.71 0.8		V V	4
$ V_{BE1} - V_{BE2} $	Input offset voltage	$I_C = 1 \text{ mA}$ $V_{CE} = 3V$		0.45	5	mV	4-6
$ V_{BE3} - V_{BE4} $	Input offset voltage						
$ V_{BE4} - V_{BE5} $	Input offset voltage						
$ V_{BE5} - V_{BE4} $	Input offset voltage						
$\frac{\Delta V_{BE}}{\Delta T}$	Base-emitter voltage temperature coefficient	$I_C = 1 \text{ mA}$ $V_{CE} = 3V$		-1.9		mV/°C	5
$\frac{ V_{BE1} - V_{BE2} }{\Delta T}$	Input offset voltage temperature coefficient	$I_C = 1 \text{ mA}$ $V_{CE} = 3V$		1.1		$\mu V/^\circ C$	6
$h_{FE}$	DC current gain	$I_C = 10 \text{ mA}$ $V_{CE} = 3V$ $I_C = 1 \text{ mA}$ $V_{CE} = 3V$ $I_C = 10 \mu A$ $V_{CE} = 3V$	40	100 100 54		— — —	3
$f_T$	Transition frequency	$I_C = 3 \text{ mA}$ $V_{CE} = 3V$	300	550		MHz	14
NF	Noise figure	$I_C = 100 \mu A$ $V_{CE} = 3V$ $R_g = 1 \text{ k}\Omega$ $f = 1 \text{ kHz}$		3.25		dB	8
$h_{ie}$	Input impedance	$I_C = 1 \text{ mA}$ $V_{CE} = 3V$ $f = 1 \text{ KHz}$		3.5		k $\Omega$	9
$h_{fe}$	Forward current transfer ratio						
$h_{re}$	Reverse voltage transfer ratio						
$h_{oe}$	Output admittance						
$V_{ie}$	Input admittance	$I_C = 1 \text{ mA}$ $V_{CE} = 3V$ $f = 1 \text{ MHz}$		0.3+j0.04		mS	11
$V_{fe}$	Forward transadmittance						
$V_{re}$	Reverse transadmittance						
$V_{oe}$	Output admittance						
$C_{EBO}$	Emitter-base capacitance	$I_C = 0$ $V_{EB} = 3V$		0.6		pF	—
$C_{CBO}$	Collector-base capacitance	$I_E = 0$ $V_{CB} = 3V$		0.58		pF	—
$C_{CSS}$	Collector-substrate capacitance	$I_C = 0$ $V_{CSS} = 3V$		2.8		pF	—

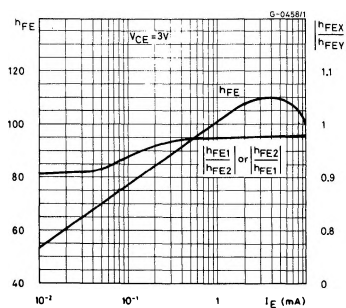
**Fig. 1 - Collector cutoff current vs. ambient temperature**



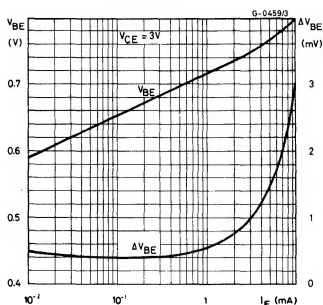
**Fig. 2 - Collector cutoff current vs. ambient temperature**



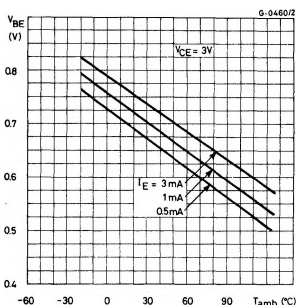
**Fig. 3 - DC current gain**



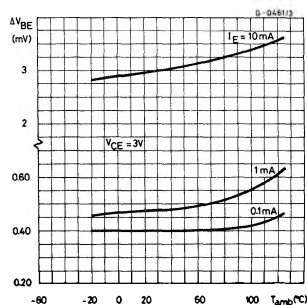
**Fig. 4 - Input voltage and input offset voltage vs. emitter current**



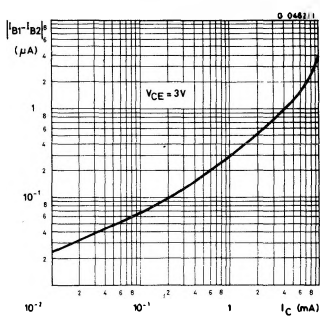
**Fig. 5 - Input characteristics for each transistor**



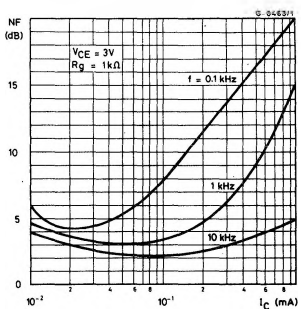
**Fig. 6 - Input offset voltage vs. ambient temperature**



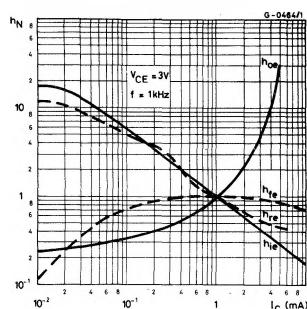
**Fig. 7 - Input offset current for matched transistor pair**



**Fig. 8 - Noise figure vs. collector current**



**Fig. 9 - Normalized h parameters vs. collector current**





LS159

Fig. 10 - Forward admittance vs. frequency

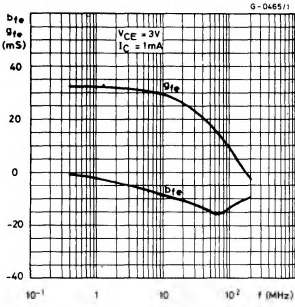


Fig. 11 - Input admittance vs. frequency

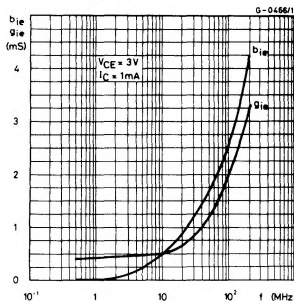


Fig. 12 - Output admittance vs. frequency

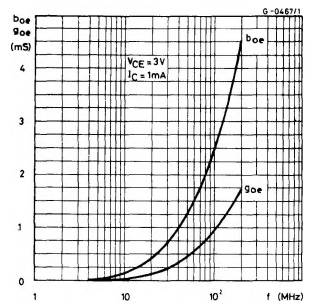


Fig. 13 - Reverse admittance vs. frequency

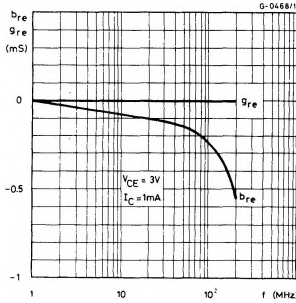


Fig. 14 - Transition frequency vs. collector current

