LMV821 Single/ LMV822 Dual/ LMV824 Quad Low Voltage, Low Power, R-to-R Output, 5 MHz Op Amps

Check for Samples: LMV821-N, LMV822-N, LMV824-N

FEATURES

- **(For Typical, 5 V Supply Values; Unless Otherwise Noted)**
- **Ultra Tiny, SC70-5 Package 2.0 x 2.0 x 1.0 mm**
- **Guaranteed 2.5 V, 2.7 V and 5 V Performance**
- **Maximum VOS 3.5 mV (Guaranteed)**
- **VOS Temp. Drift 1 uV/° C**
- **GBW product @ 2.7 V 5 MHz**
- **I_{Supply} @ 2.7 V 220 µA/Amplifier**
- **Minimum SR 1.4 V/us (Guaranteed)**
- **CMRR 90 dB**
- **PSRR 85 dB**
- **V_{CM} @ 5V -0.3V to 4.3V**
- **Rail-to-Rail (R-to-R) Output Swing**
- **@600 Ω Load 160 mV from rail**
- **@10 kΩ Load 55 mV from rail**
- **Stable with High Capacitive Loads (Refer to Application Section)**

APPLICATIONS

- **Cordless Phones**
- **Cellular Phones**
- **Laptops**
- **PDAs**
- **PCMCIA**

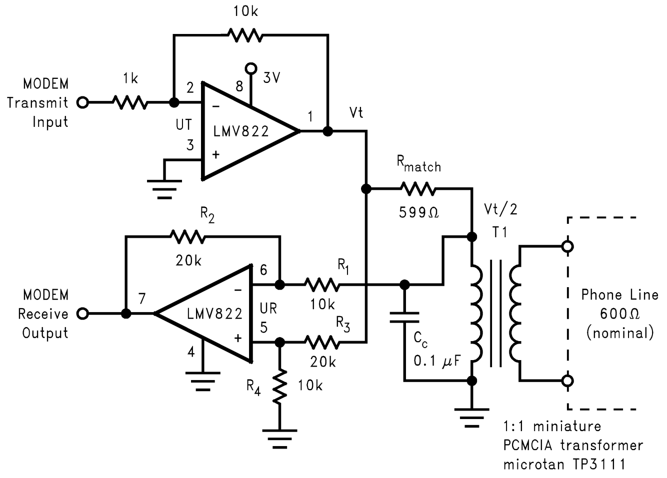
DESCRIPTION

The LMV821/LMV822/LMV824 bring performance and economy to low voltage / low power systems. With a 5 MHz unity-gain frequency and a guaranteed 1.4 V/µs slew rate, the quiescent current is only 220 µA/amplifier (2.7 V). They provide rail-to-rail (R-to-R) output swing into heavy loads (600 Ω Guarantees). The input common-mode voltage range includes ground, and the maximum input offset voltage is 3.5mV (Guaranteed). They are also capable of comfortably driving large capacitive loads (refer to the application notes section).

The LMV821 (single) is available in the ultra tiny SC70-5 package, which is about half the size of the previous title holder, the SOT23-5.

Overall, the LMV821/LMV822/LMV824 (Single/Dual/Quad) are low voltage, low power, performance op amps, that can be designed into a wide range of applications, at an economical price.

Telephone-line Transceiver for a PCMCIA Modem Card



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Machine Model	100V
Human Body Model	
LMV822/824	2000V
LMV821	1500V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ – V^-$)	5.5V
Output Short Circuit to V^+ (3)	
Output Short Circuit to V^- (3)	
Soldering Information	
Infrared or Convection (20 sec)	235°C
Storage Temperature Range	−65°C to 150°C
Junction Temperature (4)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

(2) Human body model, 1.5 kΩ in series wth 100 pF. Machine model, 200Ω in series with 100 pF.

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

(4) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings (1)

Supply Voltage	2.5V to 5.5V
Temperature Range	
LMV821, LMV822, LMV824	$−40°C \leq T_J \leq 85°C$
Thermal Resistance (θ_{JA})	
Ultra Tiny SC70-5 Package, 5-Pin Surface Mount	440 °C/W
Tiny SOT23-5 Package, 5-Pin Surface Mount	265 °C/W
SO Package, 8-Pin Surface Mount	190 °C/W
MSOP Package, 8-Pin Mini Surface Mount	235 °C/W
SO Package, 14-Pin Surface Mount	145 °C/W
TSSOP Package, 14-Pin	155 °C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	LMV821/822/824 Limit (2)	Units
V_{OS}	Input Offset Voltage		1	3.5	mV
				4	max
TCV_{OS}	Input Offset Voltage Average Drift		1		μV/°C
I_B	Input Bias Current		30	90	nA
				140	max
I_{OS}	Input Offset Current		0.5	30	nA
				50	max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V	85	70	dB
				68	min
+PSRR	Positive Power Supply Rejection Ratio	1.7V ≤ V^+ ≤ 4V, V^-= 1V, V_O = 0V, V_{CM} = 0V	85	75	dB
				70	min
−PSRR	Negative Power Supply Rejection Ratio	-1.0V ≤ V^-≤ -3.3V, V^+ = 1.7V, V_O = 0V, V_{CM} = 0V	85	73	dB
				70	min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2	V
					max
			2.0	1.9	V
					min
A_V	Large Signal Voltage Gain	Sourcing, R_L = 600Ω to 1.35V, V_O = 1.35V to 2.2V	100	90	dB
				85	min
		Sinking, R_L = 600Ω to 1.35V, V_O = 1.35V to 0.5V	90	85	dB
				80	min
		Sourcing, R_L = 2kΩ to 1.35V, V_O = 1.35V to 2.2V	100	95	dB
				90	min
		Sinking, R_L = 2kΩ to 1.35, V_O = 1.35 to 0.5V	95	90	dB
				85	min
V_O	Output Swing	V^+ = 2.7V, R_L= 600Ω to 1.35V	2.58	2.50	V
				2.40	min
			0.13	0.20	V
				0.30	max
		V^+ = 2.7V, R_L= 2kΩ to 1.35V	2.66	2.60	V
				2.50	min
			0.08	0.120	V
				0.200	max
I_O	Output Current	Sourcing, V_O = 0V	16	12	mA
					min
		Sinking, V_O = 2.7V	26	12	mA
					min
I_S	Supply Current	LMV821 (Single)	0.22	0.3	mA
				0.5	max
		LMV822 (Dual)	0.45	0.6	mA
				0.8	max
		LMV824 (Quad)	0.72	1.0	mA
				1.2	max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

2.5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. $V^+ = 2.5V$, $V^- = 0V$, $V_{CM} = 1.0V$, $V_O = 1.25V$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	**Parameter**	**Condition**	**Typ** [(1)]	**LMV821/822/824 Limit** [(2)]	**Units**
V_{OS}	Input Offset Voltage		1	3.5	mV
				4	max
V_O	Output Swing	$V^+ = 2.5V$, $R_L = 600\Omega$ to 1.25V	2.37	2.30	V
				2.20	min
			0.13	0.20	V
				0.30	max
		$V^+ = 2.5V$, $R_L = 2k\Omega$ to 1.25V	2.46	2.40	V
				2.30	min
			0.08	0.12	V
				0.20	max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 1.0V$, $V_O = 1.35V$ and $R_L > 1 M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ[1]	LMV821/822/824 Limit [2]	Units
SR	Slew Rate	[3]	1.5		V/μs
GBW	Gain-Bandwdth Product		5		MHz
Φ_m	Phase Margin		61		Deg.
G_m	Gain Margin		10		dB
	Amp-to-Amp Isolation	[4]	135		dB
e_n	Input-Related Voltage Noise	f = 1 kHz, $V_{CM} = 1V$	28		$\frac{nV}{\sqrt{Hz}}$ (1)
i_n	Input-Referred Current Noise	f = 1 kHz	0.1		$\frac{pA}{\sqrt{Hz}}$ (2)
THD	Total Harmonic Distortion	f = 1 kHz, $A_V = -2$, $R_L = 10 k\Omega$, $V_O = 4.1 V_{PP}$	0.01		%

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) $V^+ = 5V$. Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred, $V^+ = 5V$ and $R_L = 100k\Omega$ connected to 2.5V. Each amp excited in turn with 1 kHz to produce $V_O = 3 V_{PP}$.

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	LMV821/822/824 Limit (2)	Units
V_{OS}	Input Offset Voltage		1	3.5	mV
				4.0	max
TCV_{OS}	Input Offset Voltage Average Drift		1		μV/°C
I_B	Input Bias Current		40	100	nA
				150	max
I_{OS}	Input Offset Current		0.5	30	nA
				50	max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4.0V	90	72	dB
				70	min
+PSRR	Positive Power Supply Rejection Ratio	1.7V ≤ V^+ ≤ 4V, V^-= 1V, V_O = 0V, V_{CM} = 0V	85	75	dB
				70	min
−PSRR	Negative Power Supply Rejection Ratio	-1.0V ≤ V^-≤ -3.3V, V^+ = 1.7V, V_O = 0V, V_{CM} = 0V	85	73	dB
				70	min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2	V
					max
			4.3	4.2	V
					min
A_V	Large Signal Voltage Gain	Sourcing, R_L = 600Ω to 2.5V, V_O = 2.5 to 4.5V	105	95	dB
				90	min
		Sinking, R_L = 600Ω to 2.5V, V_O = 2.5 to 0.5V	105	95	dB
				90	min
		Sourcing, R_L = 2kΩ to 2.5V, V_O = 2.5 to 4.5V	105	95	dB
				90	min
		Sinking, R_L = 2kΩ to 2.5, V_O = 2.5 to 0.5V	105	95	dB
				90	min
V_O	Output Swing	V^+ = 5V,R_L = 600Ω to 2.5V	4.84	4.75	V
				4.70	min
			0.17	0.250	V
				.30	max
		V^+ = 5V, R_L = 2kΩ to 2.5V	4.90	4.85	V
				4.80	min
			0.10	0.15	V
				0.20	max
I_O	Output Current	Sourcing, V_O = 0V	45	20	mA
				15	min
		Sinking, V_O = 5V	40	20	mA
				15	min
I_S	Supply Current	LMV821 (Single)	0.30	0.4	mA
				0.6	max
		LMV822 (Dual)	0.5	0.7	mA
				0.9	max
		LMV824 (Quad)	1.0	1.3	mA
				1.5	max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 2V$, $V_O = 2.5V$ and $R_L > 1 M\Omega$. **Boldface** limits apply at the temperature extremes.

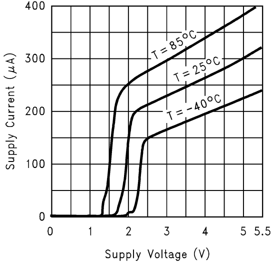
Symbol	Parameter	Conditions	Typ (1)	LMV821/822/824 Limit (2)	Units
SR	Slew Rate	(3)	2.0	1.4	V/μs min
GBW	Gain-Bandwdth Product		5.6		MHz
Φ_m	Phase Margin		67		Deg.
G_m	Gain Margin		15		dB
	Amp-to-Amp Isolation	(4)	135		dB
e_n	Input-Related Voltage Noise	f = 1 kHz, $V_{CM} = 1V$	24		$\frac{nV}{\sqrt{Hz}}$ (3)
i_n	Input-Referred Current Noise	f = 1 kHz	0.25		$\frac{pA}{\sqrt{Hz}}$ (4)
THD	Total Harmonic Distortion	f = 1 kHz, $A_V = -2$, $R_L = 10 k\Omega$, $V_O = 4.1 V_{PP}$	0.01		%

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) $V^+ = 5V$. Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred, $V^+ = 5V$ and $R_L = 100k\Omega$ connected to 2.5V. Each amp excited in turn with 1 kHz to produce $V_O = 3 V_{PP}$.

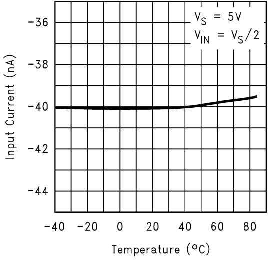
Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

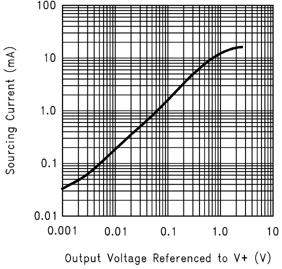
Supply Current vs. Supply Voltage (LMV821)



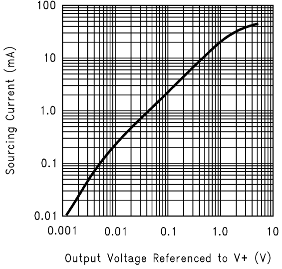
Input Current vs. Temperature



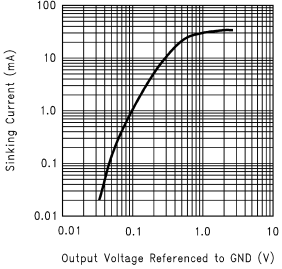
Sourcing Current vs. Output Voltage (V_S = 2.7V)



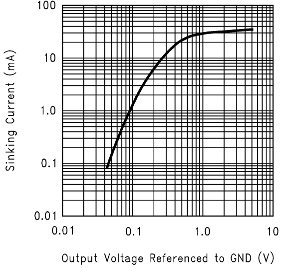
Sourcing Current vs Output Voltage (V_S = 5V)



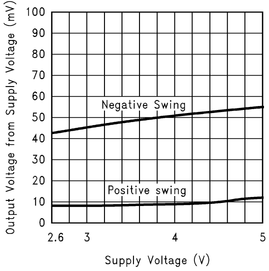
Sinking Current vs. Output Voltage (V_S = 2.7V)



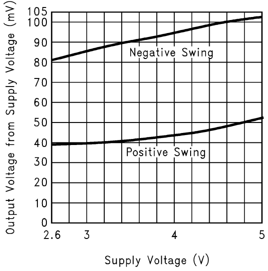
Sinking Current vs. Output Voltage (V_S = 5V)



Output Voltage Swing vs. Supply Voltage (R_L = 10kΩ)



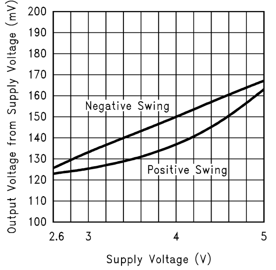
Output Voltage Swing vs. Supply Voltage (R_L = 2kΩ)



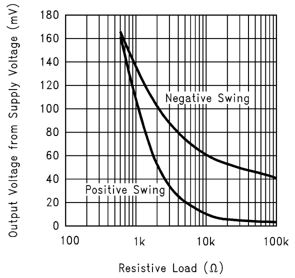
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

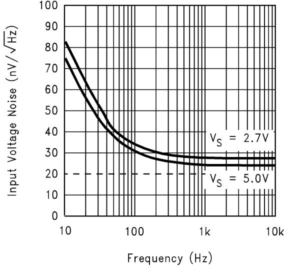
Output Voltage Swing vs. Supply Voltage (R_L = 600Ω)



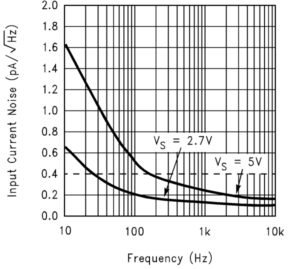
Output Voltage Swing vs. Load Resistance



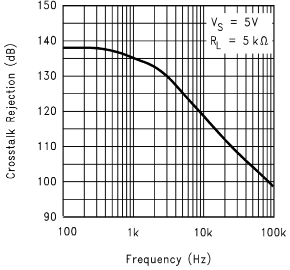
Input Voltage Noise vs. Frequency



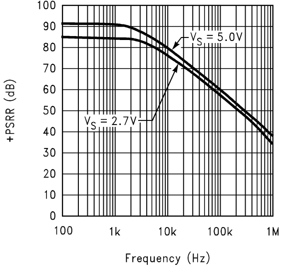
Input Current Noise vs. Frequency



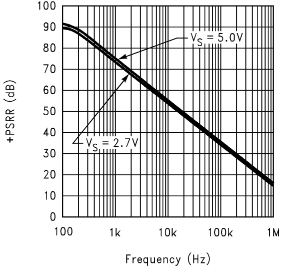
Crosstalk Rejection vs. Frequency



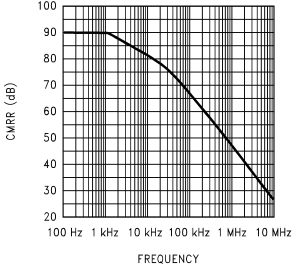
+PSRR vs. Frequency



-PSRR vs. Frequency



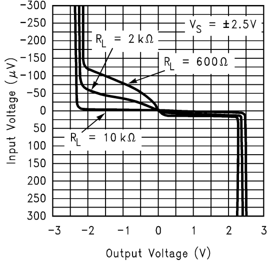
CMRR vs. Frequency



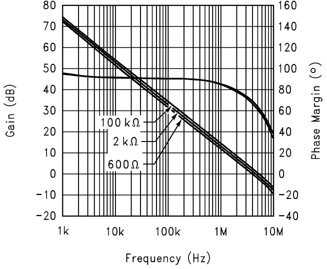
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

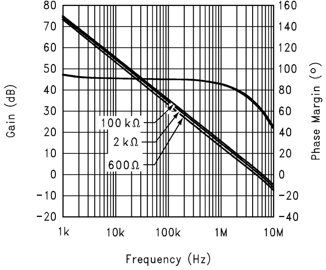
Input Voltage vs. Output Voltage



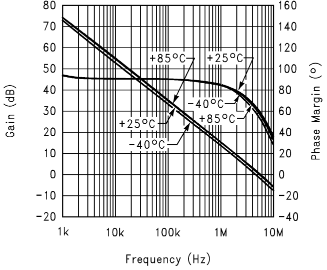
Gain and Phase Margin vs. Frequency (R_L = 100kΩ, 2kΩ, 600Ω) 2.7V



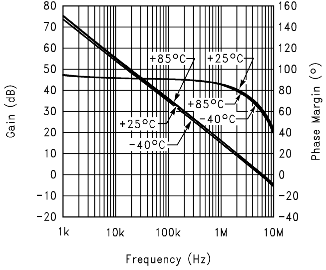
Gain and Phase Margin vs. Frequency (R_L = 100kΩ, 2kΩ, 600Ω) 5V



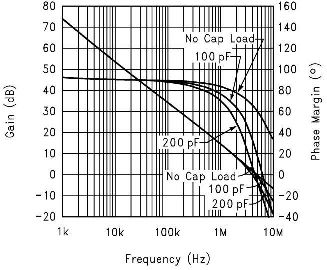
Gain and Phase Margin vs. Frequency (Temp.= 25, -40, 85°C, R_L = 10kΩ) 2.7V



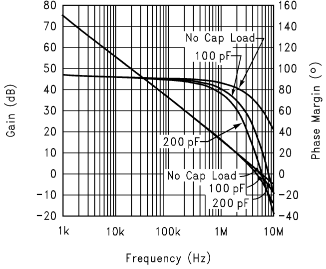
Gain and Phase Margin vs. Frequency (Temp.= 25, -40, 85 °C, R_L = 10kΩ) 5V



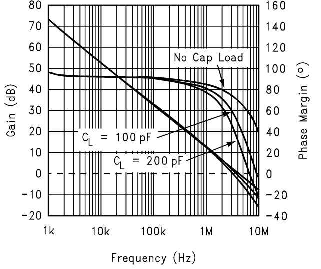
Gain and Phase Margin vs. Frequency (C_L = 100pF, 200pF, 0pF, R_L = 10kΩ)2.7V



Gain and Phase Margin vs. Frequency (C_L = 100pF, 200pF, 0pF R_L = 10kΩ) 5V

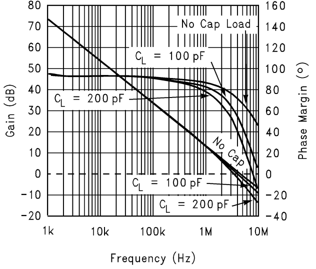


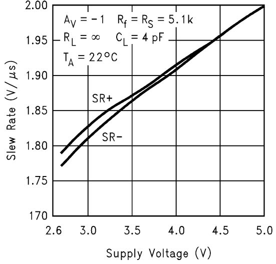
Gain and Phase Margin vs. Frequency (C_L = 100pF, 200pF, 0pF R_L = 600Ω) 2.7V

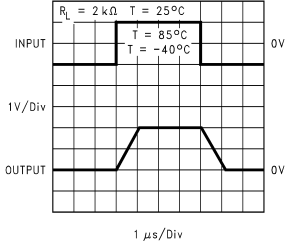


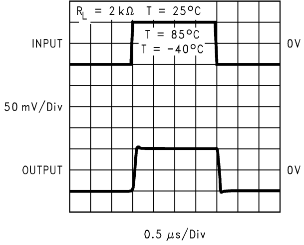
Typical Performance Characteristics (continued)

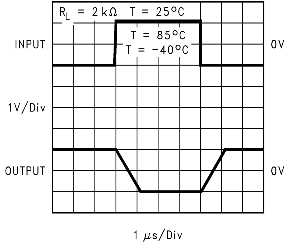
Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

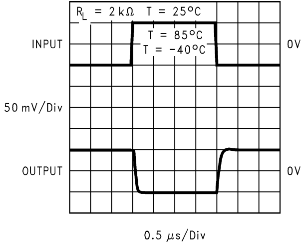

Gain and Phase Margin vs. Frequency (C_L = 100pF, 200pF, 0pF R_L = 600Ω) 5V

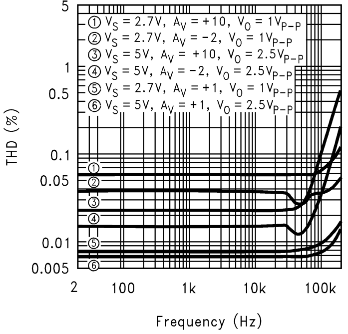

Slew Rate vs. Supply Voltage


Non-Inverting Large Signal Pulse Response


Non-Inverting Small Signal Pulse Response


Inverting Large Signal Pulse Response


Inverting Small Signal Pulse Response


THD vs. Frequency

Application Note

This application note is divided into two sections: design considerations and Application Circuits.

DESIGN CONSIDERATIONS

This section covers the following design considerations:

1. Frequency and Phase Response Considerations
2. Unity-Gain Pulse Response Considerations
3. Input Bias Current Considerations

FREQUENCY AND PHASE RESPONSE CONSIDERATIONS

The relationship between open-loop frequency response and open-loop phase response determines the closed-loop stability performance (negative feedback). The open-loop phase response causes the feedback signal to shift towards becoming positive feedback, thus becoming unstable. The further the output phase angle is from the input phase angle, the more stable the negative feedback will operate. Phase Margin (φ_m) specifies this output-to-input phase relationship at the unity-gain crossover point. Zero degrees of phase-margin means that the input and output are completely in phase with each other and will sustain oscillation at the unity-gain frequency.

The AC tables show φ_m for a no load condition. But φ_m changes with load. The Gain and Phase margin vs Frequency plots in the curve section can be used to graphically determine the φ_m for various loaded conditions. To do this, examine the phase angle portion of the plot, find the phase margin point at the unity-gain frequency, and determine how far this point is from zero degree of phase-margin. The larger the phase-margin, the more stable the circuit operation.

The bandwidth is also affected by load. The graphs of Figure 1 and Figure 2 provide a quick look at how various loads affect the φ_m and the bandwidth of the LMV821/822/824 family. These graphs show capacitive loads reducing both φ_m and bandwidth, while resistive loads reduce the bandwidth but increase the φ_m. Notice how a 600Ω resistor can be added in parallel with 220 picofarads capacitance, to increase the φ_m 20°(approx.), but at the price of about a 100 kHz of bandwidth.

Overall, the LMV821/822/824 family provides good stability for loaded condition.

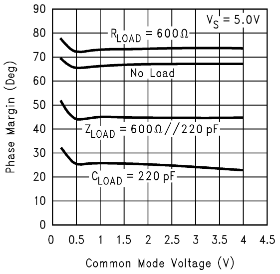


Figure 1. Phase Margin vs Common Mode Voltage for Various Loads

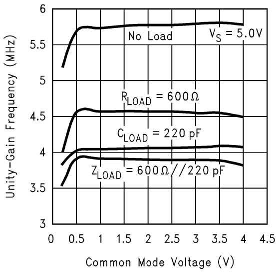


Figure 2. Unity-Gain Frequency vs Common Mode Voltage for Various Loads

UNITY GAIN PULSE RESPONSE CONSIDERATION

A pull-up resistor is well suited for increasing unity-gain, pulse response stability. For example, a 600 Ω pull-up resistor reduces the overshoot voltage by about 50%, when driving a 220 pF load. Figure 3 shows how to implement the pull-up resistor for more pulse response stability.

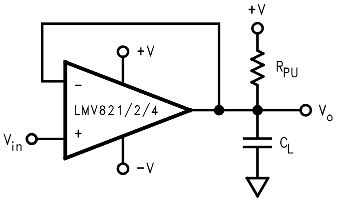


Figure 3. Using a Pull-up Resistor at the Output for Stabilizing Capacitive Loads

Higher capacitances can be driven by decreasing the value of the pull-up resistor, but its value shouldn't be reduced beyond the sinking capability of the part. An alternate approach is to use an isolation resistor as illustrated in Figure 4 .

Figure 5 shows the resulting pulse response from a LMV824, while driving a 10,000 pF load through a 20Ω isolation resistor.

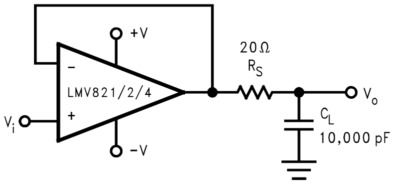


Figure 4. Using an Isolation Resistor to Drive Heavy Capacitive Loads

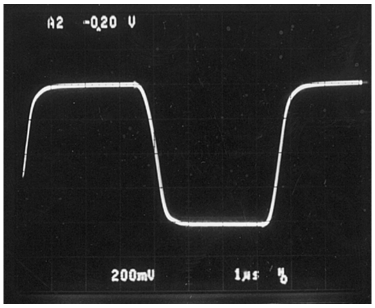


Figure 5. Pulse Response per Figure 4

INPUT BIAS CURRENT CONSIDERATION

Input bias current (I_B) can develop a somewhat significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 90 nA (max @ room) and R_F is 100 kΩ, then an offset of 9 mV will be developed ($V_{OS}=I_B x\ R_F$).Using a compensation resistor (R_C), as shown in Figure 6, cancels out this affect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner - typically 0.05 mV at room temp.

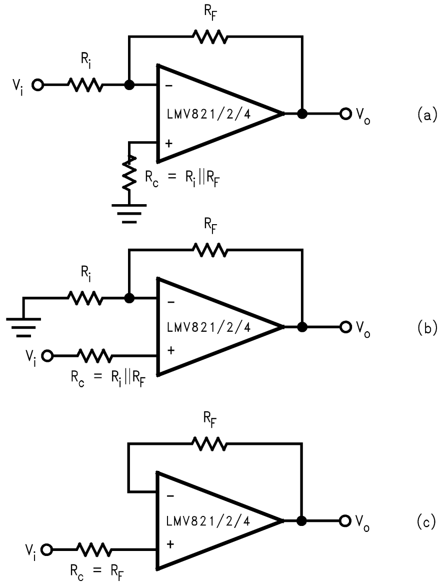


Figure 6. Canceling the Voltage Offset Effect of Input Bias Current

APPLICATION CIRCUITS

This section covers the following application circuits:

1. Telephone-Line Transceiver

2. “Simple” Mixer (Amplitude Modulator)

3. Dual Amplifier Active Filters (DAAFs)
- a. Low-Pass Filter (LPF)
- b. High-Pass Filter (HPF)

4. Tri-level Voltage Detector

TELEPHONE-LINE TRANSCEIVER

The telephone-line transceiver of Figure 7 provides a full-duplexed connection through a PCMCIA, miniature transformer. The differential configuration of receiver portion (UR), cancels reception from the transmitter portion (UT). Note that the input signals for the differential configuration of UR, are the transmit voltage (V_T) and $V_T/2$. This is because R_{match} is chosen to match the coupled telephone-line impedance; therefore dividing V_T by two (assuming R1 >> R_{match}). The differential configuration of UR has its resistors chosen to cancel the V_T and $V_T/2$ inputs according to the following equation:

$$V_0 = V_T\left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) - \frac{V_T}{2}\left(\frac{R_2}{R_1}\right) = V_T\,\frac{1}{3}\,(3) - \frac{V_T}{2}\,(2) = 0 \qquad (5)$$

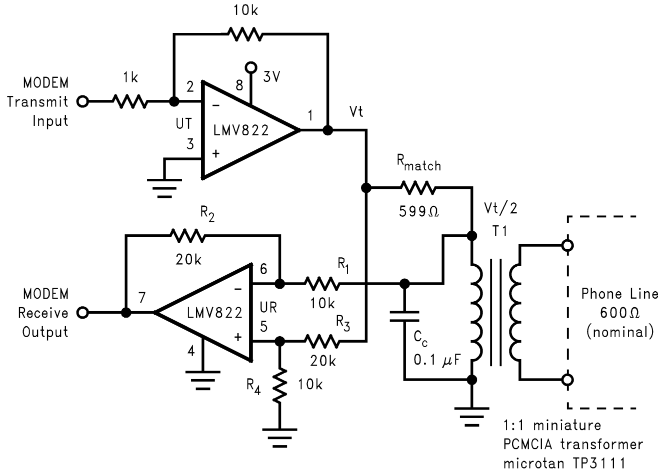


Figure 7. Telephone-line Transceiver for a PCMCIA Modem Card

Note that Cr is included for canceling out the inadequacies of the lossy, miniature transformer. Refer to application note AN-397 for detailed explanation.

“SIMPLE” MIXER (AMPLITUDE MODULATOR)

The mixer of Figure 8 is simple and provides a unique form of amplitude modulation. Vi is the modulation frequency (F_M), while a +3V square-wave at the gate of Q1, induces a carrier frequency (F_C). Q1 switches (toggles) U1 between inverting and non-inverting unity gain configurations. Offsetting a sine wave above ground at Vi results in the oscilloscope photo of Figure 9.

The simple mixer can be applied to applications that utilize the Doppler Effect to measure the velocity of an object. The difference frequency is one of its output frequency components. This difference frequency magnitude ($/F_M$-$F_C/$) is the key factor for determining an object's velocity per the Doppler Effect. If a signal is transmitted to a moving object, the reflected frequency will be a different frequency. This difference in transmit and receive frequency is directly proportional to an object's velocity.

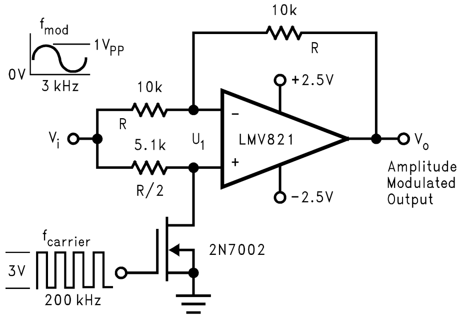


Figure 8. Amplitude Modulator Circuit

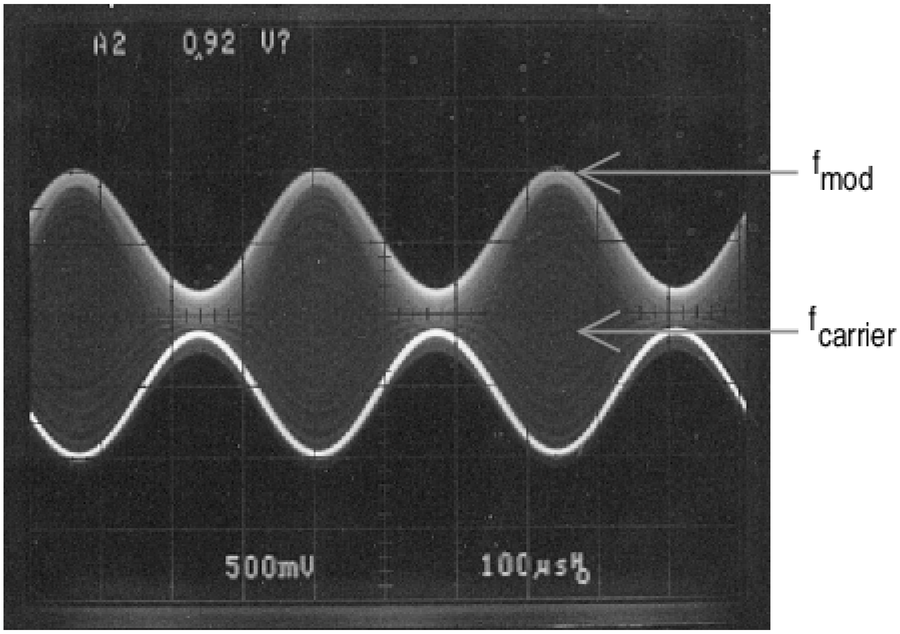


Figure 9. Output signal per the Circuit of Figure 8

DUAL AMPLIFIER ACTIVE FILTERS (DAAFs)

The LMV822/24 bring economy and performance to DAAFs. The low-pass and the high-pass filters of Figure 10 and Figure 11 (respectively), offer one key feature: excellent sensitivity performance. Good sensitivity is when deviations in component values cause relatively small deviations in a filter's parameter such as cutoff frequency (Fc). Single amplifier active filters like the Sallen-Key provide relatively poor sensitivity performance that sometimes cause problems for high production runs; their parameters are much more likely to deviate out of specification than a DAAF would. The DAAFs of Figure 10 and Figure 11 are well suited for high volume production.

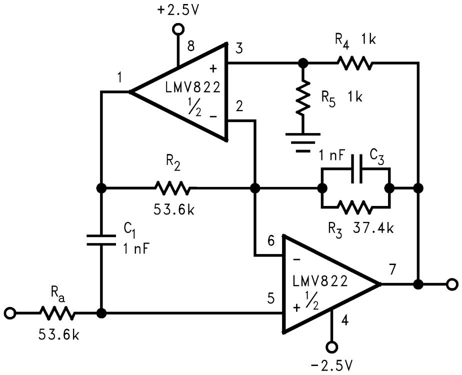


Figure 10. Dual Amplifier, 3 kHz Low-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two

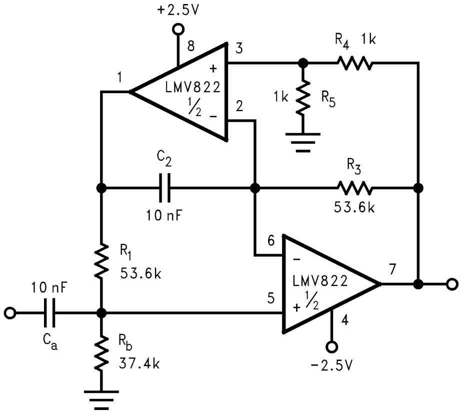


Figure 11. Dual Amplifier, 300 Hz High-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two

Table 1 provides sensitivity measurements for a 10 MΩ load condition. The left column shows the passive components for the 3 kHz low-pass DAAF. The third column shows the components for the 300 Hz high-pass DAAF. Their respective sensitivity measurements are shown to the right of each component column. Their values consists of the percent change in cutoff frequency (Fc) divided by the percent change in component value. The lower the sensitivity value, the better the performance.

Each resistor value was changed by about 10 percent, and this measured change was divided into the measured change in Fc. A positive or negative sign in front of the measured value, represents the direction Fc changes relative to components' direction of change. For example, a sensitivity value of negative 1.2, means that for a 1 percent increase in component value, Fc decreases by 1.2 percent.

Note that this information provides insight on how to fine tune the cutoff frequency, if necessary. It should be also noted that R_4 and R_5 of each circuit also caused variations in the pass band gain. Increasing R_4 by ten percent, increased the gain by 0.4 dB, while increasing R_5 by ten percent, decreased the gain by 0.4 dB.

Component (LPF)	Sensitivity (LPF)	Component (HPF)	Sensitivity (HPF)
R_a	-1.2	C_a	-0.7
C_1	-0.1	R_b	-1.0
R_2	-1.1	R_1	+0.1
R_3	+0.7	C_2	-0.1
C_3	-1.5	R_3	+0.1
R_4	-0.6	R_4	-0.1
R_5	+0.6	R_5	+0.1

Active filters are also sensitive to an op amp's parameters -Gain and Bandwidth, in particular. The LMV822/24 provide a large gain and wide bandwidth. And DAAFs make excellent use of these feature specifications.

Single Amplifier versions require a large open-loop to closed-loop gain ratio - approximately 50 to 1, at the Fc of the filter response. Figure 12 shows an impressive photograph of a network analyzer measurement (hp3577A). The measurement was taken from a 300 kHz version of Figure 10. At 300 kHz, the open-loop to closed-loop gain ratio @ Fc is about 5 to 1. This is 10 times lower than the 50 to 1 “rule of thumb” for Single Amplifier Active Filters.

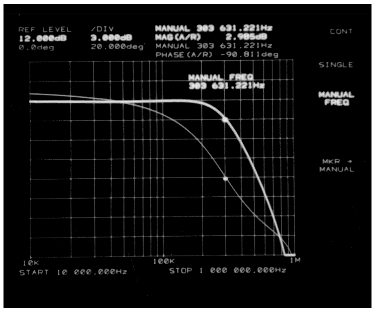


Figure 12. 300 kHz, Low-Pass Filter, Butterworth Response as Measured by the HP3577A Network Analyzer

In addition to performance, DAAFs are relatively easy to design and implement. The design equations for the low-pass and high-pass DAAFs are shown below. The first two equation calculate the Fc and the circuit Quality Factor (Q) for the LPF (Figure 10). The second two equations calculate the Fc and Q for the HPF (Figure 11).

$$\begin{aligned}
&(\text{LPF}) \quad F_C = \frac{\sqrt{R_5}}{2\pi\sqrt{R_a}\cdot\sqrt{R_2}\cdot\sqrt{R_4}\cdot\sqrt{C_1}\cdot\sqrt{C_3}} \\
&\qquad\quad\;\; Q = 2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3} \\
&(\text{HPF}) \quad F_C = \frac{\sqrt{R_4}}{2\pi\sqrt{R_1}\cdot\sqrt{R_3}\cdot\sqrt{R_5}\cdot\sqrt{C_a}\cdot\sqrt{C_2}} \\
&\qquad\quad\;\; Q = 2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}
\end{aligned} \tag{6}$$

To simplify the design process, certain components are set equal to each other. Refer to Figure 10 and Figure 11. These equal component values help to simplify the design equations as follows:

$$\begin{aligned}
&(\text{LPF}) \quad R_a = R_2 = \frac{1}{2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}} \\
&\qquad\qquad\quad R_3 = \frac{Q}{2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}} \\
&(\text{HPF}) \quad R_1 = R_3 = \frac{1}{2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}} \\
&\qquad\qquad\quad R_b = \frac{Q}{2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}}
\end{aligned} \tag{7}$$

To illustrate the design process/implementation, a 3 kHz, Butterworth response, low-pass filter DAAF (Figure 10) is designed as follows:

1. Choose $C_1 = C_3 = C = 1$ nF
2. Choose $R_4 = R_5 = 1$ kΩ
3. Calculate R_a and R_2 for the desired Fc as follows:

$$\begin{aligned}
R_a = R_2 &= \frac{1}{2\pi(F_C)C} \\
&= \frac{1}{2\pi(3\text{ kHz})1\text{nF}} \\
&= 53.1\text{ k}\Omega \\
&\cong 53.6\text{ k}\Omega\text{ (Practical Value)}
\end{aligned} \tag{8}$$

4. Calculate R_3 for the desired Q. The desired Q for a Butterworth (Maximally Flat) response is 0.707 (45 degrees into the s-plane). R_3 calculates as follows:

$$\begin{aligned}
R_3 &= \frac{Q}{2\pi(F_C)C} \\
&= \frac{0.707}{2\pi(3\text{ kHz})1\text{nF}} \\
&= 37.5\text{ k}\Omega \\
&\cong 37.4\text{ k}\Omega\text{ (Practical Value)}
\end{aligned} \tag{9}$$

Notice that R_3 could also be calculated as 0.707 of R_a or R_2.

The circuit was implemented and its cutoff frequency measured. The cutoff frequency measured at 2.92 kHz.

The circuit also showed good repeatability. Ten different LMV822 samples were placed in the circuit. The corresponding change in the cutoff frequency was less than a percent.

TRI-LEVEL VOLTAGE DETECTOR

The tri-level voltage detector of Figure 13 provides a type of window comparator function. It detects three different input voltage ranges: Min-range, Mid-range, and Max-range. The output voltage (V_O) is at V_{CC} for the Min-range. V_O is clamped at GND for the Mid-range. For the Max-range, V_O is at V_{ee}. Figure 14 shows a V_O vs. V_I oscilloscope photo per the circuit of Figure 13.

Its operation is as follows: V_I deviating from GND, causes the diode bridge to absorb I_{IN} to maintain a clamped condition (V_O= 0V). Eventually, I_{IN} reaches the bias limit of the diode bridge. When this limit is reached, the clamping effect stops and the op amp responds open loop. The design equation directly preceding Figure 14, shows how to determine the clamping range. The equation solves for the input voltage band on each side GND. The mid-range is twice this voltage band.

$$\Delta V = \frac{R}{R_1}(V_{CC} - V_{Diode})$$

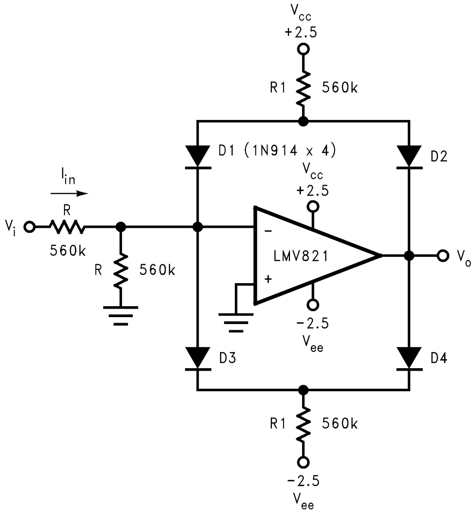


Figure 13. Tri-level Voltage Detector

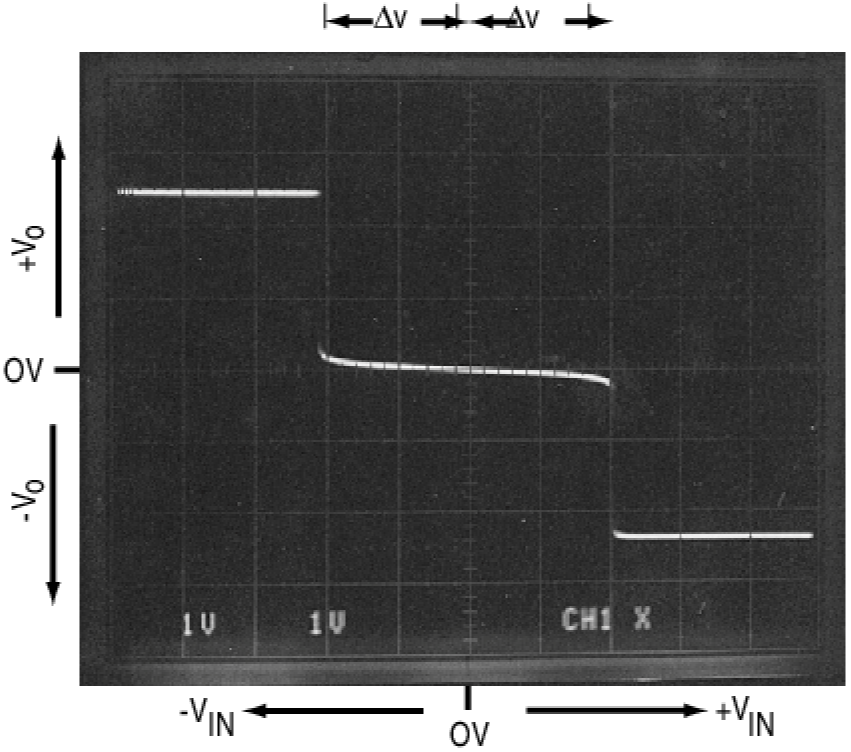


Figure 14. X, Y Oscilloscope Trace showing V_{OUT} vs V_{IN} per the Circuit of Figure 13

Connection Diagram

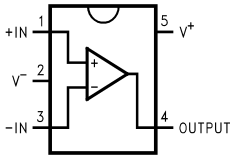


Figure 15. 5-Pin SC70-5/SOT23-5
Top View

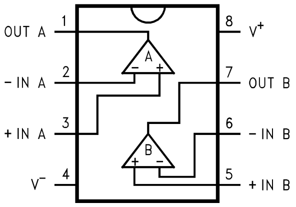


Figure 16. 8-Pin SO/MSOP
Top View

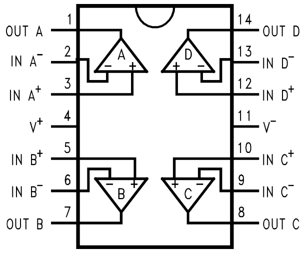


Figure 17. 14-Pin SO/TSSOP
Top View

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV821M5	ACTIVE	SOT-23	DBV	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A14	Samples
LMV821M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A14	Samples
LMV821M5X	ACTIVE	SOT-23	DBV	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A14	Samples
LMV821M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A14	Samples
LMV821M7	ACTIVE	SC70	DCK	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A15	Samples
LMV821M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A15	Samples
LMV821M7X	ACTIVE	SC70	DCK	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A15	Samples
LMV821M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A15	Samples
LMV822M	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMV 822M	Samples
LMV822M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV 822M	Samples
LMV822MM	ACTIVE	VSSOP	DGK	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	V822	Samples
LMV822MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	V822	Samples
LMV822MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	V822	Samples
LMV822MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	V822	Samples
LMV822MX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMV 822M	Samples
LMV822MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV 822M	Samples
LMV824M	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMV824M	Samples
LMV824M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV824M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV824MT	ACTIVE	TSSOP	PW	14	94	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	LMV824 MT	Samples
LMV824MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV824 MT	Samples
LMV824MTX	ACTIVE	TSSOP	PW	14	2500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	LMV824 MT	Samples
LMV824MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV824 MT	Samples
LMV824MX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMV824M	Samples
LMV824MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV824M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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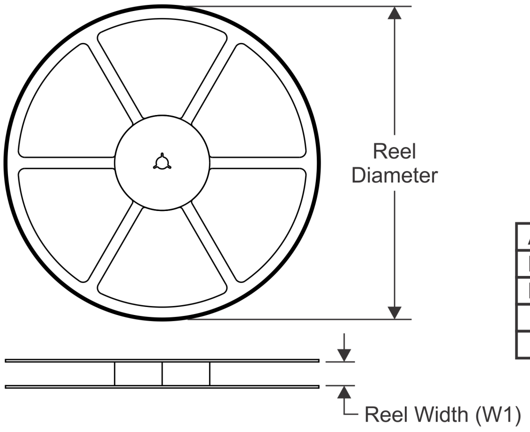
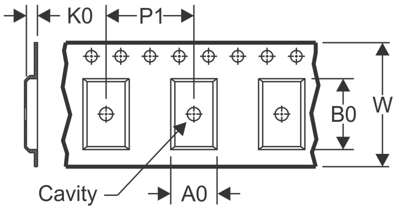
TAPE AND REEL INFORMATION

REEL DIMENSIONS

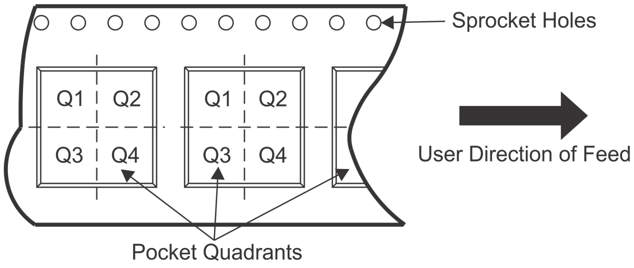


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

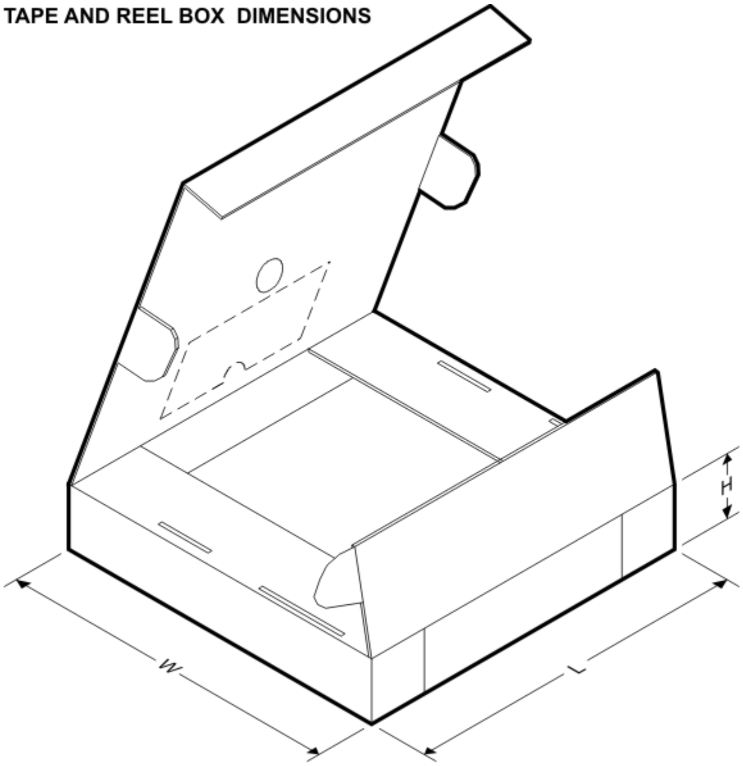
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV821M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV821M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV821M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV821M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV822MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV822MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV824MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMV824MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMV824MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV824MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

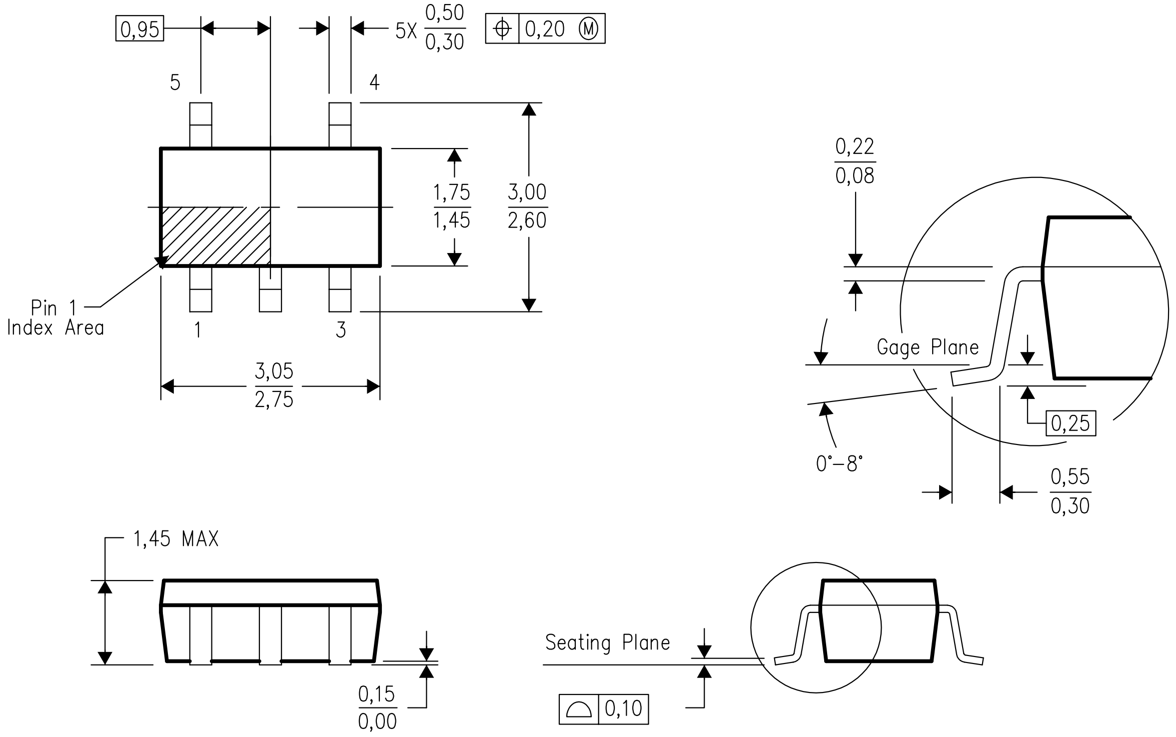
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV821M5	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV821M5/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV821M5X	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV821M5X/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV821M7	SC70	DCK	5	1000	203.0	190.0	41.0
LMV821M7/NOPB	SC70	DCK	5	1000	203.0	190.0	41.0
LMV821M7X	SC70	DCK	5	3000	206.0	191.0	90.0
LMV821M7X/NOPB	SC70	DCK	5	3000	206.0	191.0	90.0
LMV822MM	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV822MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV822MMX	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMV822MMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMV822MX	SOIC	D	8	2500	349.0	337.0	45.0
LMV822MX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMV824MTX	TSSOP	PW	14	2500	349.0	337.0	45.0
LMV824MTX/NOPB	TSSOP	PW	14	2500	349.0	337.0	45.0
LMV824MX	SOIC	D	14	2500	349.0	337.0	45.0
LMV824MX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0

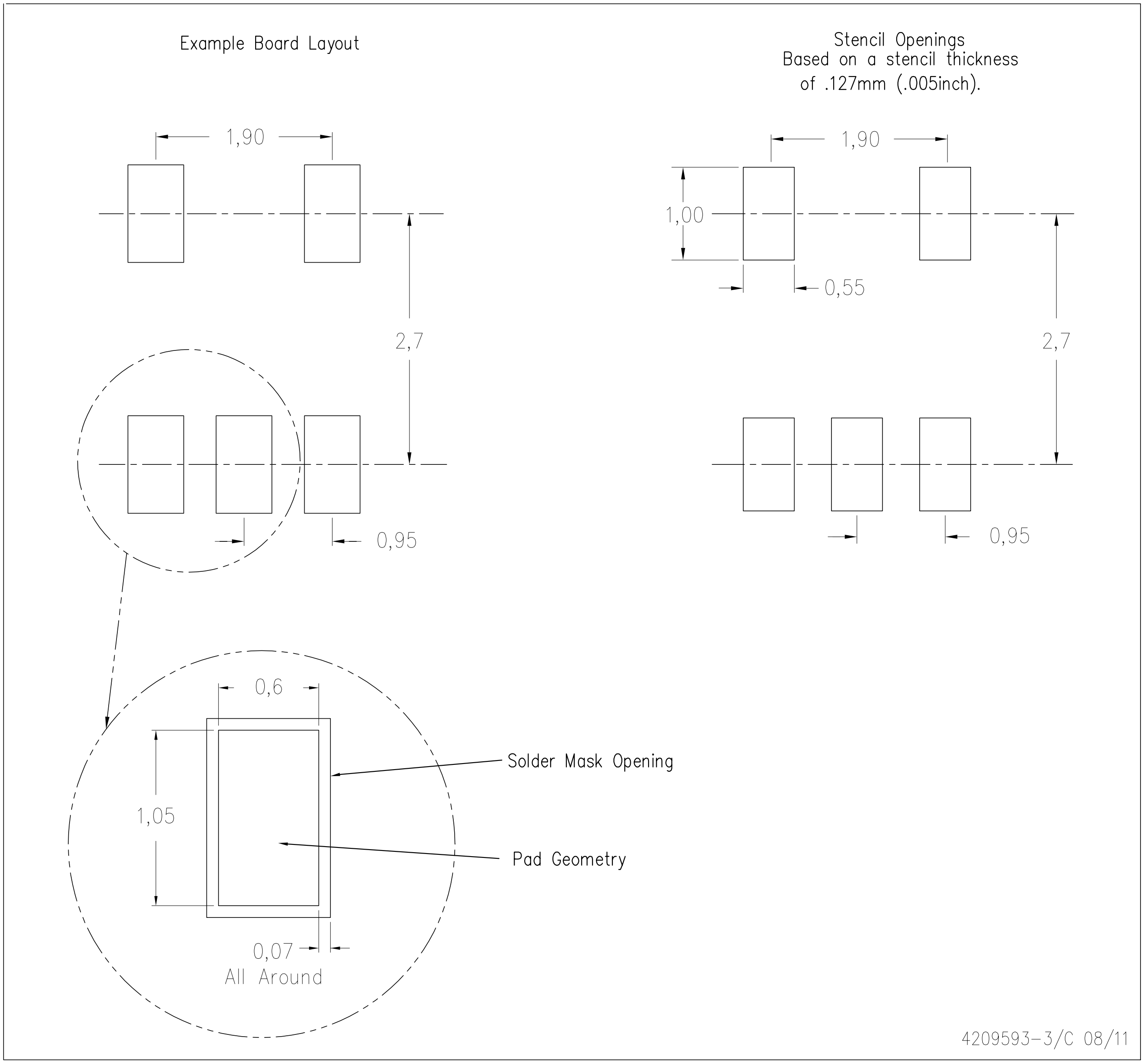
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

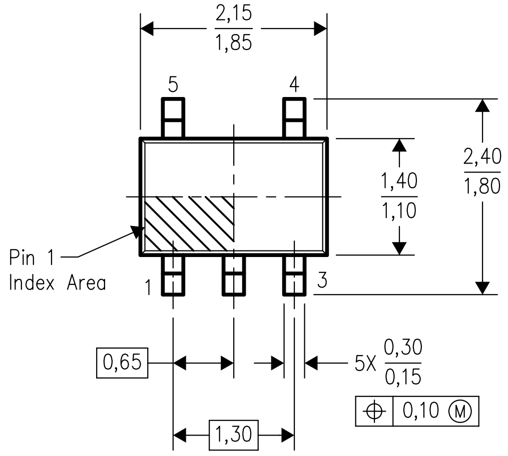
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–178 Variation AA.

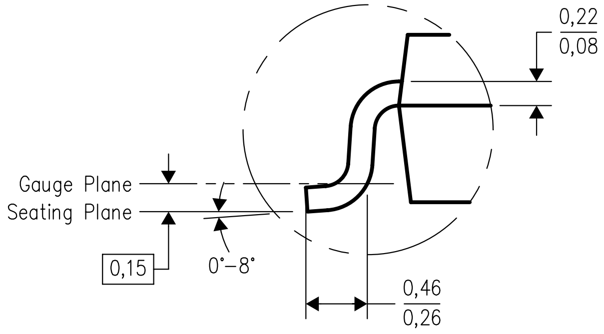
DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE

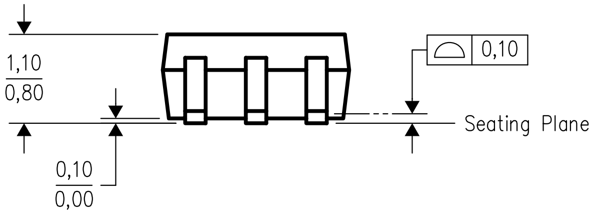


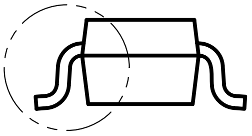
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE





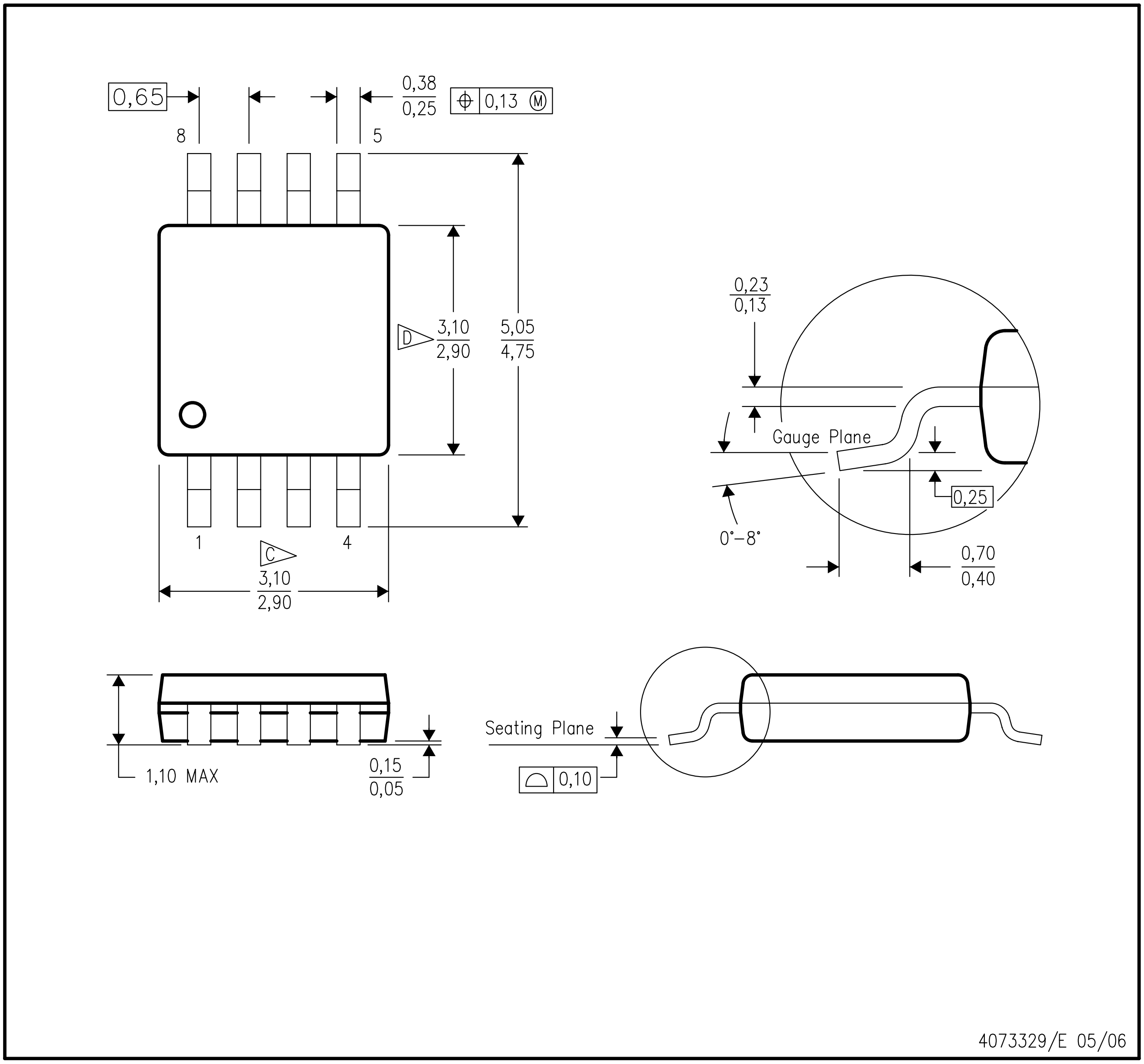




4093553-3/G 01/2007

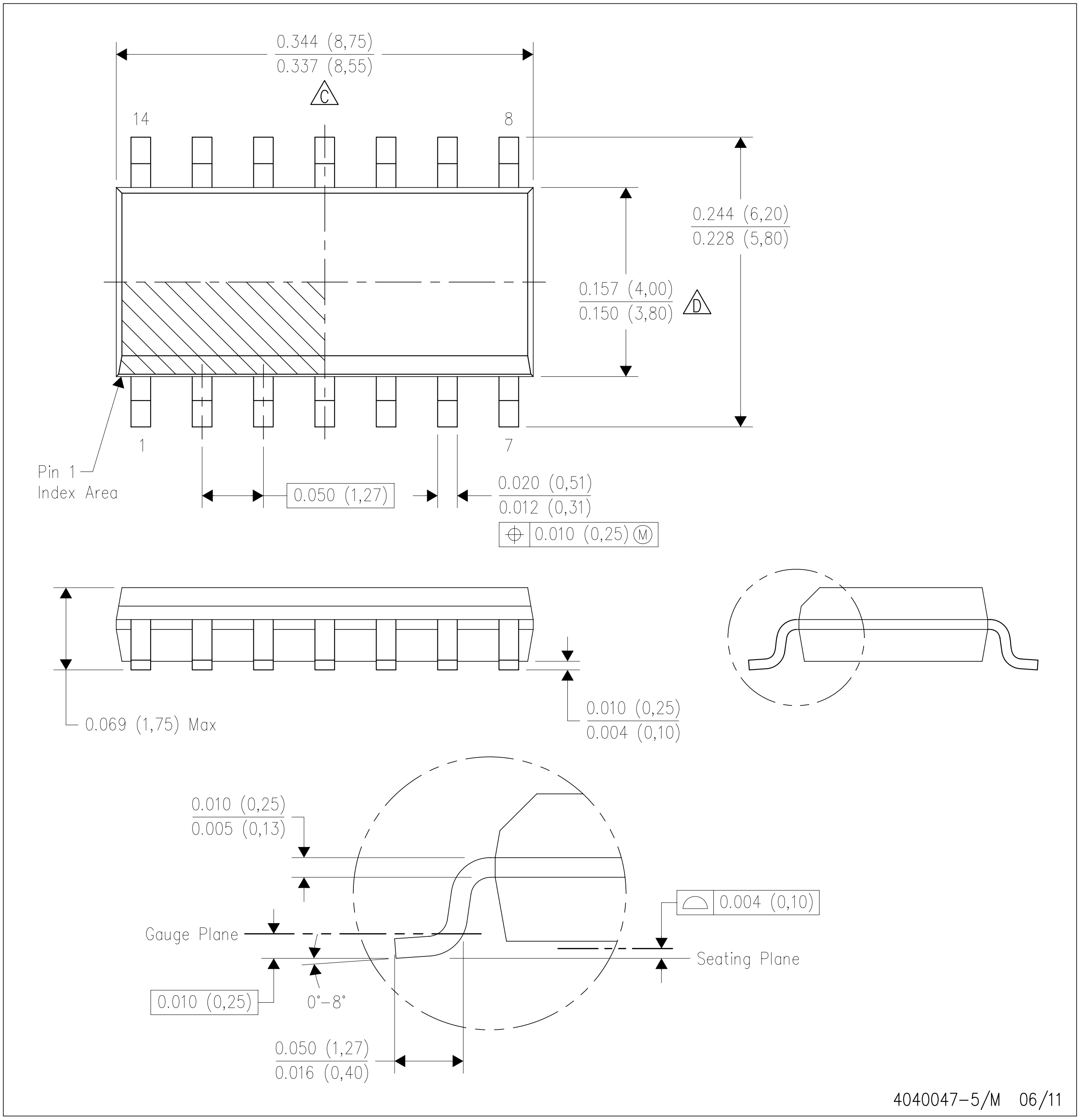
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



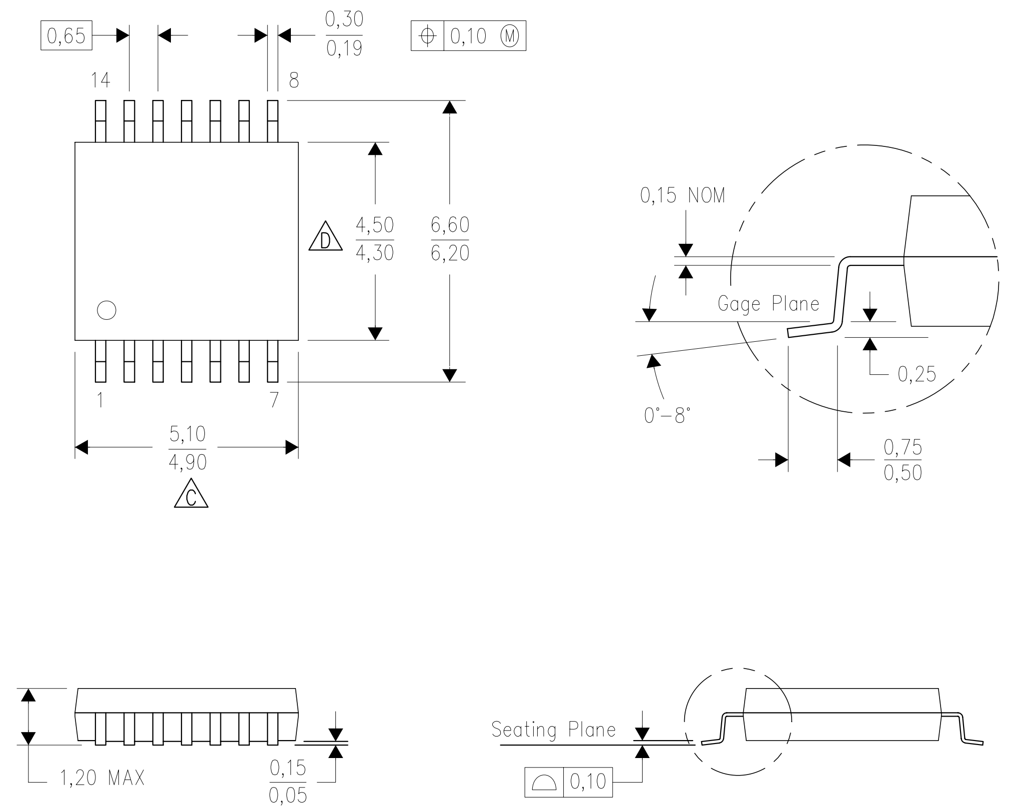
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

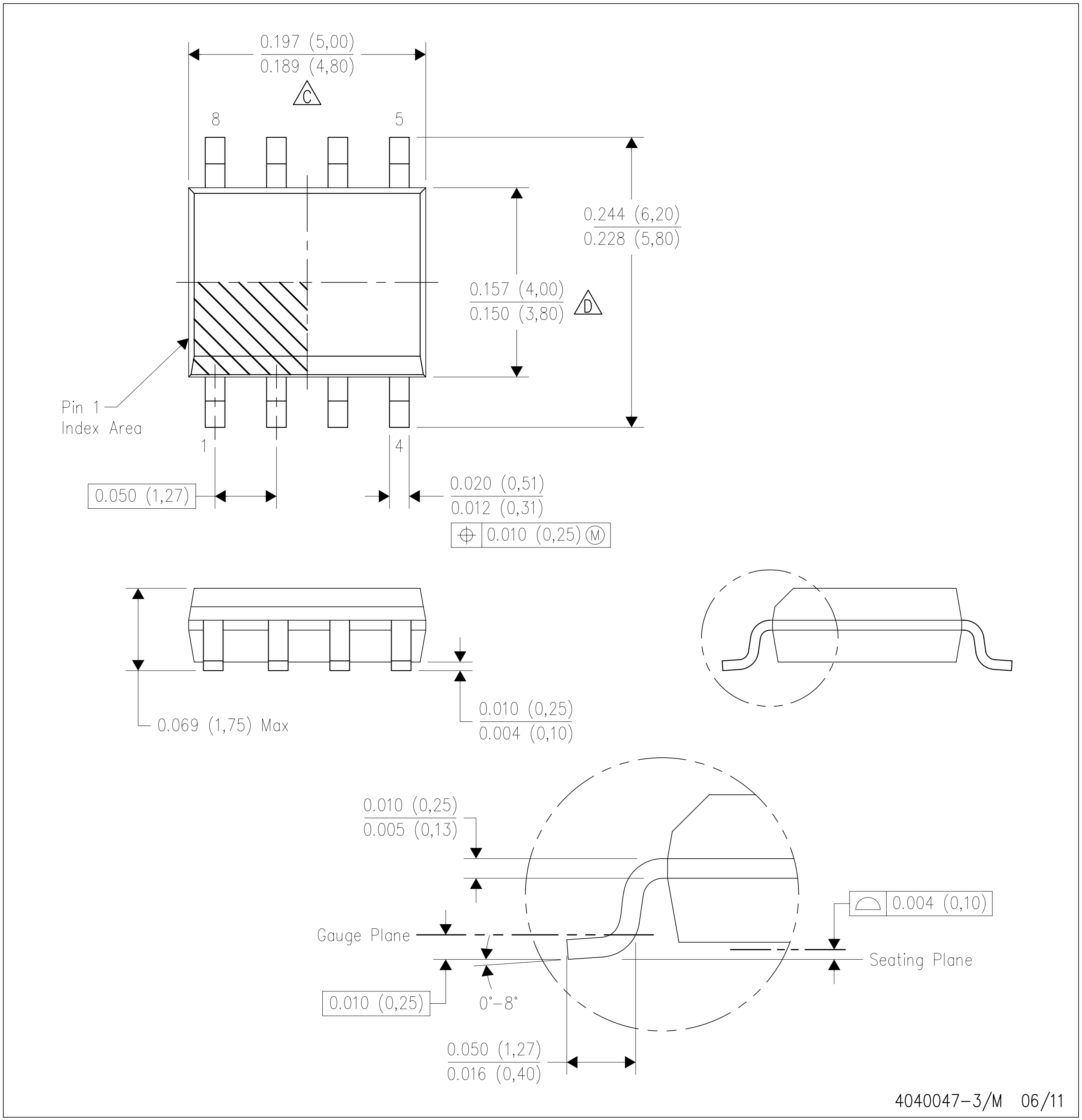
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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