

# LMR33620 SIMPLE SWITCHER® 3.8-V to 36-V, 2-A Synchronous Step-Down Voltage Converter

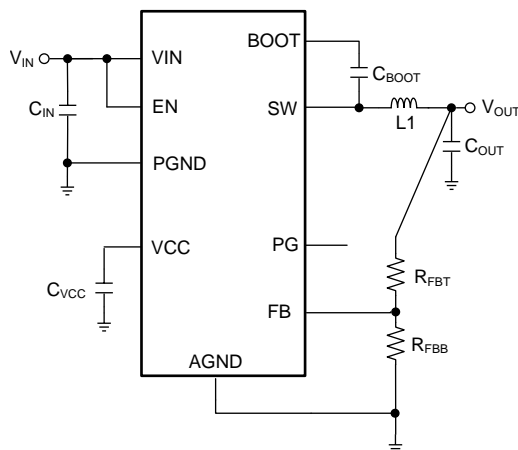
## 1 Features

- Configured for Rugged Industrial Applications
  - Input Voltage Range: 3.8 V to 36 V
  - Output Voltage Range: 1 V to 24 V
  - Output Current: 2 A
  - 75 mΩ/50 mΩ Low  $R_{DS-ON}$  Power MOSFETs
  - Peak-Current-Mode Control
  - Short Minimum On-Time of 68 ns
  - Frequency: 400 kHz, 1.4 MHz, 2.1 MHz
  - Junction Temperature Range  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
  - Integrated Synchronous Rectification
  - Integrated Compensation Network
- High Efficiency Solution
  - Peak Efficiency > 95%
  - Low Shutdown Quiescent Current of 5  $\mu\text{A}$
  - Low Operating Quiescent Current of 25  $\mu\text{A}$
- Flexible System Interface
  - Power-Good Flag and Precision Enable
- Create a Custom Design Using the LMR33620 with the [WEBENCH® Power Designer](#)

## 2 Applications

- Motor Drive Systems: Drones, AC Inverters, VF Drives, Servos
- Factory and Building Automation Systems: PLC CPU, HVAC Control, Elevator Control
- General Purpose Wide  $V_{IN}$  Power Supplies

### Simplified Schematic



## 3 Description

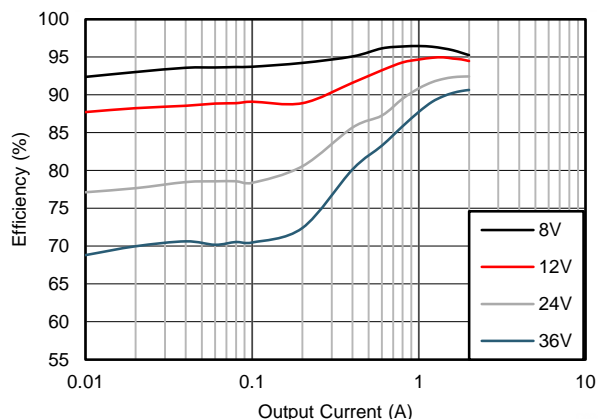
The LMR33620 SIMPLE SWITCHER® regulator is an easy-to-use, synchronous, step-down DC/DC converter that delivers best-in-class efficiency for rugged industrial applications. The LMR33620 is capable of driving up to 2 A of load current from an input of up to 36 V. The LMR33620 provides high light load efficiency and output accuracy in a very small solution size. Features such as a power-good flag and precision enable provide both flexible and easy-to-use solutions for a wide range of applications. The LMR33620 automatically folds back frequency at light load to improve efficiency. Integration eliminates most external components and provides a pinout designed for simple PCB layout. Protection features include thermal shutdown, input undervoltage lockout, cycle-by-cycle current limit, and hiccup short-circuit protection. The LMR33620 is available in an 8-pin HSOIC package and in a 12-pin 3 mm × 2 mm VQFN package with wettable flanks.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMR33620	HSOIC (8)	5.00 mm × 4.00 mm
LMR33620	VQFN (12)	3.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Efficiency vs Output Current $V_{OUT} = 5\text{ V}$ , 400 kHz, VQFN



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.4 Device Functional Modes.....	<b>16</b>
<b>2 Applications</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>20</b>
<b>3 Description</b> .....	<b>1</b>	9.1 Application Information.....	<b>20</b>
<b>4 Revision History</b> .....	<b>2</b>	9.2 Typical Application .....	<b>20</b>
<b>5 Device Comparison Table</b> .....	<b>3</b>	9.3 Do's and Don'ts.....	<b>32</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Power Supply Recommendations</b> .....	<b>33</b>
<b>7 Specifications</b> .....	<b>5</b>	<b>11 Layout</b> .....	<b>34</b>
7.1 Absolute Maximum Ratings .....	<b>5</b>	11.1 Layout Guidelines .....	<b>34</b>
7.2 ESD Ratings.....	<b>5</b>	11.2 Layout Example .....	<b>36</b>
7.3 Recommended Operating Conditions .....	<b>5</b>	<b>12 Device and Documentation Support</b> .....	<b>38</b>
7.4 Thermal Information .....	<b>6</b>	12.1 Device Support .....	<b>38</b>
7.5 Electrical Characteristics.....	<b>6</b>	12.2 Documentation Support .....	<b>38</b>
7.6 Timing Characteristics.....	<b>8</b>	12.3 Receiving Notification of Documentation Updates	<b>38</b>
7.7 System Characteristics .....	<b>9</b>	12.4 Community Resources.....	<b>38</b>
7.8 Typical Characteristics.....	<b>10</b>	12.5 Trademarks .....	<b>39</b>
<b>8 Detailed Description</b> .....	<b>11</b>	12.6 Electrostatic Discharge Caution.....	<b>39</b>
8.1 Overview .....	<b>11</b>	12.7 Glossary .....	<b>39</b>
8.2 Functional Block Diagram .....	<b>11</b>	<b>13 Mechanical, Packaging, and Orderable</b>	
8.3 Feature Description.....	<b>12</b>	<b>Information</b> .....	<b>39</b>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

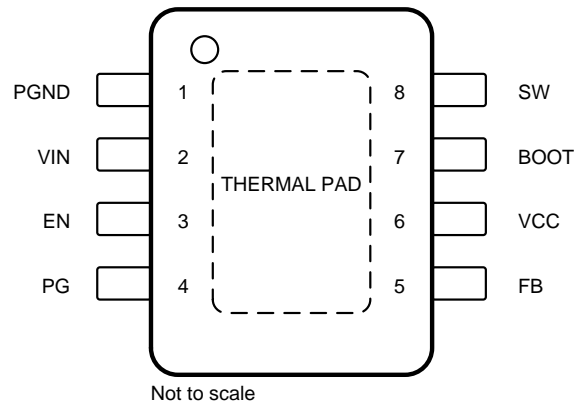
<b>Changes from Original (February 2018) to Revision A</b>	<b>Page</b>
• Added WSON information throughout data sheet.....	<b>1</b>

## 5 Device Comparison Table

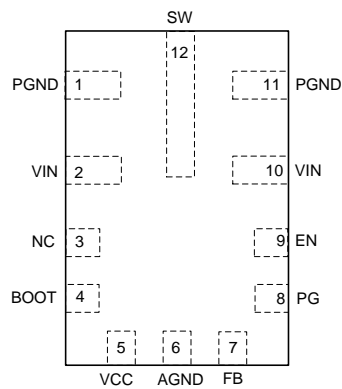
DEVICE NUMBER	PACKAGE	FREQUENCY	RATED CURRENT	OUTPUT VOLTAGE
LMR33620ADDA	DDA (8-pin HSOIC) 5.0 × 4.0 mm	400 kHz	2 A	Adjustable
LMR33620BDDA		1400 kHz	2 A	
LMR33620CDDA		2100 kHz	2 A	
LMR33620ARNX	RNX (12-pin VQFN) 3.0 × 2.0 × 0.85 mm	400 kHz	2 A	Adjustable
LMR33620BRNX		1400 kHz	2 A	
LMR33620CRNX		2100 kHz	2 A	

## 6 Pin Configuration and Functions

**DDA Package  
8-Pin HSOIC With PowerPAD™  
Top View**



**RNX Package  
12-Pin VQFN  
Top View**



### Pin Functions

PIN			TYPE	DESCRIPTION
HSOIC	VQFN	NAME		
1	1,11	PGND	G	Power ground terminal. Connect to system ground and AGND. Connect to C <sub>IN</sub> with short wide traces.
2	2,10	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor(s) directly to this pin and PGND.
3	9	EN	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; DO NOT FLOAT.
4	8	PG	A	Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Flag pulls low when EN = Low. Can be open or grounded when not used.
5	7	FB	A	Feedback input to regulator. Connect to tap point of feedback voltage divider. DO NOT FLOAT. DO NOT GROUND.
6	5	VCC	P	Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high quality 1-μF capacitor from this pin to GND.
7	4	BOOT	P	Boot-strap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. On the VQFN package connect the SW pin to NC on the PCB. This simplifies the connection from the C <sub>BOOT</sub> capacitor to the SW pin.
8	12	SW	P	Regulator switch node. Connect to power inductor. On the VQFN package connect the SW pin to NC on the PCB. This simplifies the connection from the C <sub>BOOT</sub> capacitor to the SW pin.
THERMAL PAD	6	AGND	G	Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB. For the HSOIC package, the pad on the bottom of the device serves as both the AGND connection and a thermal connection to the heat sink ground plane. This pad must be soldered to a ground plane to achieve good electrical and thermal performance.
—	3	NC	—	On the VQFN package the SW pin must be connected to NC on the PCB. This simplifies the connection from the C <sub>BOOT</sub> capacitor to the SW pin. This pin has no internal connection to the regulator.

A = Analog, P = Power, G = Ground

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range<sup>(1)</sup>

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to PGND	-0.3	38	V
	EN to AGND <sup>(2)</sup>	-0.3	V <sub>IN</sub> + 0.3	
	FB to AGND	-0.3	5.5	
	PG to AGND <sup>(2)</sup>	0	22	
	AGND to PGND	-0.3	0.3	
	SW to PGND	-0.3	V <sub>IN</sub> + 0.3	V
	SW to PGND less than 100-ns transients	-3.5	38	
	BOOT to SW	-0.3	5.5	
	VCC to AGND <sup>(3)</sup>	-0.3	5.5	
T <sub>J</sub>	Junction temperature <sup>(4)</sup>	-40	150	°C
T <sub>stg</sub>	Storage temperature	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V
- (3) Under some operating conditions the VCC LDO voltage may increase beyond 5.5V.
- (4) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM) <sup>(1)</sup>	±2500
		Charged-device model (CDM) <sup>(2)</sup>	±750

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40 °C to 125 °C (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage	VIN to PGND	3.8	36	V
	EN <sup>(2)</sup>	0	V <sub>IN</sub>	
	PG <sup>(2)</sup>	0	18	
Adjustable output voltage	V <sub>OUT</sub> <sup>(3)</sup>	1	24	V
Output current	I <sub>OUT</sub>	0	2	A
Temperature	Operating junction temperature, T <sub>J</sub> <sup>(4)</sup>	-40	125	°C

- (1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see [Electrical Characteristics](#).
- (2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
- (3) The maximum output voltage can be extended to 95% of V<sub>IN</sub>; contact TI for details. Under no conditions should the output voltage be allowed to fall below zero volts.
- (4) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1) (2)</sup>		LMR336x0		UNIT
		DDA (HSOIC)	RNX (VQFN)	
		8 PINS	12 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	42.9	72.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	54	35.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	13.6	23.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	4.3	0.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	13.8	23.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	4.3	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The value of R<sub>θJA</sub> given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature*.

## 7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T<sub>J</sub>) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T<sub>J</sub> = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V<sub>IN</sub> = 12 V, V<sub>EN</sub> = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY VOLTAGE</b>						
V <sub>IN</sub>	Minimum operating input voltage				3.8	V
I <sub>Q</sub>	Non-switching input current; measured at VIN pin <sup>(1)</sup>	V <sub>FB</sub> = 1.2 V		24	34	μA
I <sub>SD</sub>	Shutdown quiescent current; measured at VIN pin	EN = 0		5	10	μA
<b>ENABLE</b>						
V <sub>EN-VCC-H</sub>	EN input level required to turn on internal LDO	Rising threshold			1	V
V <sub>EN-VCC-L</sub>	EN input level required to turn off internal LDO	Falling threshold	0.3			V
V <sub>EN-H</sub>	EN input level required to start switching	Rising threshold	1.2	1.231	1.26	V
V <sub>EN-HYS</sub>	Hysteresis below V <sub>EN-H</sub>	Hysteresis below V <sub>EN-H</sub> ; falling		100		mV
I <sub>LKG-EN</sub>	Enable input leakage current	V <sub>EN</sub> = 3.3 V		0.2		nA
<b>INTERNAL SUPPLIES</b>						
V <sub>CC</sub>	Internal LDO output voltage appearing at the VCC pin	6 V ≤ V <sub>IN</sub> ≤ 36 V	4.75	5	5.25	V
V <sub>BOOT-UVLO</sub>	Bootstrap voltage undervoltage lock-out threshold <sup>(2)</sup>			2.2		V
<b>VOLTAGE REFERENCE (FB PIN)</b>						
V <sub>FB</sub>	Feedback voltage; ADJ option		0.985	1	1.015	V
I <sub>FB</sub>	Current into FB pin; ADJ option	FB = 1 V		0.2	50	nA

(1) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.

(2) When the voltage across the C<sub>BOOT</sub> capacitor falls below this voltage, the low side MOSFET is turned on to recharge C<sub>BOOT</sub>.

## Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature ( $T_J$ ) range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}\text{C}$ , and are provided for reference purposes only. Unless otherwise stated, the following conditions apply:  $V_{IN} = 12\text{ V}$ ,  $V_{EN} = 4\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CURRENT LIMITS<sup>(3)</sup></b>						
$I_{SC}$	High-side current limit	LMR33620	2.9	3.5	4	A
$I_{LIMIT}$	Low-side current limit	LMR33620	1.95	2.45	2.9	A
$I_{PEAK-MIN}$	Minimum peak inductor current	LMR33620		0.65		A
$I_{ZC}$	Zero current detector threshold			0.01		A
<b>SOFT START</b>						
$t_{SS}$	Internal soft-start time		2.9	4	6	ms
<b>POWER GOOD (PG PIN)</b>						
$V_{PG-HIGH-UP}$	Power-good upper threshold - rising	% of FB voltage	105%	107%	110%	
$V_{PG-HIGH-DN}$	Power-good upper threshold - falling	% of FB voltage	103%	105%	108%	
$V_{PG-LOW-UP}$	Power-good lower threshold - rising	% of FB voltage	92%	94%	97%	
$V_{PG-LOW-DN}$	Power-good lower threshold - falling	% of FB voltage	90%	92%	95%	
$t_{PG}$	Power-good glitch filter delay <sup>(4)</sup>		60		170	$\mu\text{s}$
$R_{PG}$	Power-good flag $R_{DSON}$	$V_{IN} = 12\text{ V}$ , $V_{EN} = 4\text{ V}$		76	150	$\Omega$
		$V_{EN} = 0\text{ V}$		35	60	
$V_{IN-PG}$	Minimum input voltage for proper PG function	50- $\mu\text{A}$ , $EN = 0\text{ V}$			2	V
$V_{PG}$	PG logic low output	50- $\mu\text{A}$ , $EN = 0\text{ V}$ , $V_{IN} = 2\text{ V}$			0.2	V
<b>OSCILLATOR</b>						
$f_{SW}$	Switching frequency	"A" Version	340	400	460	kHz
$f_{SW}$	Switching frequency	"B" Version	1.2	1.4	1.6	MHz
$f_{SW}$	Switching frequency	"C" Version, DDA package	1.8	2.1	2.4	MHz
$f_{SW}$	Switching frequency	"C" Version, RNX package	1.8	2.1	2.3	MHz

(3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

(4) See *Power-Good Flag Output* for details.

## Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature ( $T_J$ ) range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}\text{C}$ , and are provided for reference purposes only. Unless otherwise stated, the following conditions apply:  $V_{IN} = 12\text{ V}$ ,  $V_{EN} = 4\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>MOSFETS</b>						
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	RNX package		75	145	m $\Omega$
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	DDA package		95	160	m $\Omega$
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	RNX package		50	95	m $\Omega$
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	DDA package		66	110	m $\Omega$

## 7.6 Timing Characteristics

Limits apply over the recommended operating junction temperature ( $T_J$ ) range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}\text{C}$ , and are provided for reference purposes only. Unless otherwise stated, the following conditions apply:  $V_{IN} = 12\text{ V}$ ,  $V_{EN} = 4\text{ V}$ .

			MIN	NOM	MAX	UNIT
$t_{ON-MIN}$	Minimum switch on-time	RNX package		68	80	ns
$t_{ON-MIN}$	Minimum switch on-time	DDA package		75	108	ns
$t_{OFF-MIN}$	Minimum switch off-time	RNX package		52	70	ns
$t_{OFF-MIN}$	Minimum switch off-time	DDA package		50	85	ns
$t_{ON-MAX}$	Maximum switch on-time			7	9	$\mu\text{s}$

## 7.7 System Characteristics

The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to  $T_J = 25^\circ\text{C}$  only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ . *These specifications are not ensured by production testing.*

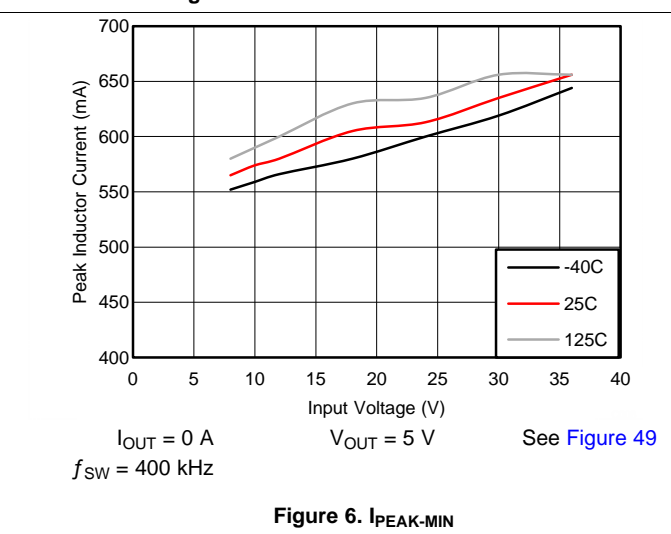
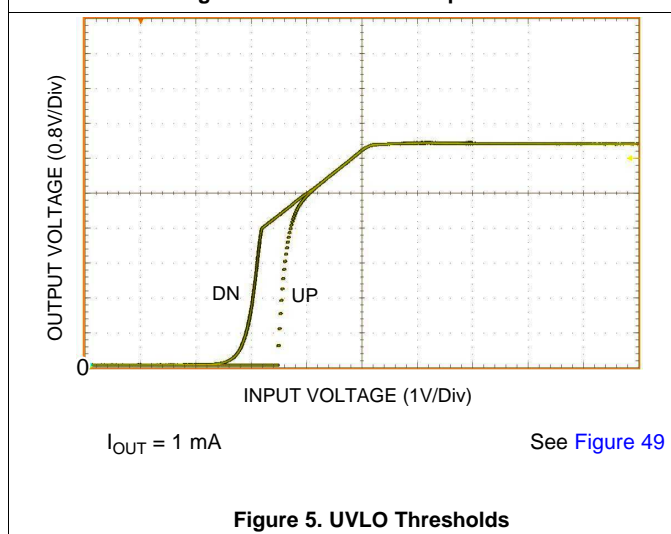
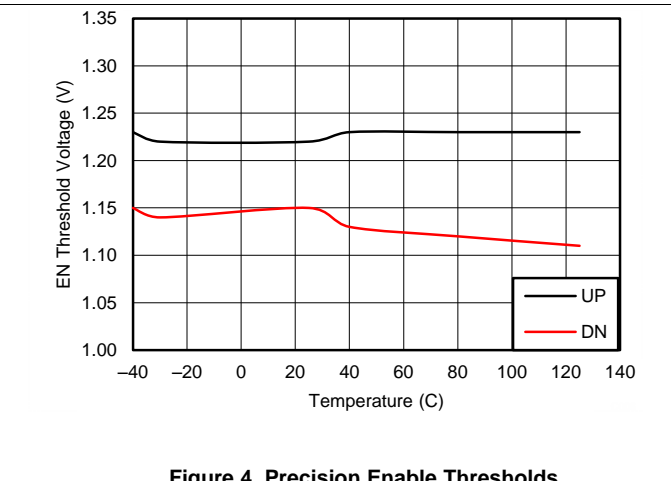
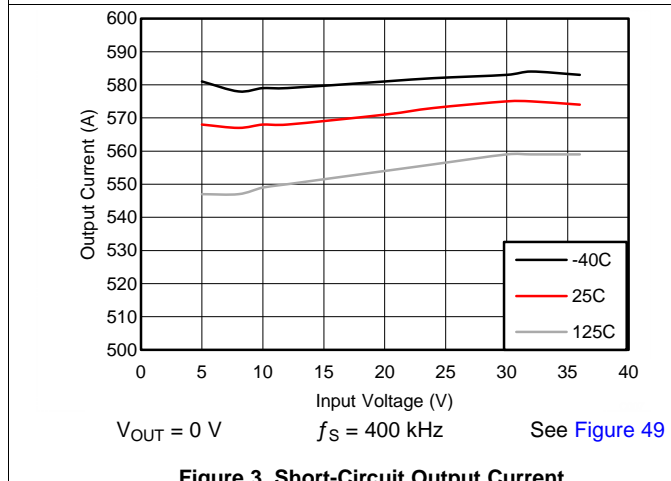
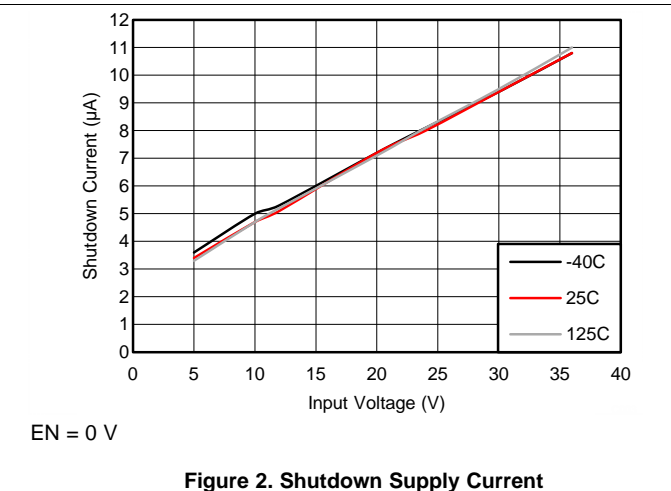
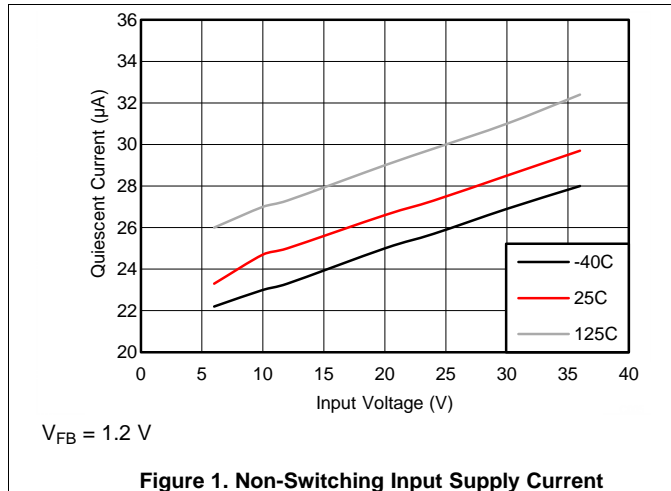
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Operating input voltage range	$V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 0\text{ A}$	3.8		36	V
$V_{OUT}$	Output voltage regulation for $V_{OUT} = 5\text{ V}^{(1)}$	$V_{OUT} = 5\text{ V}$ , $V_{IN} = 7\text{ V to } 36\text{ V}$ , $I_{OUT} = 0\text{ A}$ to max. load	-1.5%		2.5%	
		$V_{OUT} = 5\text{ V}$ , $V_{IN} = 7\text{ V to } 36\text{ V}$ , $I_{OUT} = 1\text{ A}$ to max. load	-1.5%		1.5%	
	Output voltage regulation for $V_{OUT} = 3.3\text{ V}^{(1)}$	$V_{OUT} = 3.3\text{ V}$ , $V_{IN} = 3.8\text{ V to } 36\text{ V}$ , $I_{OUT} = 0\text{ A}$ to max. load	-1.5%		2.5%	
		$V_{OUT} = 3.3\text{ V}$ , $V_{IN} = 3.8\text{ V to } 36\text{ V}$ , $I_{OUT} = 1\text{ A}$ to max. load	-1.5%		1.5%	
$I_{SUPPLY}$	Input supply current when in regulation	$V_{IN} = 12\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 0\text{ A}$ , $R_{FBT} = 1\text{ M}\Omega$		25		$\mu\text{A}$
$V_{DROP}$	Dropout voltage; ( $V_{IN} - V_{OUT}$ )	$V_{OUT} = 5\text{ V}$ , $I_{OUT} = 1\text{ A}$ Dropout at -1% of regulation, $f_{SW} = 140\text{ kHz}$		150		mV
$D_{MAX}$	Maximum switch duty cycle <sup>(2)</sup>	$V_{IN} = V_{OUT} = 12\text{ V}$ , $I_{OUT} = 1\text{ A}$		98%		
$V_{HC}$	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
$t_{HC}$	Time between current-limit hiccup burst			94		ms
$t_D$	Switch voltage dead time			2		ns
$T_{SD}$	Thermal shutdown temperature	Shutdown temperature		165		$^\circ\text{C}$
		Recovery temperature		148		$^\circ\text{C}$

(1) Deviation is with respect to  $V_{IN} = 12\text{ V}$ ,  $I_{OUT} = 1\text{ A}$ .

(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately:  $f_{MIN} = 1 / (t_{ON-MAX} + t_{OFF-MIN})$ .  $D_{MAX} = t_{ON-MAX} / (t_{ON-MAX} + t_{OFF-MIN})$ .

## 7.8 Typical Characteristics

Unless otherwise specified the following conditions apply:  $T_A = 25^\circ\text{C}$  and  $V_{IN} = 12\text{ V}$

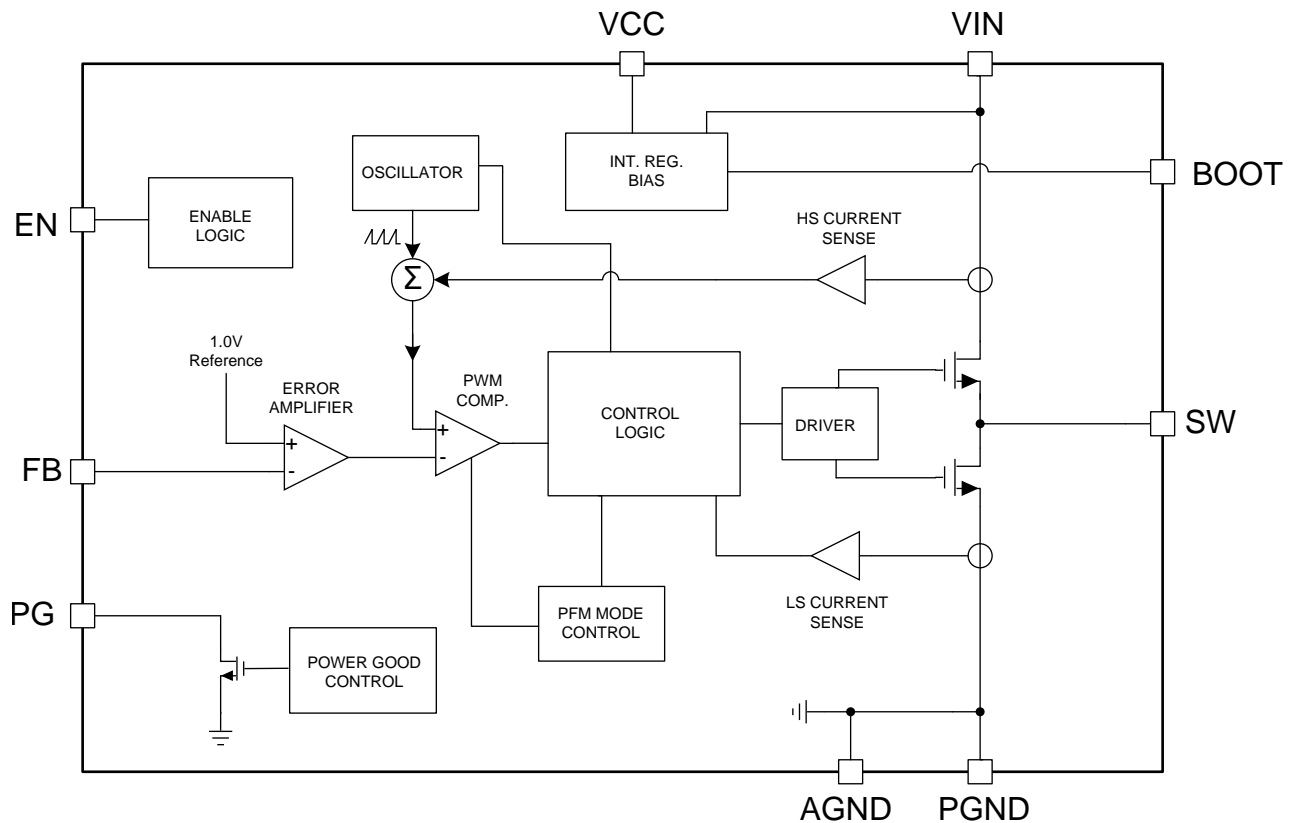


## 8 Detailed Description

### 8.1 Overview

The LMR33620 is a synchronous peak-current-mode buck regulator designed for a wide variety of industrial applications. The regulator automatically switches modes between PFM and PWM depending on load. At heavy load, the device operates in PWM at a constant switching frequency. At light loads the mode changes to PFM, with diode emulation allowing DCM. This reduces the input supply current and keeps efficiency high. The device features internal loop compensation which reduces design time and requires fewer external components than externally compensated regulators.

### 8.2 Functional Block Diagram



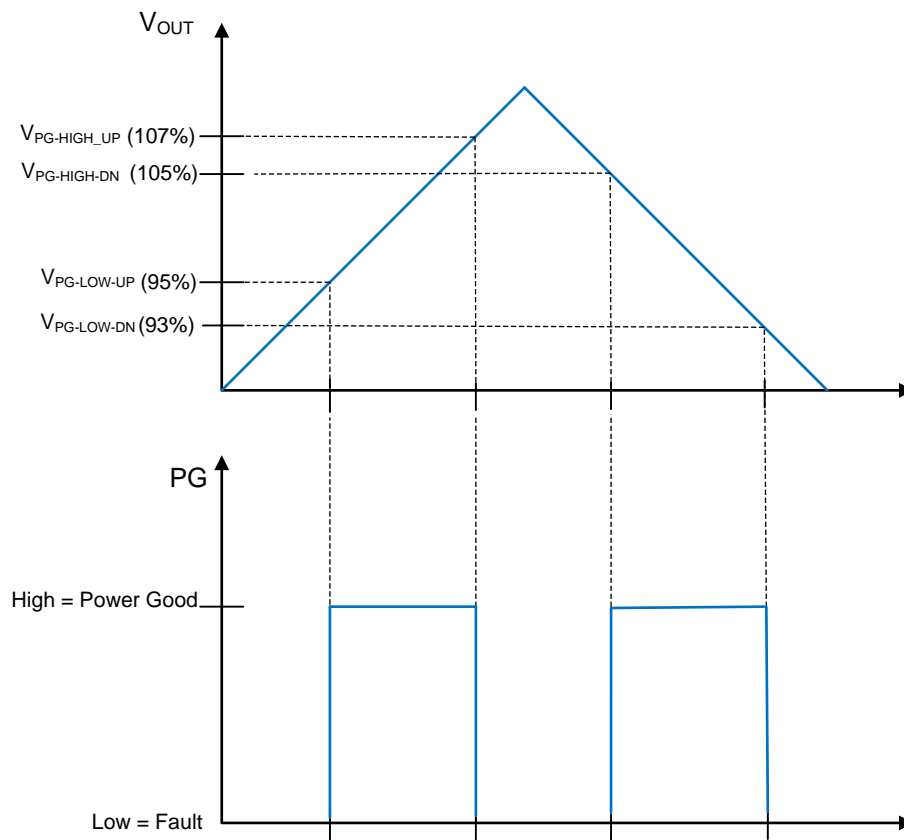
Copyright © 2017, Texas Instruments Incorporated

## 8.3 Feature Description

### 8.3.1 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR33620 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. The timing parameters of the glitch filter are found in the [Electrical Characteristics](#) table. Output voltage excursions lasting less than  $t_{PG}$  do not trip the power-good flag. Power-good operation can best be understood by reference to [Figure 7](#) and [Figure 8](#). Note that during initial power-up a delay of about 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

The power-good output consists of an open drain NMOS; requiring an external pull up resistor to a suitable logic supply. It can also be pulled up to either VCC or V<sub>OUT</sub>, through a 100-kΩ resistor, as desired. If this function is not needed, the PG pin should be left floating. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ≥ 2 V (typical). Limit the current into the power-good flag pin to less than 5 mA D.C. The maximum current is internally limited to about 35 mA when the device is enabled and about 65 mA when the device is disabled. The internal current limit protects the device from any transient currents that may occur when discharging a filter capacitor connected to this output.



**Figure 7. Static Power-Good Operation**

Feature Description (continued)

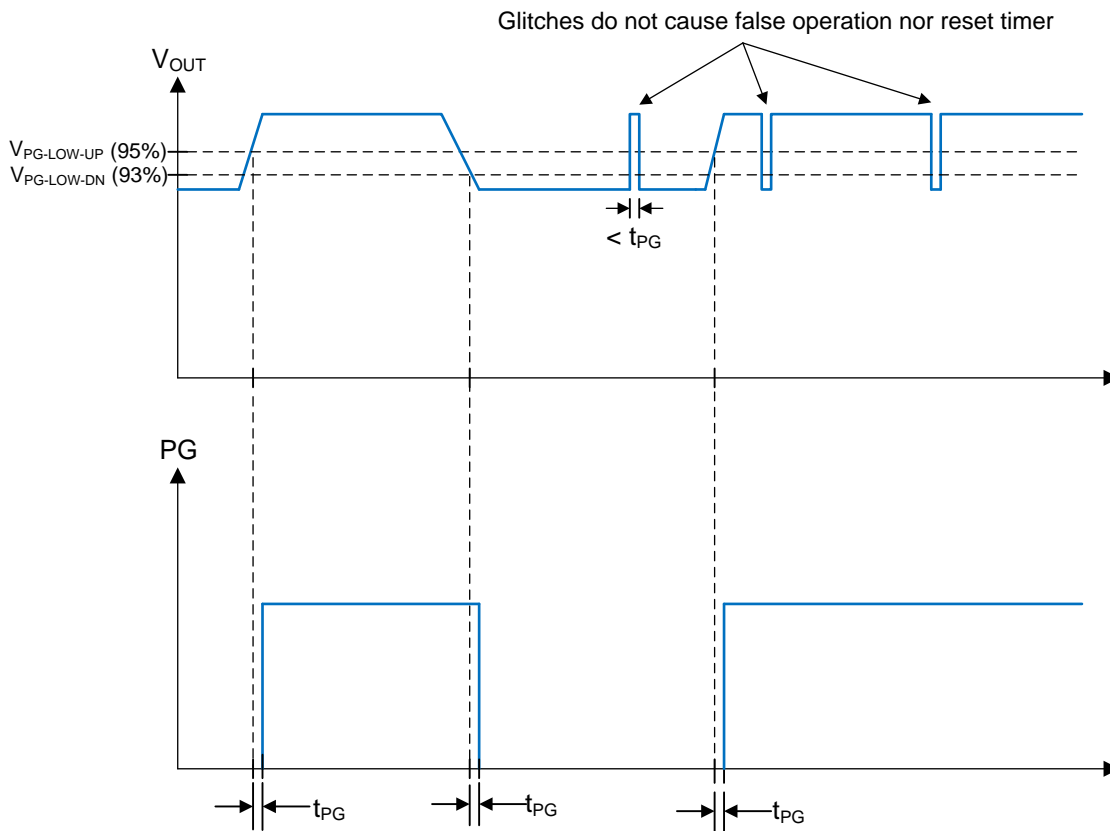


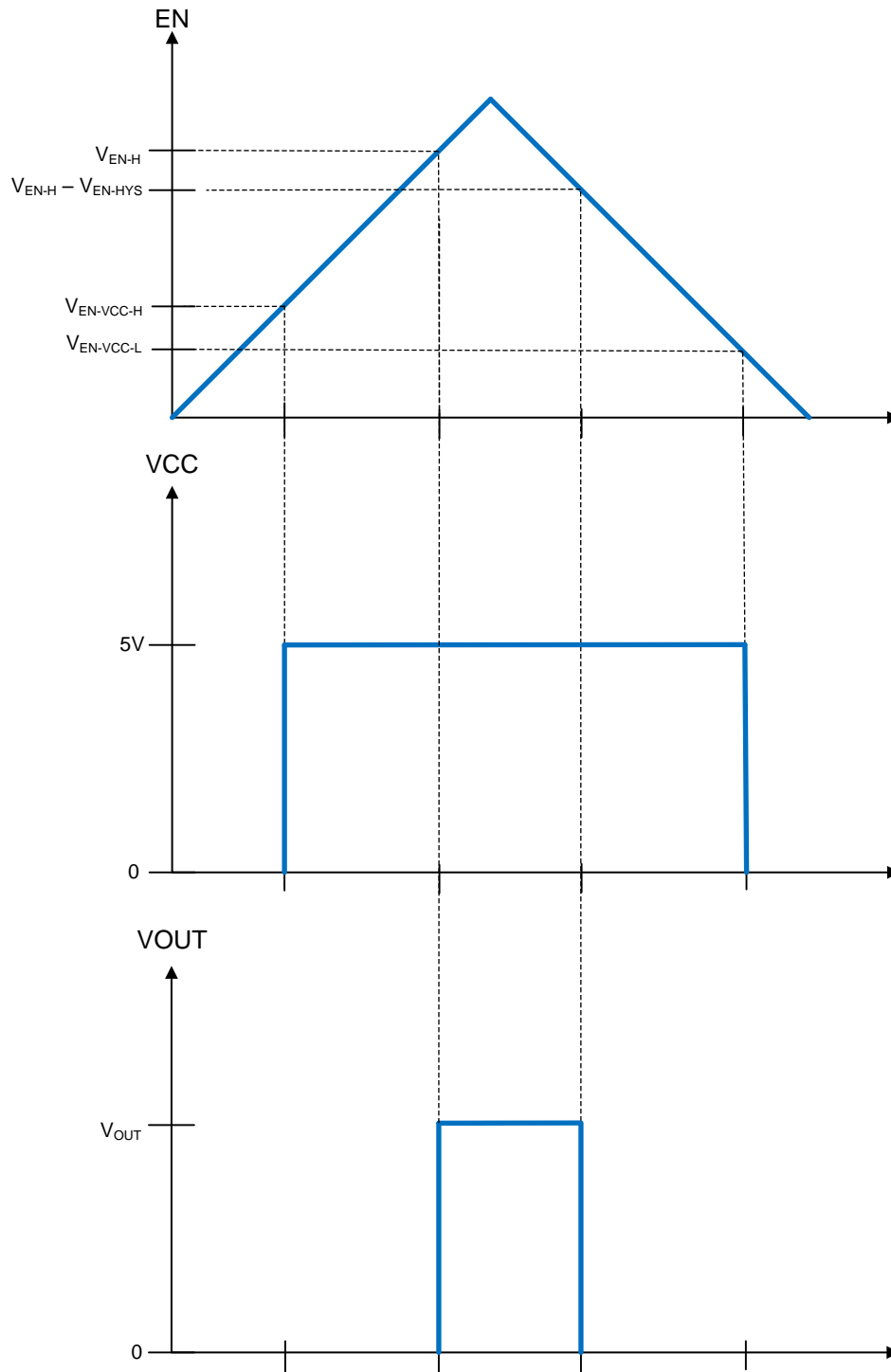
Figure 8. Power-Good-Timing Behavior

8.3.2 Enable and Start-up

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO (see the [External UVLO](#) section). Applying a voltage of  $\geq V_{EN-VCC\_H}$  causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to  $V_{EN-H}$  fully enables the device, allowing it to enter start-up mode and beginning the soft-start period. When the EN input is brought below  $V_{EN-H}$  by  $V_{EN-HYS}$ , the regulator stops running and enters standby mode. Further decrease in the EN voltage to below  $V_{EN-VCC-L}$  completely shuts down the device. This behavior is shown in [Figure 9](#). The EN input may be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in the [Electrical Characteristics](#) table.

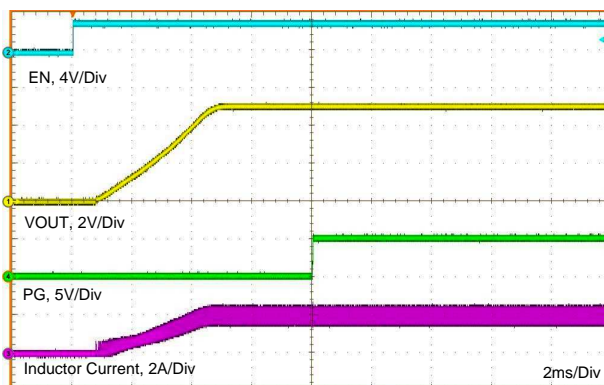
The LMR33620 utilizes a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. A typical start-up waveform is shown in [Figure 10](#) along with typical timings. The rise time of the output voltage is about 4 ms (see [Electrical Characteristics](#)).

**Feature Description (continued)**



**Figure 9. Precision Enable Behavior**

## Feature Description (continued)



**Figure 10. Typical Start-up Behavior**  
 $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 5\text{ V}$ ,  $I_{OUT} = 2\text{ A}$

### 8.3.3 Current Limit and Short Circuit

The LMR33620 incorporates valley current limit for normal overloads and for short-circuit protection. In addition the high-side power MOSFET is protected from excessive current by a peak current limit circuit. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement DEM at light loads (see [Glossary](#)). The typical value of this current limit is found under  $I_{ZC}$  in the [Electrical Characteristics](#).

During overloads the low-side current limit,  $I_{LIMIT}$ , (see [Electrical Characteristics](#) table) determines the maximum load current that the LMR33620 can supply. When the low-side switch turns on, the inductor current begins to ramp down. If the current does not fall below  $I_{LIMIT}$  before the next turn-on cycle, then that cycle is skipped, and the low-side MOSFET is left on until the current falls below  $I_{LIMIT}$ . This is somewhat different than the more typical peak current limit and results in [Equation 1](#) for the maximum load current.

$$I_{OUT}|_{max} = I_{LIMIT} + \frac{(V_{IN} - V_{OUT})}{2 \cdot f_{SW} \cdot L} \cdot \frac{V_{OUT}}{V_{IN}}$$

where

- $f_{SW}$  = Switching frequency
- $L$  = Inductor value

(1)

If, during current limit, the voltage on the FB input falls below about 0.4 V, due to a short circuit, the device enters into hiccup mode. In this mode the device stops switching for  $t_{HC}$  (see [System Characteristics](#)), or about 94 ms and then goes through a normal re-start with soft start. If the short-circuit condition remains, the device runs in current limit for about 20 ms (typical) and then shuts down again. This cycle repeats, as shown in [Figure 11](#) as long as the short-circuit-condition persists. This mode of operation helps to reduce the temperature rise of the device during a hard short on the output. The output current is greatly reduced during hiccup mode (see [Typical Characteristics](#)). Once the output short is removed, and the hiccup delay is passed, the output voltage recovers normally as shown in [Figure 12](#)

The high-side-current limit trips when the peak inductor current reaches  $I_{SC}$  (see [Electrical Characteristics](#) table). This is a cycle-by-cycle current limit and does not produce any frequency or load current fold back. It is meant to protect the high-side MOSFET from excessive current. Under some conditions, such as high input voltages, this current limit may trip before the low-side protection. Under this condition,  $I_{SC}$  determines the maximum output current. Note that  $I_{SC}$  varies with duty cycle.

## Feature Description (continued)

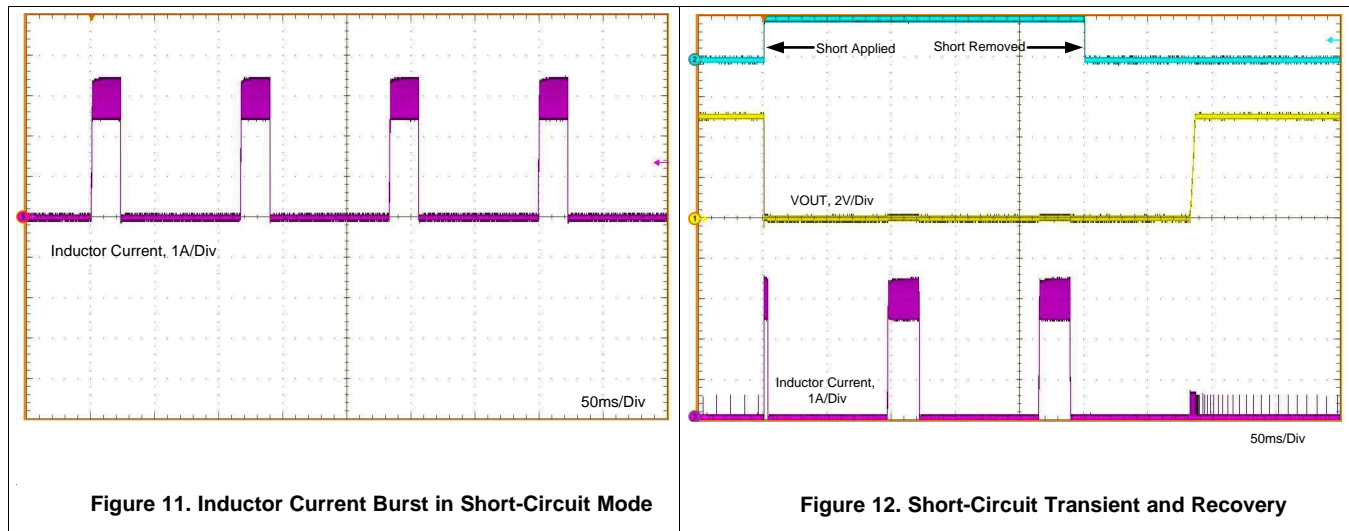


Figure 11. Inductor Current Burst in Short-Circuit Mode

Figure 12. Short-Circuit Transient and Recovery

### 8.3.4 Undervoltage Lockout and Thermal Shutdown

The LMR33620 incorporates an undervoltage-lockout feature on the output of the internal LDO (at the VCC pin). When VCC reaches about 3.7 V the device is ready to receive an EN signal and start up. When VCC falls below about 3 V the device shuts down, regardless of EN status. Since the LDO is in dropout during these transitions, the above values roughly represent the input voltage levels during the transitions.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches about 165°C the device shuts down; re-start occurs when the temperature falls to about 148°C .

## 8.4 Device Functional Modes

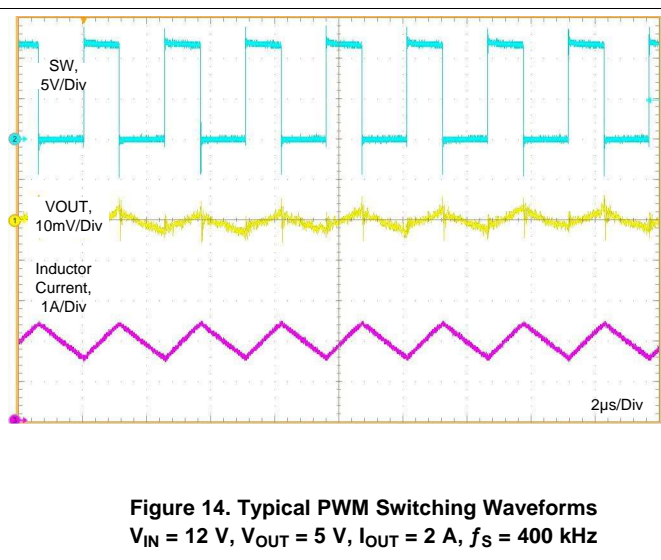
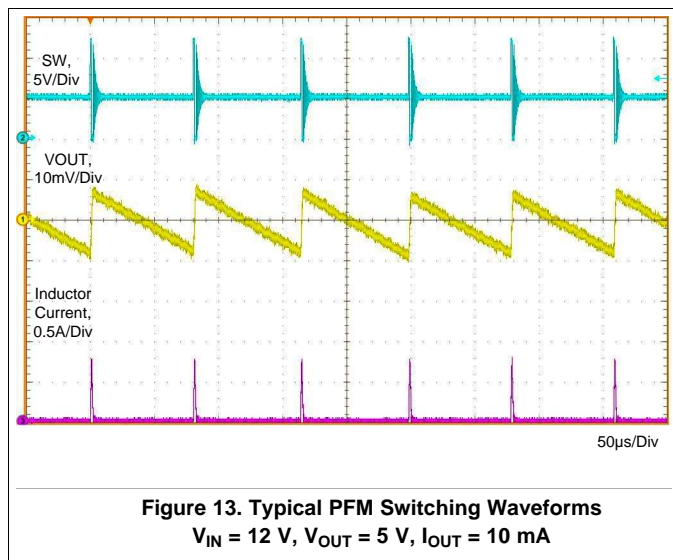
### 8.4.1 Auto Mode

In auto mode the device moves between PWM and PFM as the load changes. At light loads the regulator operates in PFM. At higher loads the mode changes to PWM. The load current for which the device moves from PFM to PWM can be found in the [Application Curves](#). The output current at which the device changes modes depends somewhat on the input voltage, inductor value and the nominal switching frequency. For output currents above the curve, the device is in PWM mode. For currents below the curve, the device is in PFM. The curves apply for a nominal switching frequency of 400 kHz and the BOM shown in [Table 4](#). At higher switching frequencies the load at which the mode change occurs will be greater. For applications where the switching frequency must be known for a given condition, the above mentioned effects must be carefully tested before the design is finalized.

In PWM the regulator operates as a constant frequency, current mode, full synchronous converter using PWM to regulate the output voltage. While operating in this mode the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

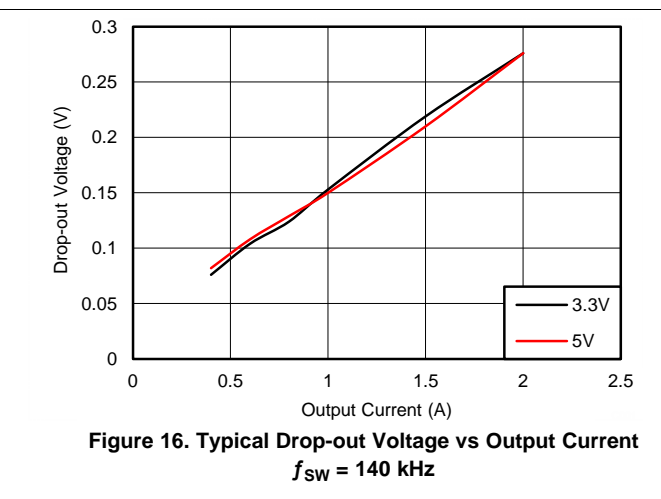
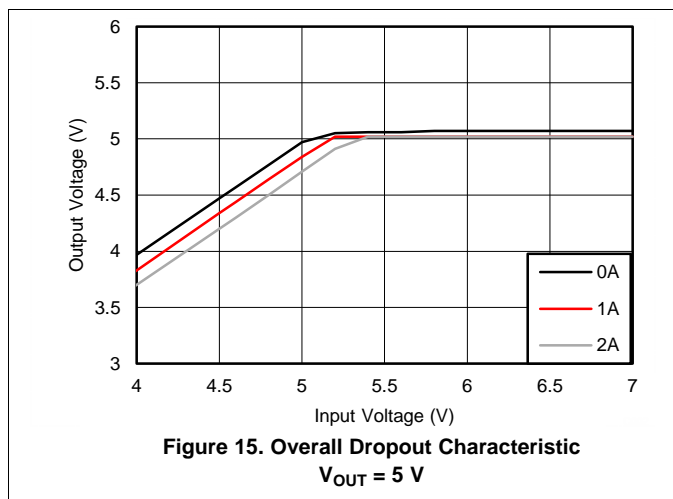
In PFM the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach  $I_{PEAK-MIN}$ . The frequency of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency (see [Glossary](#)). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. This trades off very good light-load efficiency for larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depends on the input voltage, output voltage, and load. Typical switching waveforms in PFM and PWM are shown in [Figure 13](#) and [Figure 14](#). See the [Application Curves](#) for output voltage variation with load in auto mode.

Device Functional Modes (continued)



8.4.2 Dropout

The dropout performance of any buck regulator is affected by the  $R_{DS(ON)}$  of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage is reduced to near the output voltage, the off-time of the high side MOSFET starts to approach the minimum value (see *Timing Characteristics*). Beyond this point the switching may become erratic, and/or the output voltage falls out of regulation. To avoid this problem the LMR33620 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. In this data sheet the dropout voltage is defined as the difference between the input and output voltage when the output has dropped by 1% of its nominal value. Under this condition the switching frequency has dropped to its minimum value of about 140 kHz. Note that the 0.4 V short circuit detection threshold is not activated when in dropout mode. Typical drop-out characteristics can be found in Figure 15, Figure 16, Figure 17, and Figure 18.



Device Functional Modes (continued)

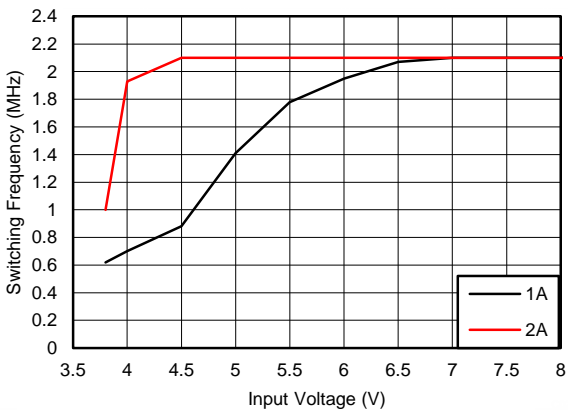


Figure 17. Typical Switching Frequency in Drop-out Mode  
 $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 2.1\text{ MHz}$

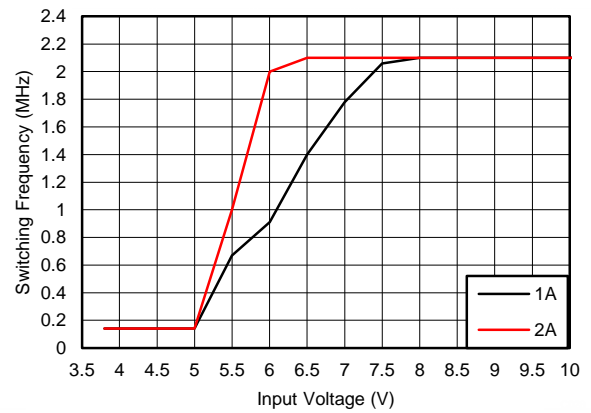


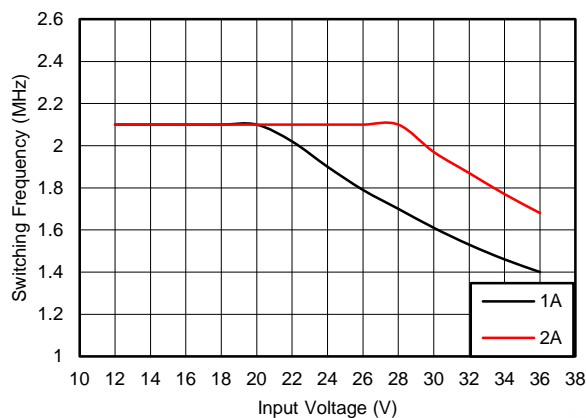
Figure 18. Typical Switching Frequency in Drop-out Mode  
 $V_{OUT} = 5\text{ V}$ ,  $f_{SW} = 2.1\text{ MHz}$

**Device Functional Modes (continued)**

**8.4.3 Minimum Switch On-Time**

Every switching regulator has a minimum controllable on-time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle and therefore a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the LMR33620 automatically reduces the switching frequency when the minimum on-time limit is reached. In this way the converter can regulate the lowest programmable output voltage at the maximum input voltage. An estimate for the approximate input voltage, for a given output voltage, before frequency fold-back occurs is found in Equation 2. The values of  $t_{ON}$  and  $f_{SW}$  can be found in the *Electrical Characteristics* table. As the input voltage is increased, the switch on-time (duty-cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops, while the on-time remains fixed. This relationship is highlighted in Figure 19 for a nominal switching frequency of 2.1 MHz.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \cdot f_{SW}} \tag{2}$$



**Figure 19. Switching Frequency vs Input Voltage**  
**V<sub>OUT</sub> = 3.3 V,**

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### NOTE

In this data sheet the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature; not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias the capacitance drops considerably. Large case sizes and/or higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank should be made in order to ensure that the minimum value of *effective* capacitance is provided.

### 9.1 Application Information

The LMR33620 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A. The following design procedure can be used to select components for the LMR33620. Alternately, the WEBENCH® Design Tool may be used to generate a complete design. This tool utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various options.

### 9.2 Typical Application

Figure 20 shows a typical application circuit for the LMR33620. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, Table 2 provides typical component values for a range of the most common output voltages. The values given in the table are typical. Other values may be used to enhance certain performance criterion as required by the application.

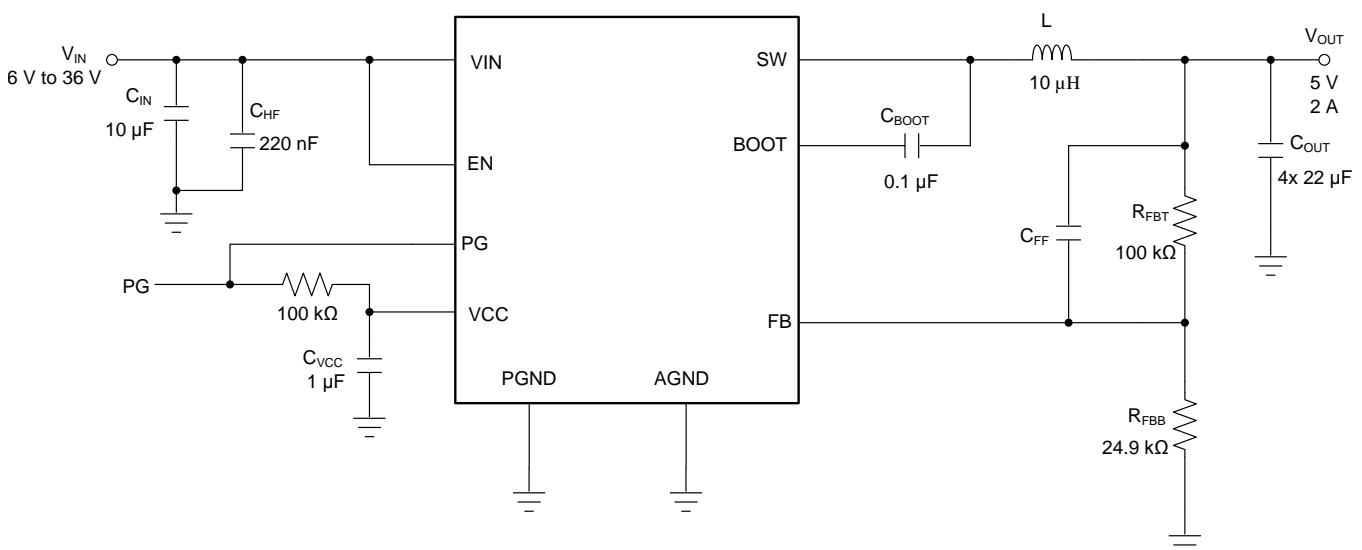


Figure 20. Example Application Circuit (400 kHz)

## Typical Application (continued)

### 9.2.1 Design Requirements

Table 1 provides the parameters for our detailed design procedure example:

**Table 1. Detailed Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V (6 V to 36 V)
Output voltage	5 V
Maximum output current	0 A to 2 A
Switching frequency	400 kHz

**Table 2. Typical External Component Values**

$f_{sw}$ (kHz)	$V_{OUT}$ (V)	L ( $\mu$ H)	$C_{OUT}$ (rated capacitance)	$R_{FBT}$ ( $\Omega$ )	$R_{FBB}$ ( $\Omega$ )	$C_{IN} + C_{HF}$	$C_{BOOT}$	$C_{VCC}$	$C_{FF}$
400	3.3	10	4 x 22 $\mu$ F	100 k	43.2 k	10 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	open
1400	3.3	2.2	2 x 22 $\mu$ F	100 k	43.2 k	10 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	open
2100	3.3	1.2	2 x 22 $\mu$ F	100 k	43.2 k	10 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	open
400	5	10	4 x 22 $\mu$ F	100 k	24.9 k	10 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	open
1400	5	2.2	2 x 22 $\mu$ F	100 k	24.9 k	10 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	open
2100	5	1.5	2 x 22 $\mu$ F	100 k	24.9 k	10 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	open
400	12	27	4 x 22 $\mu$ F	100 k	9.09 k	10 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	open
1400	12	4.7	4 x 10 $\mu$ F	100 k	9.09 k	10 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	open
2100	12	3.3	4 x 10 $\mu$ F	100 k	9.09 k	10 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	open

### 9.2.2 Detailed Design Procedure

The following design procedure applies to [Figure 20](#) and [Table 1](#).

#### 9.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LMR33620 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

#### 9.2.2.2 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, and hence a more compact design. For this example we choose 400 kHz.

### 9.2.2.3 Setting the Output Voltage

The output voltage of LMR33620 is externally adjustable using a resistor divider network. The range of recommended output voltage is found in the [Recommended Operating Conditions](#) table. The divider network is comprised of  $R_{FBT}$  and  $R_{FBB}$ , and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage,  $V_{REF}$ . The resistance of the divider is a compromise between excessive noise pick-up and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for  $R_{FBT}$  is 100 k $\Omega$ ; with a maximum value of 1 M $\Omega$ . If a 1 M $\Omega$  is selected for  $R_{FBT}$ , then a feed-forward capacitor must be used across this resistor to provide adequate loop phase margin (see [C<sub>FF</sub> Selection](#)). Once  $R_{FBT}$  is selected, [Equation 3](#) is used to select  $R_{FBB}$ .  $V_{REF}$  is nominally 1 V (see [Electrical Characteristics](#) for limits).

$$R_{FBB} = \frac{R_{FBT}}{\left[ \frac{V_{OUT}}{V_{REF}} - 1 \right]} \quad (3)$$

For this 5-V example,  $R_{FBT} = 100$  k $\Omega$  and  $R_{FBB} = 24.9$  k $\Omega$  are chosen.

### 9.2.2.4 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current should be used. [Equation 4](#) can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example we choose  $K = 0.3$  and find an inductance ; we select the next standard value of 10  $\mu$ H.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUTmax}} \cdot \frac{V_{OUT}}{V_{IN}} \quad (4)$$

Ideally, the saturation current rating of the inductor should be at least as large as the high-side switch current limit,  $I_{SC}$  (see [Electrical Characteristics](#) ). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit,  $I_{LIMIT}$ , is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This may lead to component damage; do not allow the inductor to saturate! Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies above about 1 MHz. In any case the inductor saturation current should not be less than the device low-side current limit,  $I_{LIMIT}$  (see [Electrical Characteristics](#)). In order to avoid sub-harmonic oscillation, the inductance value should not be less than that given in [Equation 5](#) The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current should be no less than about 10% of the device maximum rated current under nominal conditions.

$$L_{MIN} \geq 0.36 \cdot \frac{V_{OUT}}{f_{SW}} \quad (5)$$

### 9.2.2.5 Output Capacitor Selection

The value of the output capacitor, and its ESR, determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements, rather than the output voltage ripple. Equation 6 can be used to estimate a lower bound on the total output capacitance, and an upper bound on the ESR, required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[ (1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[ 1+K + \frac{K^2}{12} \cdot \left( 1 + \frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- $\Delta V_{OUT}$  = output voltage transient
  - $\Delta I_{OUT}$  = output current transient
  - $K$  = Ripple factor from [Inductor Selection](#)
- (6)

Once the output capacitor and ESR have been calculated, Equation 7 can be used to check the peak-to-peak output voltage ripple;  $V_r$ .

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}}$$
(7)

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

For this example we require a  $\Delta V_{OUT}$  of  $\leq 250$  mV for an output current step of  $\Delta I_{OUT} = 2$  A. Equation 6 gives a minimum value of  $45 \mu\text{F}$  and a maximum ESR of  $0.11 \Omega$ . Assuming a 20% tolerance and a 10% bias de-rating, we arrive at a minimum capacitance of  $63 \mu\text{F}$ . This can be achieved with a bank of  $4 \times 22\text{-}\mu\text{F}$ , 16-V, ceramic capacitors in the 1210 case size. More output capacitance can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases an aluminum electrolytic capacitor can be placed in parallel with the ceramics to help build up the required value of capacitance. In general use a capacitor of at least 10 V for output voltages of 3.3 V or less, while a capacitor of 16 V or more should be used for output voltages of 5 V and above.

In practice the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and Bode plots are the best way to validate any given design and should always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help to reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

The maximum value of total output capacitance should be limited to about 10 times the design value, or  $1000 \mu\text{F}$ , whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

### 9.2.2.6 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of  $10 \mu\text{F}$  of ceramic capacitance is required on the input of the LMR33620. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and/or maintain the input voltage during load transients. In addition a small case size 220-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency

bypass for the control circuits internal to the device. For this example a 10- $\mu$ F, 50-V, X7R (or better) ceramic capacitor is chosen. The 220 nF must also be rated at 50 V with an X7R dielectric. The VQFN (RNX) package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split, and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. In this example, place two 4.7- $\mu$ F and two 100-nF ceramic capacitors at each VIN/PGND location. A single 10- $\mu$ F can also be used on one side of the package.

Many times it is desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor(s). The approximate RMS value of this current can be calculated from [Equation 8](#) and should be checked against the manufacturers' maximum ratings.

$$I_{\text{RMS}} \cong \frac{I_{\text{OUT}}}{2} \quad (8)$$

### 9.2.2.7 $C_{\text{BOOT}}$

The LMR33620 requires a boot-strap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 10 V is required.

### 9.2.2.8 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1- $\mu$ F, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see [Power-Good Flag Output](#)). A value of 100 k $\Omega$  is a good choice in this case. The nominal output voltage on VCC is 5 V; see [Electrical Characteristics](#) for limits. Do not short this output to ground or any other external voltage.

### 9.2.2.9 $C_{\text{FF}}$ Selection

In some cases a feed-forward capacitor can be used across  $R_{\text{FBT}}$  to improve the load transient response or improve the loop-phase margin. This is especially true when values of  $R_{\text{FBT}} > 100$  k $\Omega$  are used. Large values of  $R_{\text{FBT}}$ , in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A  $C_{\text{FF}}$  can help to mitigate this effect. [Equation 9](#) can be used to estimate the value of  $C_{\text{FF}}$ . The value found with [Equation 9](#) is a starting point; use lower values to determine if any advantage is gained by the use of a  $C_{\text{FF}}$  capacitor. The application report [Optimizing Transient Response of Internally Compensated DC-DC Converters with Feed-forward Capacitor](#) is helpful when experimenting with a feed-forward capacitor.

$$C_{\text{FF}} < \frac{V_{\text{OUT}} \cdot C_{\text{OUT}}}{120 \cdot R_{\text{FBT}} \cdot \sqrt{\frac{V_{\text{REF}}}{V_{\text{OUT}}}}} \quad (9)$$

### 9.2.2.10 External UVLO

In some cases an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in [Figure 21](#). The input voltage at which the device turns on is designated  $V_{\text{ON}}$ ; while the turnoff voltage is  $V_{\text{OFF}}$ . First a value for  $R_{\text{ENB}}$  is chosen in the range of 10 k $\Omega$  to 100 k $\Omega$  and then [Equation 10](#) is used to calculate  $R_{\text{ENT}}$  and  $V_{\text{OFF}}$ .

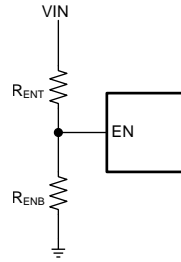


Figure 21. Set-Up for External UVLO Application

$$R_{ENT} = \left( \frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left( 1 - \frac{V_{EN-HYS}}{V_{EN-H}} \right)$$

where

- $V_{ON} = V_{IN}$  turnon voltage
  - $V_{OFF} = V_{IN}$  turnoff voltage
- (10)

### 9.2.2.11 Maximum Ambient Temperature

As with any power conversion device, the LMR33620 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature ( $T_J$ ) is a function of the ambient temperature, the power loss and the effective thermal resistance,  $R_{\theta JA}$  of the device and PCB combination. The maximum internal die temperature for the LMR33620 must be limited to 125°C. This establishes a limit on the maximum device power dissipation and therefore the load current. Equation 11 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures ( $T_A$ ) and larger values of  $R_{\theta JA}$  reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions can not be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of  $R_{\theta JA}$  is more difficult to estimate. As stated in *Semiconductor and IC Package Thermal Metrics*, the value of  $R_{\theta JA}$  given in the *Thermal Information* table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1 - \eta)} \cdot \frac{1}{V_{OUT}}$$

where

- $\eta$  = Efficiency
- (11)

The effective  $R_{\theta JA}$  is a critical parameter and depends on many factors such as power dissipation, air temperature/flow, PCB area, copper heat-sink area, number of thermal vias under the package, and adjacent component placement; to mention just a few. The HSOIC (DDA) package utilizes a die attach paddle, or thermal pad (PAD) to provide a place to solder down to the PCB heat-sinking copper. This provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. Due to the ultra-miniature size of the VQFN (RNx) package, a DAP is not available. This means that this package exhibits a somewhat large value  $R_{\theta JA}$ . Typical examples of  $R_{\theta JA}$  vs copper board area can be found in Figure 22 and Figure 23. The copper area given in the graph is for each layer; the top and bottom layers are 2 oz. copper each, while the inner layers are 1 oz. A typical curve of maximum output current vs. ambient temperature is shown in Figure 24. This data was taken with a device/PCB combination giving an  $R_{\theta JA}$  of about 30°C/W. It must be remembered that the data given in these graphs are for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.

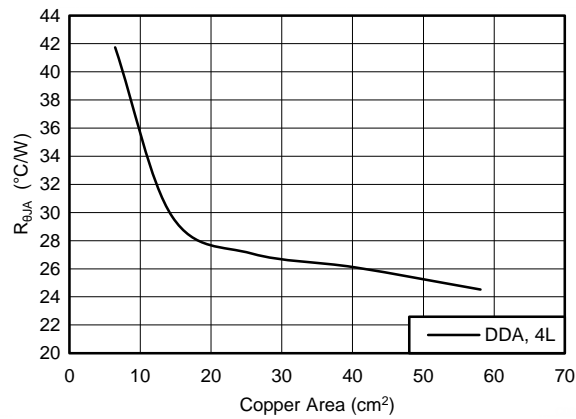


Figure 22. Typical  $R_{\theta JA}$  vs Copper Area for a Four-Layer Board and the HSOIC (DDA) Package

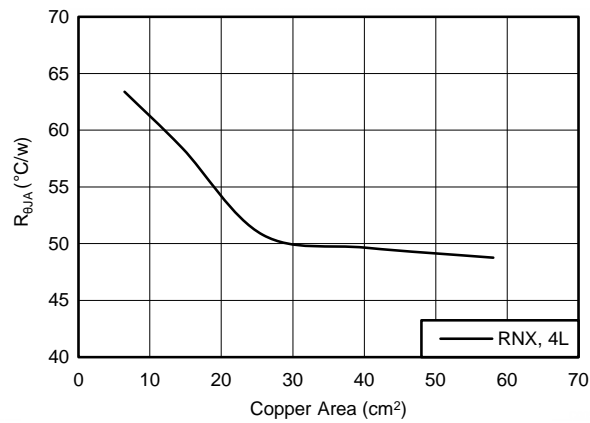


Figure 23.  $R_{\theta JA}$  vs Copper Board Area for the VQFN (RNX) Package

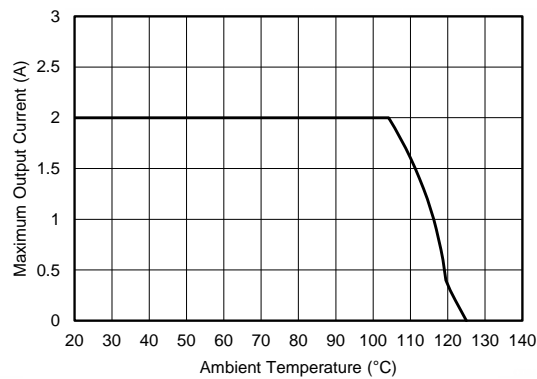


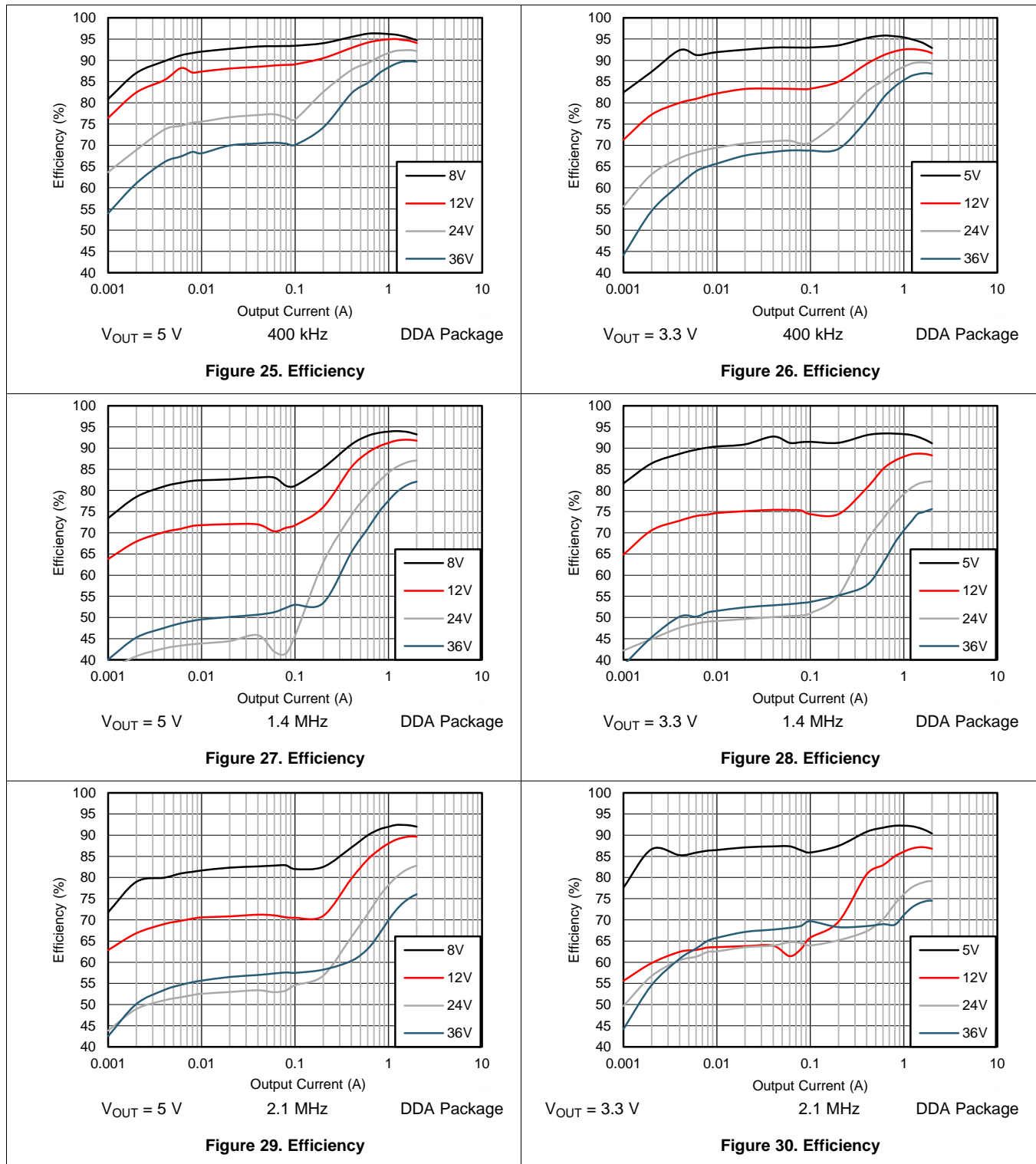
Figure 24. Maximum Output Current vs Ambient Temperature  
 $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 5\text{ V}$ ,  $f_{SW} = 400\text{ kHz}$ ,  $R_{\theta JA} = 30^\circ\text{C/W}$

The resources below can be used as a guide to optimal thermal PCB design and estimating  $R_{\theta JA}$  for a given application environment:

- [Thermal Design by Insight not Hindsight](#)
- [A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages](#)
- [Semiconductor and IC Package Thermal Metrics](#)
- [Thermal Design Made Simple with LM43603 and LM43602](#)
- [SLMA002 PowerPAD™ Thermally Enhanced Package](#)
- [PowerPAD™ Made Easy](#)
- [SBVA025 Using New Thermal Metrics](#)

### 9.2.3 Application Curves

Unless otherwise specified the following conditions apply:  $V_{IN} = 12\text{ V}$ ,  $T_A = 25^\circ\text{C}$ . The circuit is shown in [Figure 49](#), with the appropriate BOM from [Table 3](#) or [Table 4](#).



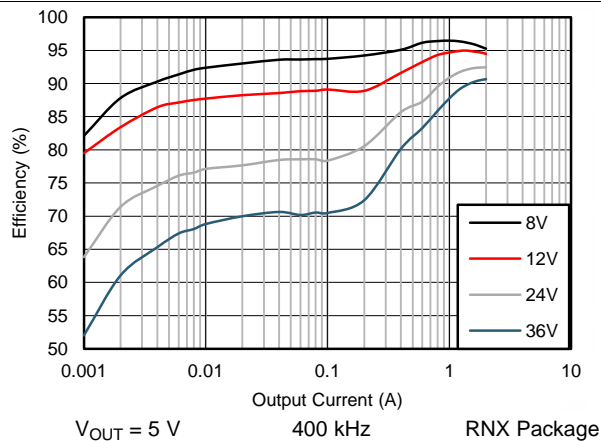


Figure 31. Efficiency

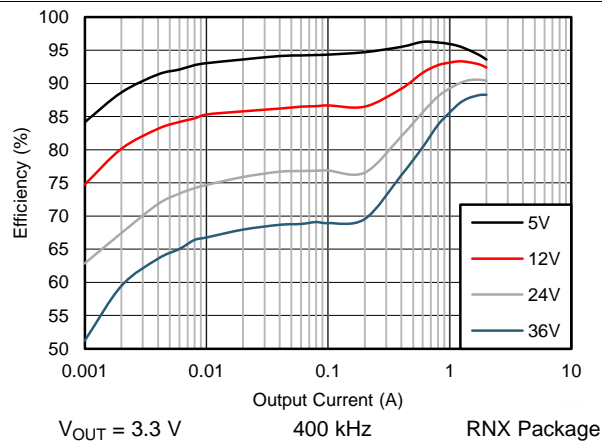


Figure 32. Efficiency

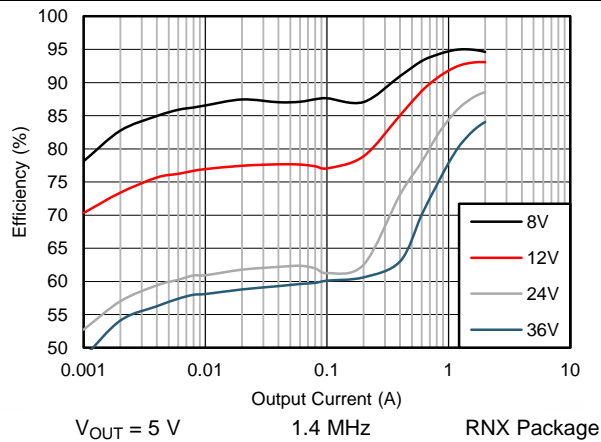


Figure 33. Efficiency

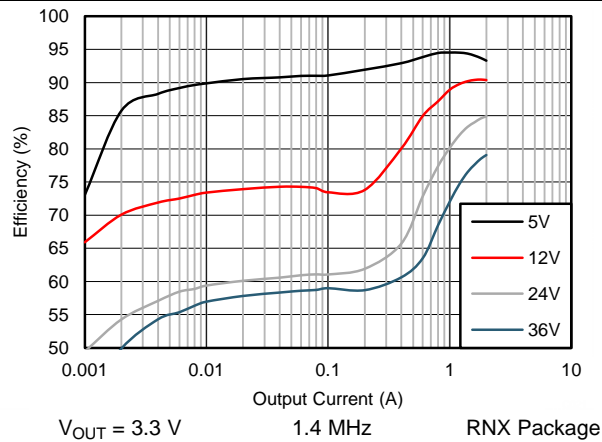


Figure 34. Efficiency

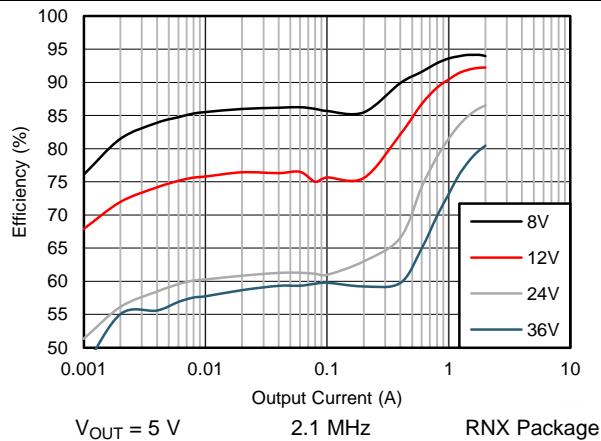


Figure 35. Efficiency

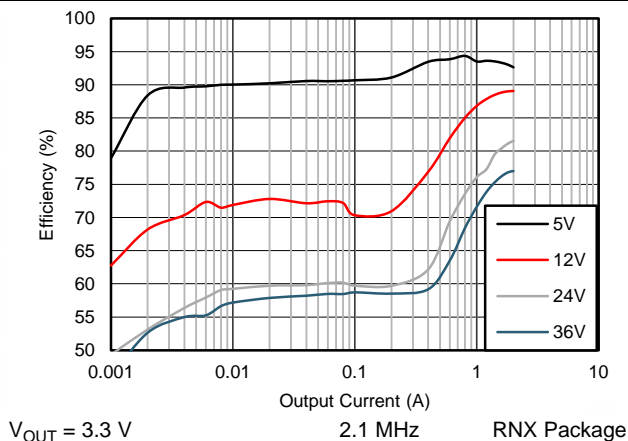
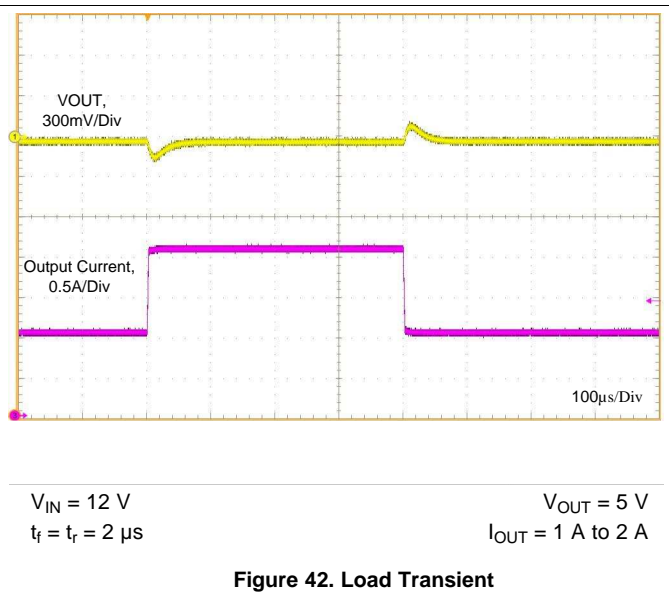
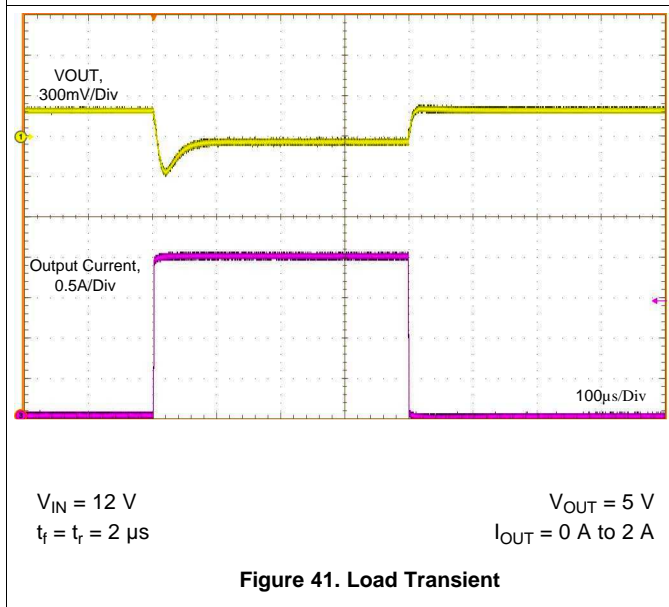
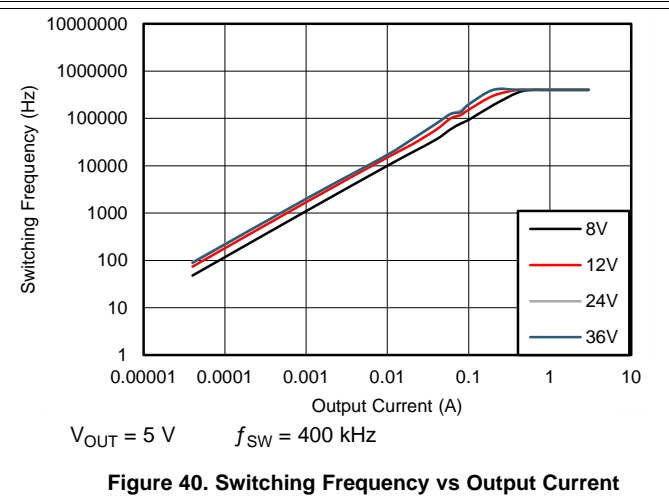
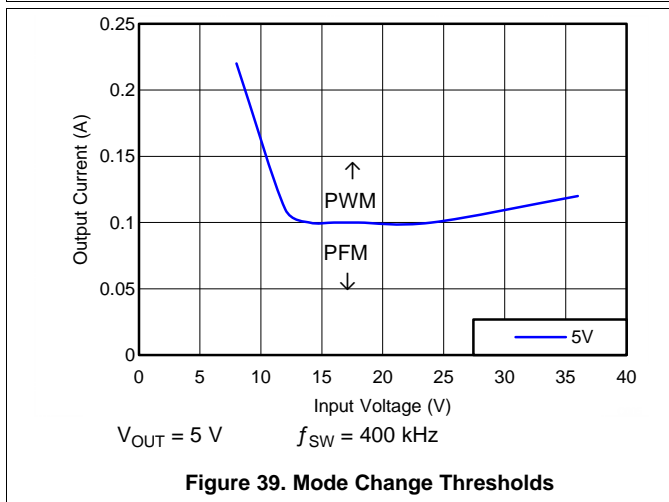
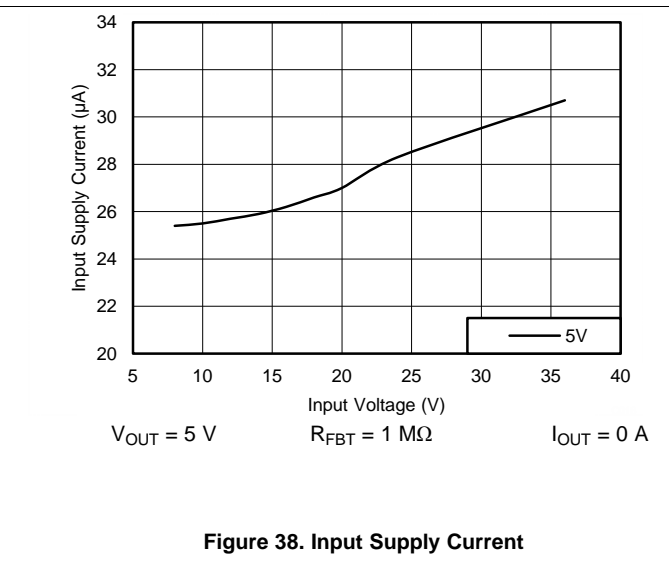
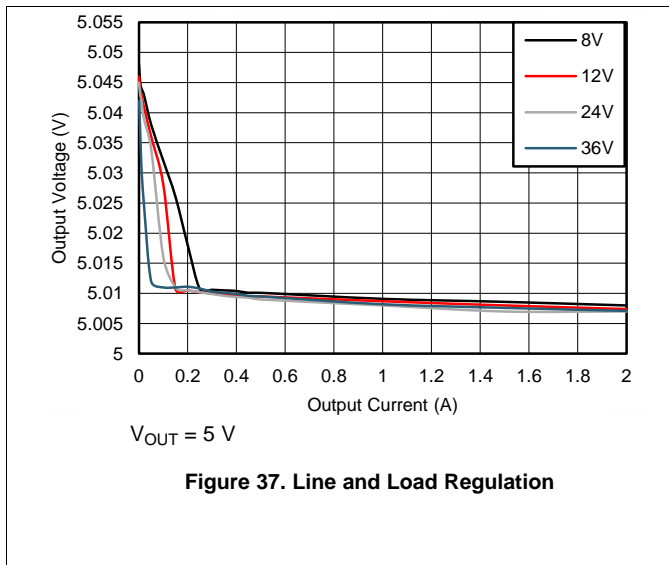


Figure 36. Efficiency

**LMR33620**

SNVSAW1A – FEBRUARY 2018 – REVISED APRIL 2018

www.ti.com



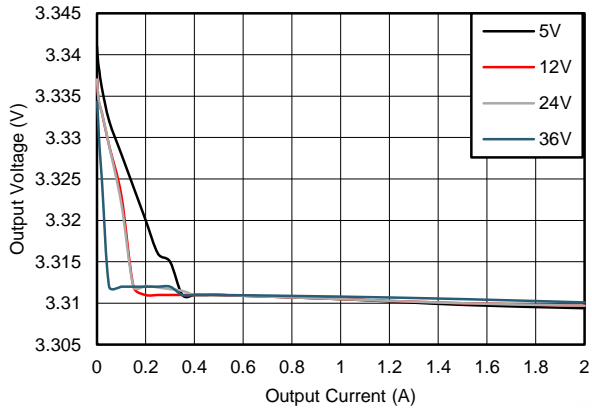


Figure 43. Line and Load Regulation

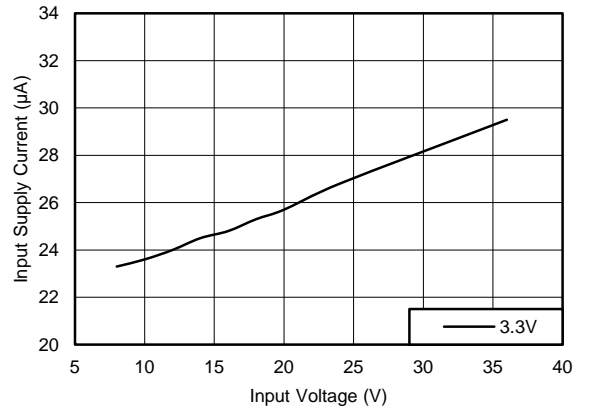


Figure 44. Input Supply Current

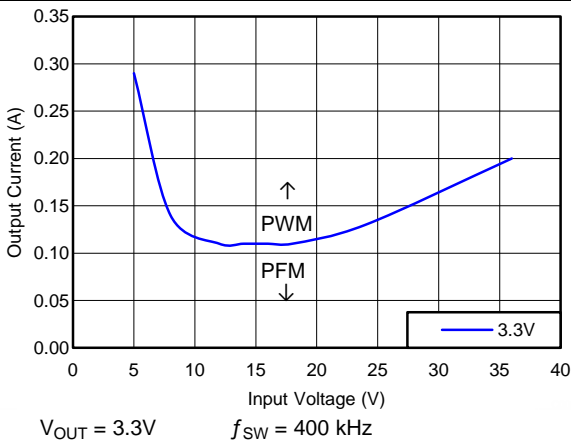


Figure 45. Mode Change Thresholds

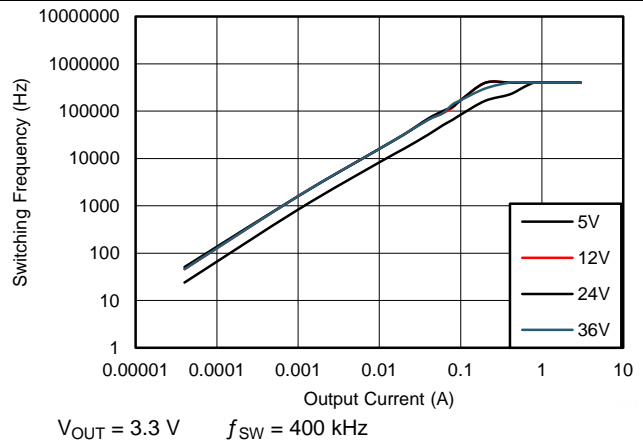


Figure 46. Switching Frequency vs Output Current

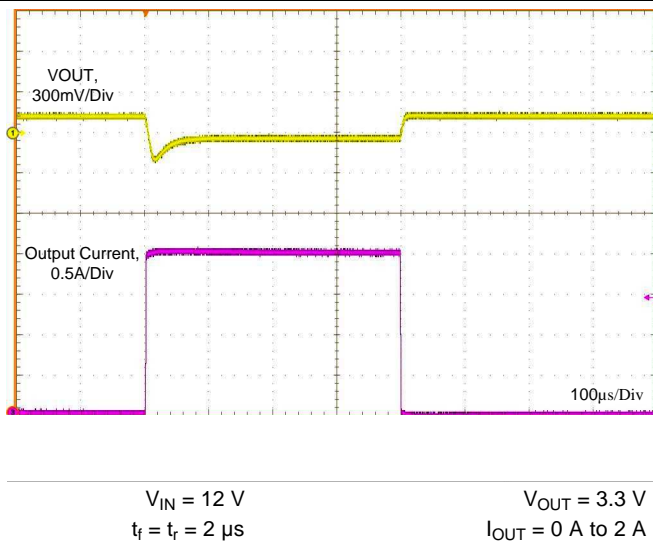


Figure 47. Load Transient

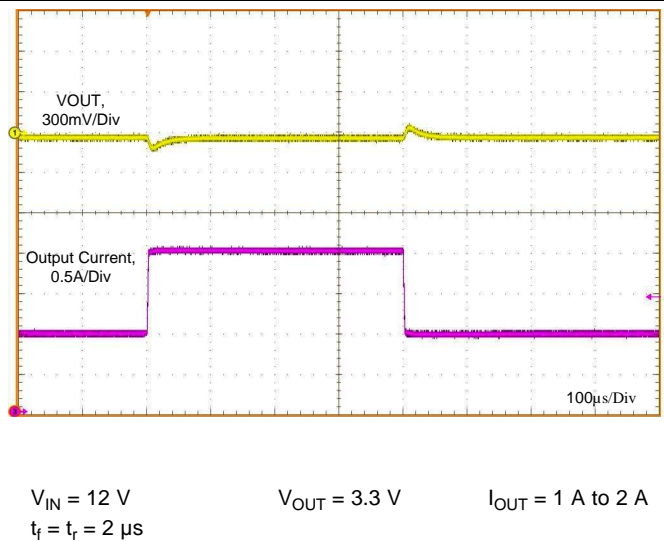
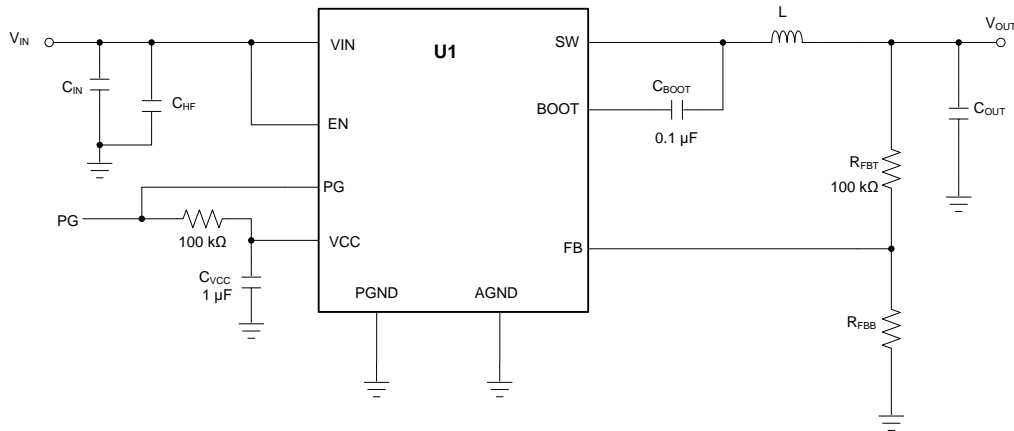


Figure 48. Load Transient


**Figure 49. Circuit for Application Curves**
**Table 3. BOM for Typical Application Curves DDA Package<sup>(1)</sup>**

V <sub>OUT</sub>	FREQUENCY	R <sub>FBB</sub>	C <sub>OUT</sub>	C <sub>IN</sub> + C <sub>HF</sub>	L	U1
3.3 V	400 kHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	6.8 µH, 14 mΩ	LMR33620ADDA
3.3 V	1400 KHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	2.2 µH, 11.4 mΩ	LMR33620BDDB
3.3 V	2100 kHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	1.2 µH, 16 mΩ	LMR33620CDDA
5 V	400 kHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	8.2 µH, 14 mΩ	LMR33620ADDA
5 V	1400 KHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	2.2 µH, 11.4 mΩ	LMR33620BDDB
5 V	2100 kHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	1.5 µH, 8.2 mΩ	LMR33620CDDA

(1) The values in this table were selected to enhance certain performance criteria and may not represent typical values.

**Table 4. BOM for Typical Application Curves RNX Package<sup>(1)</sup>**

V <sub>OUT</sub>	FREQUENCY	R <sub>FBB</sub>	C <sub>OUT</sub>	C <sub>IN</sub> + C <sub>HF</sub>	L	U1
3.3 V	400 kHz	43.3 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	4.7 µH, 28 mΩ	LMR33620ARNX
3.3 V	1400 KHz	43.3 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	2.2 µH, 11.4 mΩ	LMR33620BRNX
3.3 V	2100 kHz	43.3 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	2.2 µH, 11.4 mΩ	LMR33620CRNX
5 V	400 kHz	24.9 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	6.8 µH, 14 mΩ	LMR33620ARNX
5 V	1400 KHz	24.9 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	2.2 µH, 11.4 mΩ	LMR33620BRNX
5 V	2100 kHz	24.9 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	2.2 µH, 11.4 mΩ	LMR33620CRNX

(1) The values in this table were selected to enhance certain performance criteria and may not represent typical values.

### 9.3 Do's and Don'ts

- **Don't:** Exceed the [Absolute Maximum Ratings](#)
- **Don't:** Exceed the [ESD Ratings](#)
- **Don't:** Exceed the [Recommended Operating Conditions](#)
- **Don't:** Allow the EN input to float.
- **Don't:** Allow the output voltage to exceed the input voltage, nor go below ground.
- **Don't:** Use the value of R<sub>θJA</sub> given in the [Thermal Information](#) table to design your application.
- **Do:** Follow all the guidelines and/or suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success (see [Community Resources](#)).

## 10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the [Absolute Maximum Ratings](#) and [Recommended Operating Conditions](#) found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with [Equation 12](#), where  $\eta$  is the efficiency.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (12)$$

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under damped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip may cause the regulator to momentarily shutdown and/or reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help to damp the input resonant circuit and reduce any overshoots. A value in the range of 20  $\mu$ F to 100  $\mu$ F is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The user guide [AN-2162 Simple Success With Conducted EMI From DCDC Converters](#) provides helpful suggestions when designing an input filter for any switching regulator.

In some cases a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow may damage the device.

The input voltage should not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors will discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then a Schottky diode between the input supply and the output should be used.

## 11 Layout

### 11.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter the most critical PCB feature is the loop formed by the input capacitor(s) and power ground, as shown in [Figure 50](#). This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages will disrupt the proper operation of the converter. Because of this, the traces in this loop should be wide and short, and the loop area as small as possible to reduce the parasitic inductance. [Figure 51](#) and [Figure 52](#) show recommended layouts for the critical components of the LMR33620 .

1. **Place the input capacitor(s) as close as possible to the VIN and GND terminals.** VIN and GND pins are adjacent, simplifying the input capacitor placement.
2. **Place bypass capacitor for VCC close to the VCC pin.** This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. **Use wide traces for the  $C_{BOOT}$  capacitor.** Place  $C_{BOOT}$  close to the device with short/wide traces to the BOOT and SW pins. For the VQFN package, it is important to route the SW connection under the device to the NC pin, and use this path to connect the BOOT capacitor to SW.
4. **Place the feedback divider as close as possible to the FB pin of the device.** Place  $R_{FBB}$ ,  $R_{FBT}$ , and  $C_{FF}$ , if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to  $V_{OUT}$  can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. **Use at least one ground plane in one of the middle layers.** This plane acts as a noise shield and also act as a heat dissipation path.
6. **Connect the thermal pad to the ground plane.** The SOIC package has a thermal pad (PAD) connection that must be soldered down to the PCB ground plane. This pad acts as a heat-sink connection and an electrical ground connection for the regulator. The integrity of this solder connection has a direct bearing on the total effective  $R_{\theta JA}$  of the application.
7. **Provide wide paths for VIN, VOUT, and GND.** Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. **Provide enough PCB area for proper heat sinking.** As stated in the [Maximum Ambient Temperature](#) section, enough copper area must be used to ensure a low  $R_{\theta JA}$ , commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. With the SOIC package, use an array of heat-sinking vias to connect the thermal pad (PAD) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
9. **Keep switch area small.** Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time the total area of this node should be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- [Layout Guidelines for Switching Power Supplies](#)
- [Simple Switcher PCB Layout Guidelines](#)
- [Construction Your Power Supply- Layout Considerations](#)
- [Low Radiated EMI Layout Made Simple with LM4360x and LM4600x](#)

Layout Guidelines (continued)

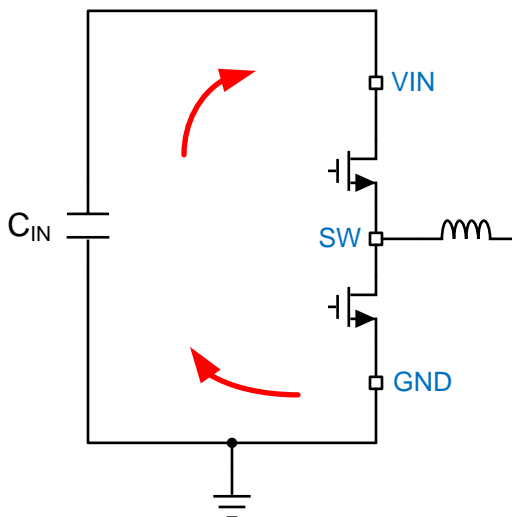


Figure 50. Current Loops with Fast Edges

11.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins should be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and may bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by utilizing the thermal pad (PAD) of the device as the primary thermal path. Use a minimum 4 × 3 array of 10 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

### 11.2 Layout Example

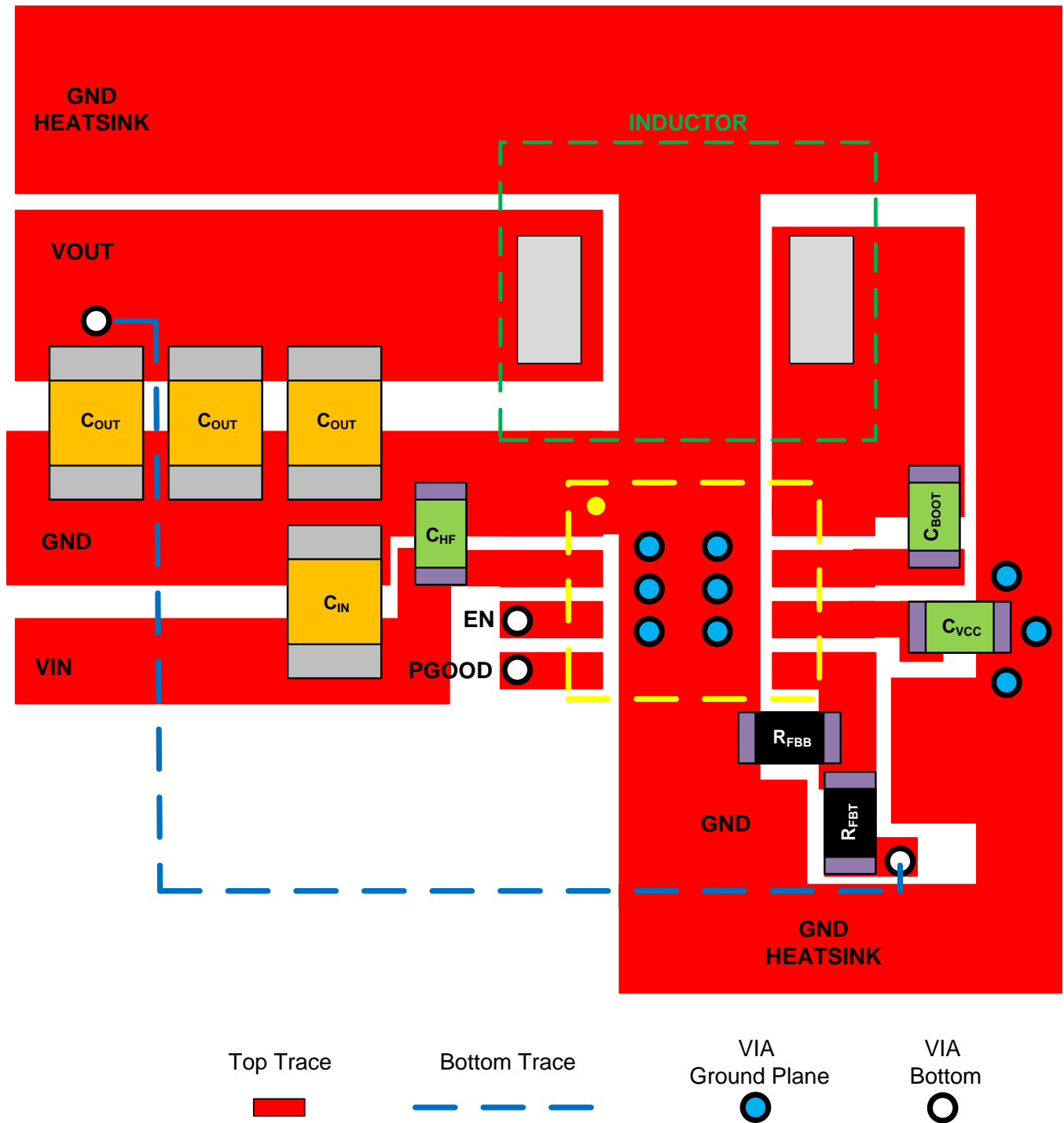
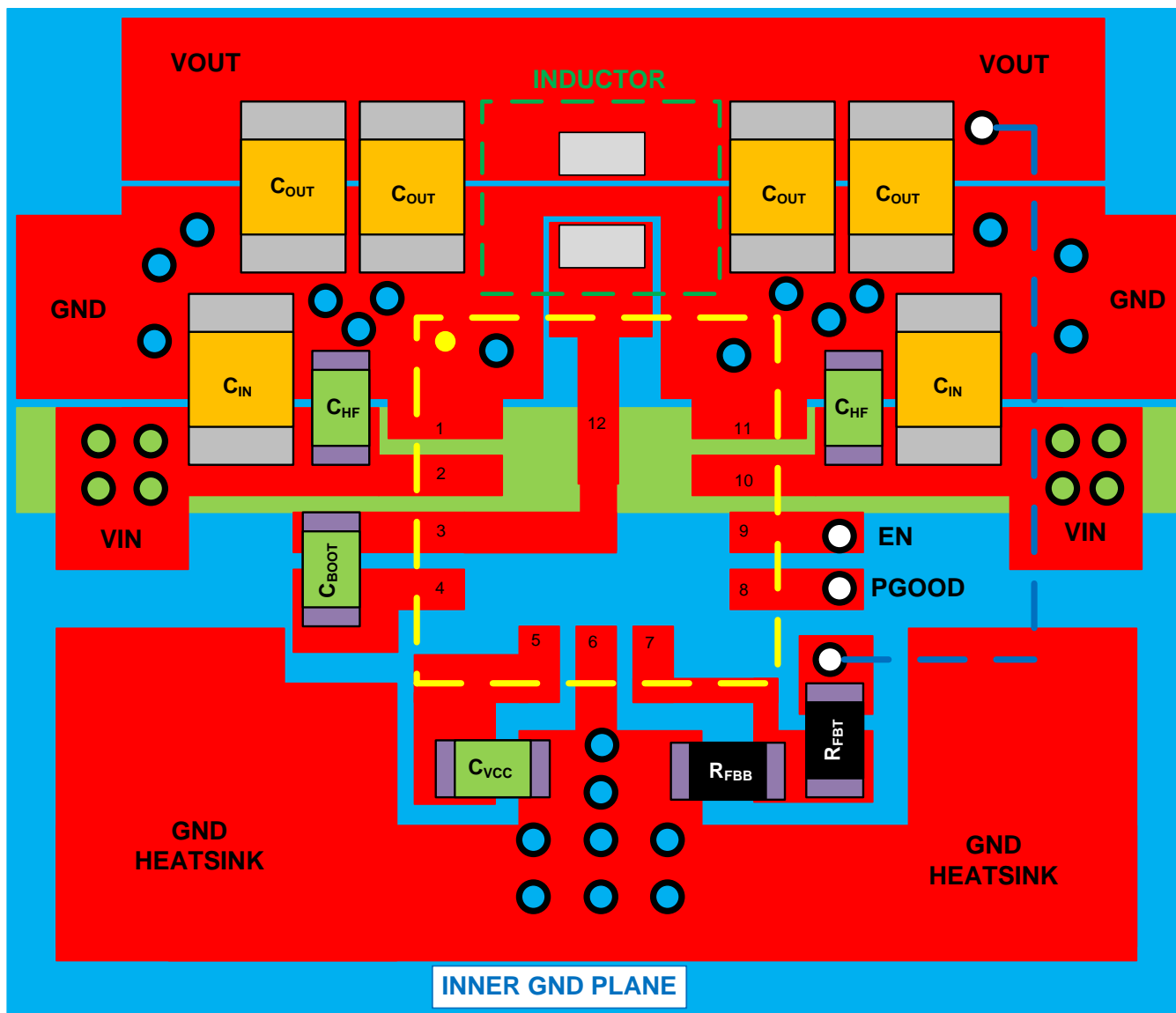


Figure 51. Example Layout for HSOIC (DDA) Package

Layout Example (continued)



- Top Trace/Plane █
- Inner GND Plane █
- VIN Strap on Inner Layer █
- VIA to Signal Layer
- VIA to GND Planes
- VIA to VIN Strap
- Trace on Signal Layer — — — — —

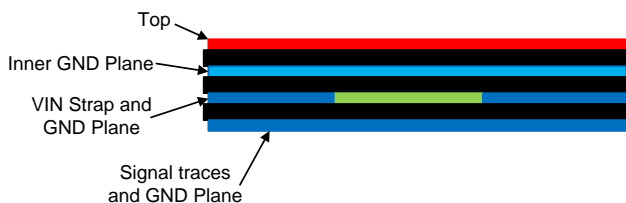


Figure 52. Example Layout for VQFN Package

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

##### 12.1.1.1 Custom Design With WEBENCH® Tools

Click [here](#) to create a custom design using the LM33620 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation see the following:

- [Thermal Design by Insight not Hindsight](#)
- [A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages](#)
- [Semiconductor and IC Package Thermal Metrics](#)
- [Thermal Design Made Simple with LM43603 and LM43602](#)
- [SLMA002 PowerPAD™ Thermally Enhanced Package](#)
- [PowerPAD™ Made Easy](#)
- [SBVA025 Using New Thermal Metrics](#)
- [Layout Guidelines for Switching Power Supplies](#)
- [Simple Switcher PCB Layout Guidelines](#)
- [Construction Your Power Supply- Layout Considerations](#)
- [Low Radiated EMI Layout Made Simple with LM4360x and LM4600x](#)

#### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.  
SIMPLE SWITCHER, WEBENCH are registered trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

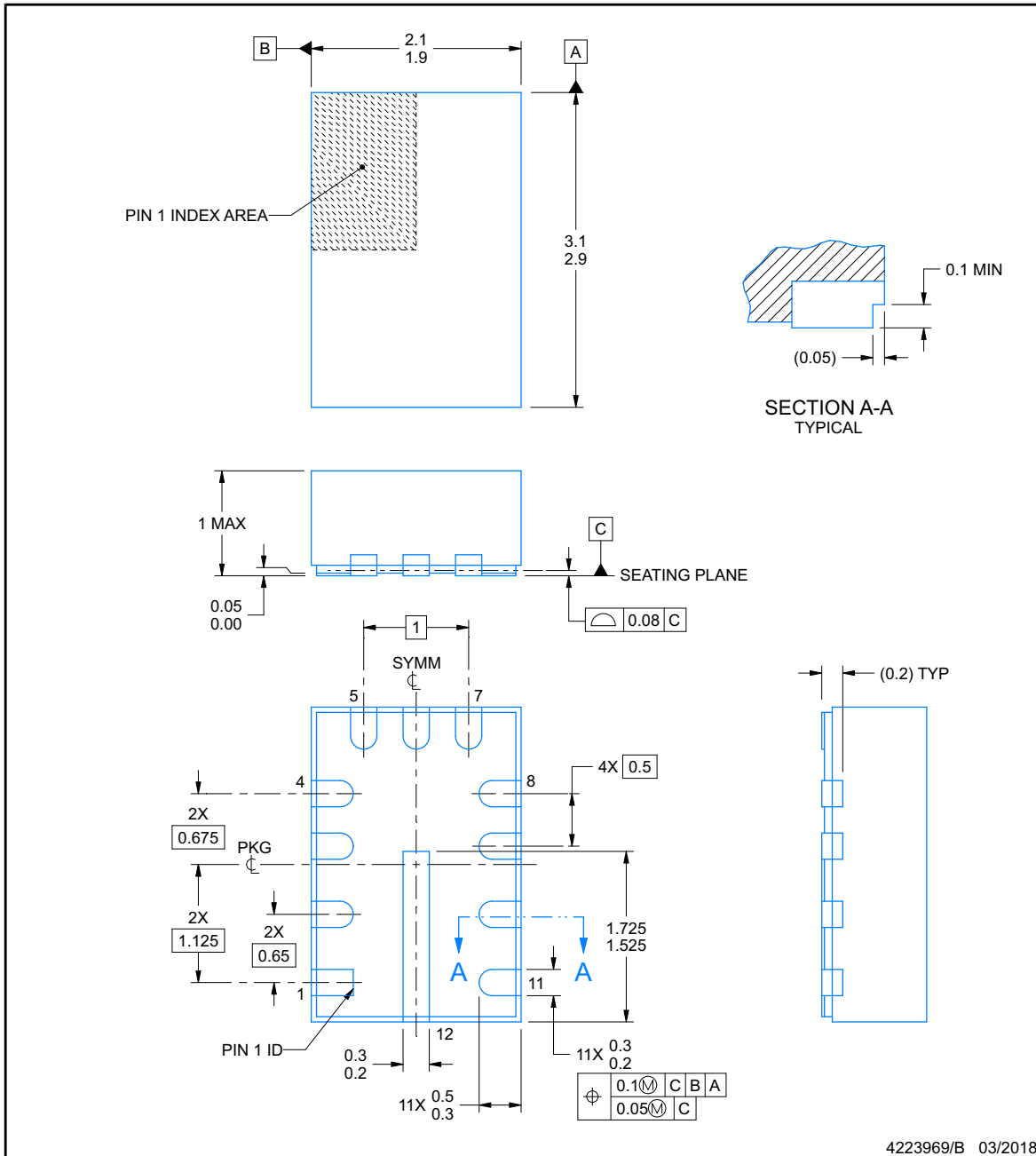


**PACKAGE OUTLINE**

**RNX0012B**

**VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

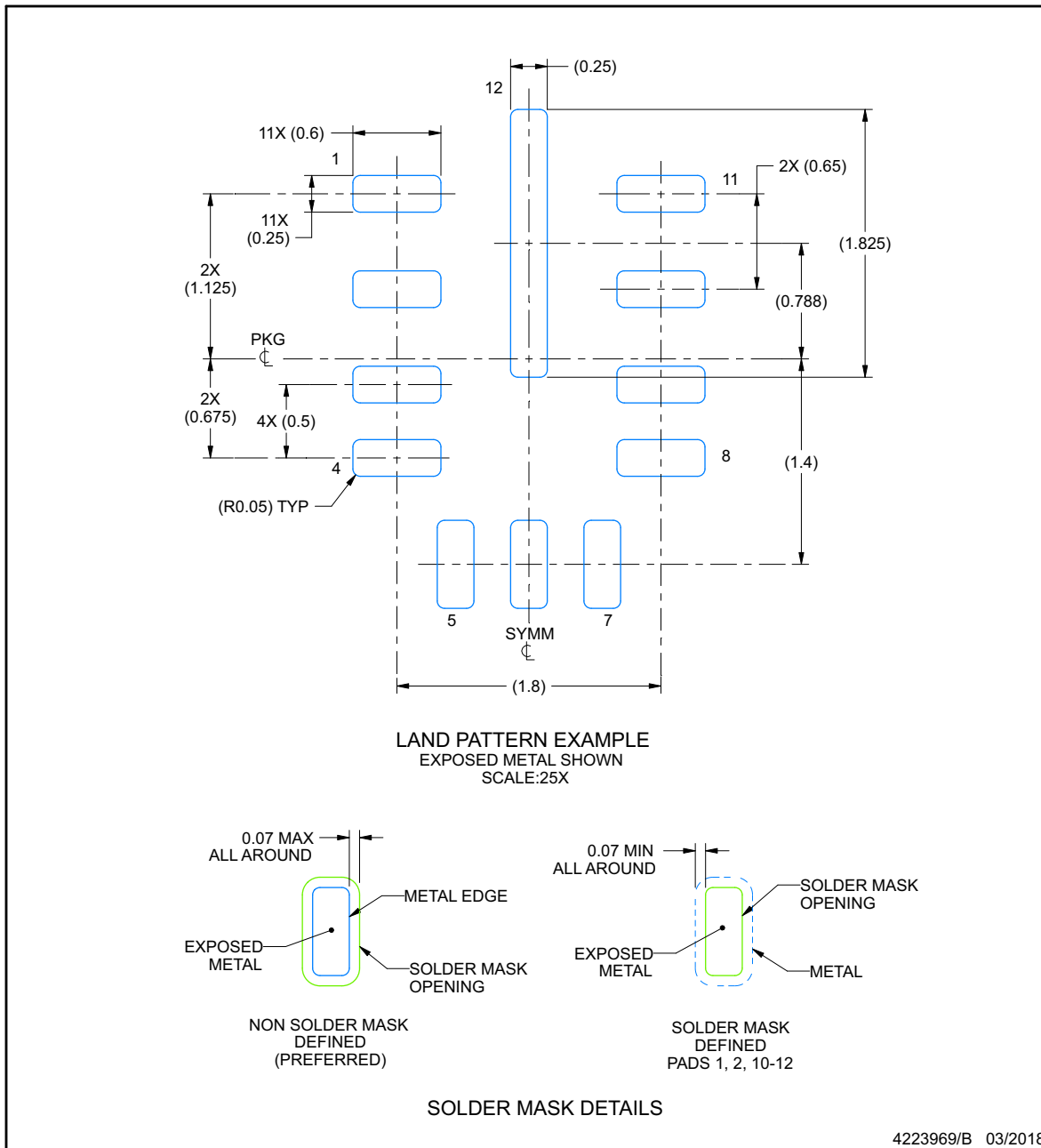
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**EXAMPLE BOARD LAYOUT**

**RNX0012B**

**VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

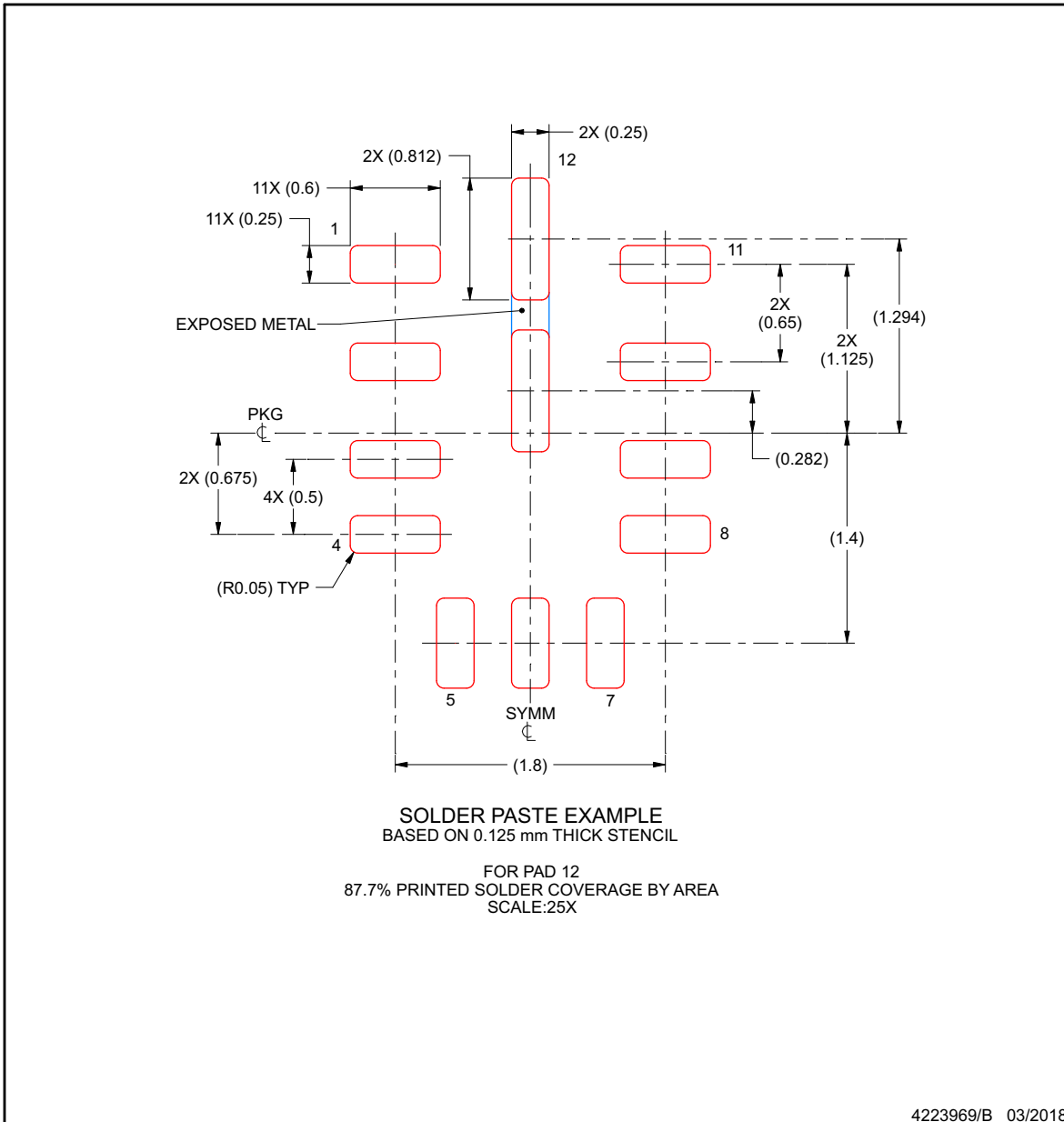
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

**EXAMPLE STENCIL DESIGN**

**RNX0012B**

**VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR33620ADDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33620A	<a href="#">Samples</a>
LMR33620ADDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33620A	<a href="#">Samples</a>
LMR33620ARNXR	ACTIVE	VQFN-HR	RNX	12	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	33620A	<a href="#">Samples</a>
LMR33620ARNXT	ACTIVE	VQFN-HR	RNX	12	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	33620A	<a href="#">Samples</a>
LMR33620BDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33620B	<a href="#">Samples</a>
LMR33620BDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33620B	<a href="#">Samples</a>
LMR33620BRNXR	ACTIVE	VQFN-HR	RNX	12	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	33620B	<a href="#">Samples</a>
LMR33620BRNXT	ACTIVE	VQFN-HR	RNX	12	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	33620B	<a href="#">Samples</a>
LMR33620CDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33620C	<a href="#">Samples</a>
LMR33620CDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33620C	<a href="#">Samples</a>
LMR33620CRNXR	ACTIVE	VQFN-HR	RNX	12	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	33620C	<a href="#">Samples</a>
LMR33620CRNXT	ACTIVE	VQFN-HR	RNX	12	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	33620C	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

---

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

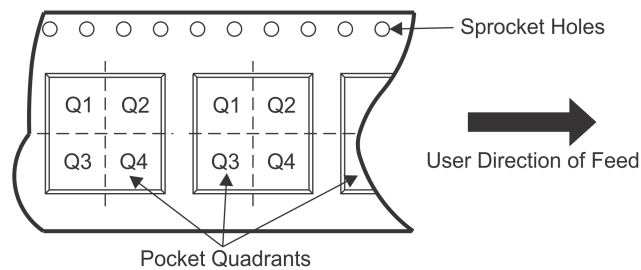
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

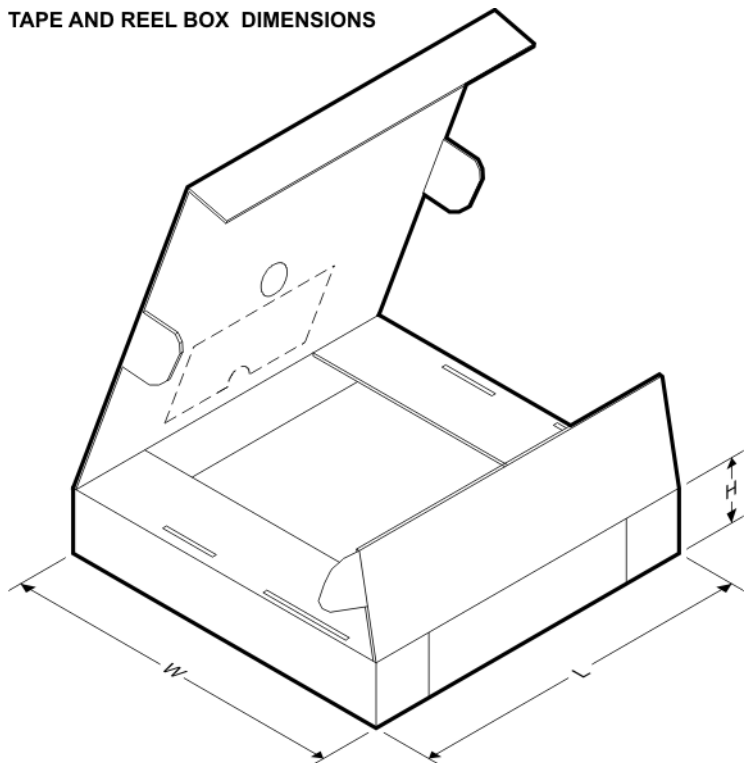
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

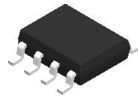
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR33620ADDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR33620ARNXR	VQFN-HR	RNX	12	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LMR33620ARNXT	VQFN-HR	RNX	12	250	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LMR33620BDDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR33620BRNXR	VQFN-HR	RNX	12	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LMR33620BRNXT	VQFN-HR	RNX	12	250	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LMR33620CDDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR33620CRNXR	VQFN-HR	RNX	12	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LMR33620CRNXT	VQFN-HR	RNX	12	250	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR33620ADDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR33620ARNXR	VQFN-HR	RNX	12	3000	195.0	200.0	45.0
LMR33620ARNXT	VQFN-HR	RNX	12	250	195.0	200.0	45.0
LMR33620BDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR33620BRNXR	VQFN-HR	RNX	12	3000	195.0	200.0	45.0
LMR33620BRNXT	VQFN-HR	RNX	12	250	195.0	200.0	45.0
LMR33620CDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR33620CRNXR	VQFN-HR	RNX	12	3000	195.0	200.0	45.0
LMR33620CRNXT	VQFN-HR	RNX	12	250	195.0	200.0	45.0

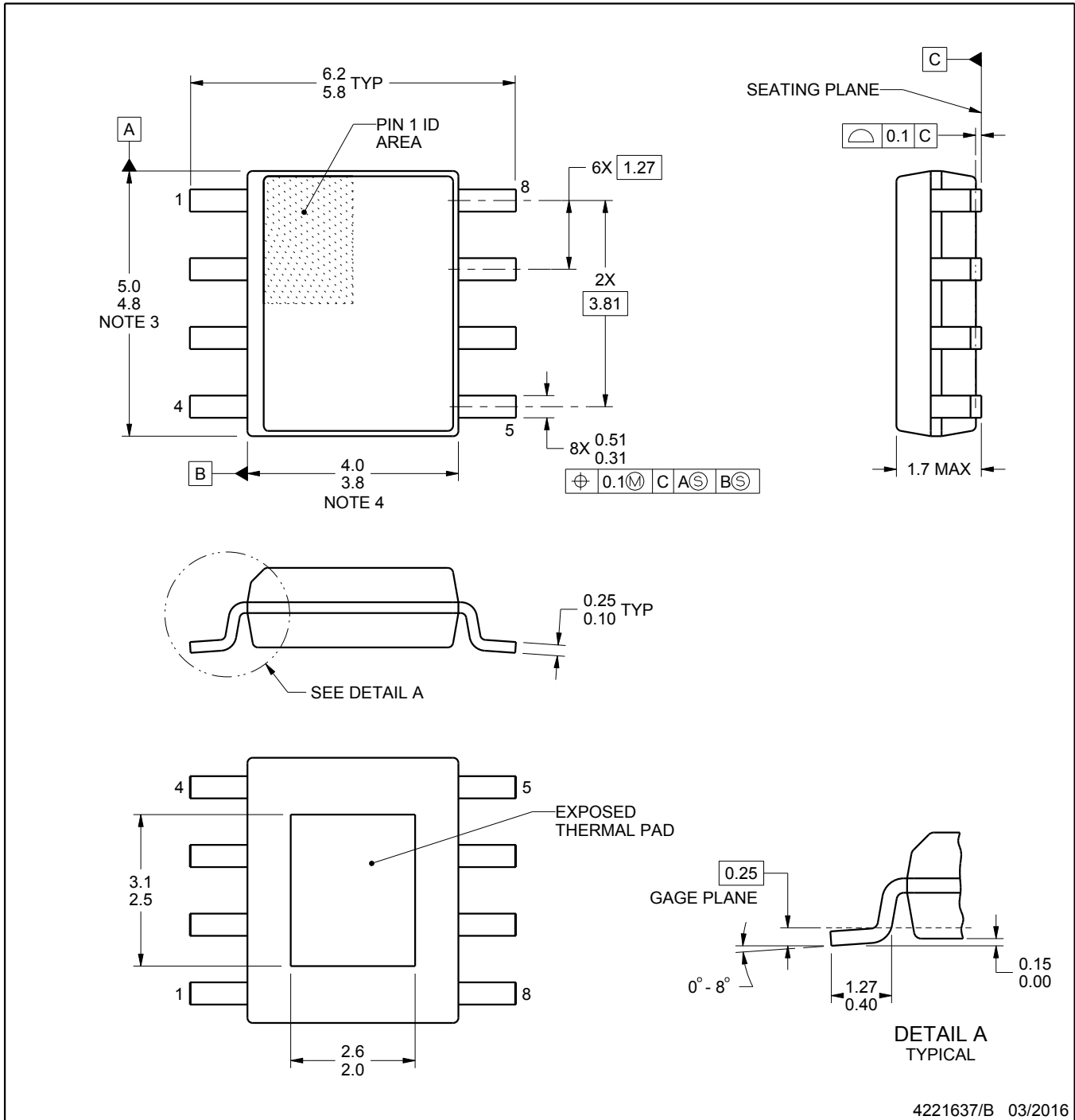
DDA0008J



# PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4221637/B 03/2016

PowerPAD is a trademark of Texas Instruments.

**NOTES:**

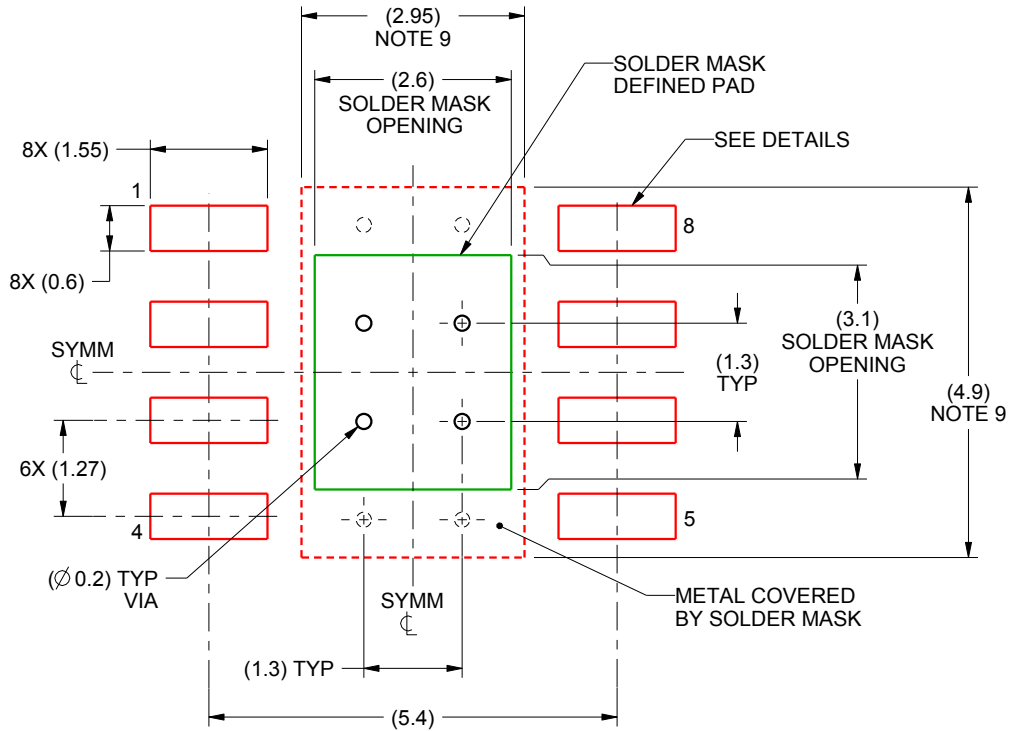
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

# EXAMPLE BOARD LAYOUT

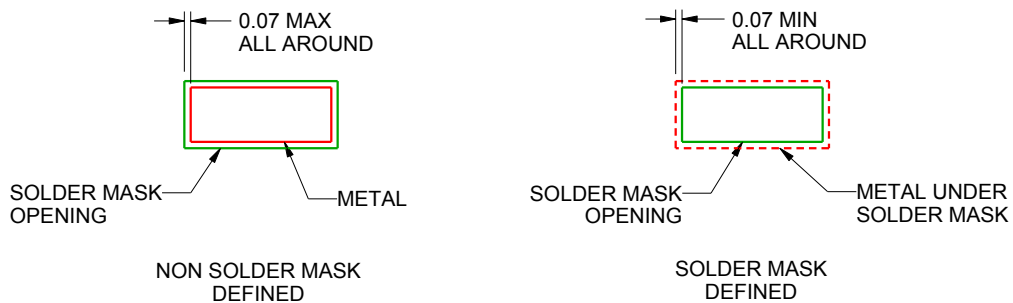
DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

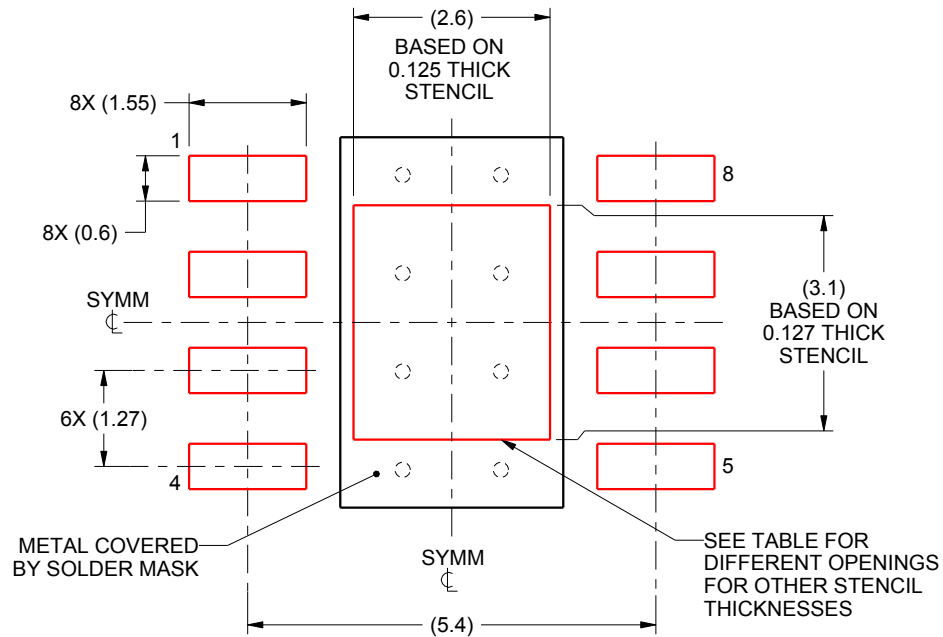
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
- 9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
 EXPOSED PAD  
 100% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

- 10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 11. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.