

## LMP7312 Precision SPI-Programmable AFE with Differential/Single-Ended Input/Output

Check for Samples: [LMP7312](#)

### FEATURES

- Typical Values,  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ .
- Gain bandwidth 1 MHz
- Input voltage range ( $G = 0.096 \text{ V/V}$ ) -15V to +15V
- Core op-amp input offset voltage 100  $\mu\text{V}$  (max)
- Supply current 2 mA (max)
- Gain (Attenuation Mode) 0.096 V/V, 0.192 V/V, 0.384 V/V, 0.768 V/V
- Gain (Amplification Mode) 1 V/V, 2 V/V
- Gain Error 0.035% (max)
- Core op-amp PSRR 90 dB (min)
- CMRR 80 dB (min)
- Adjustable output common mode 1V to 4V

- Temperature range  $-40$  to  $125^\circ\text{C}$
- Package 14-Pin SOIC

### APPLICATIONS

- Signal conditioning AFE
  - $\pm 10\text{V}$ ;  $\pm 5\text{V}$ ; 0-5V; 0-10V; 0-20mA; 4-20mA
- Data Acquisition systems
- Motor control
- Instrument and process control
- Remote sensing
- Programmable automation control

### DESCRIPTION

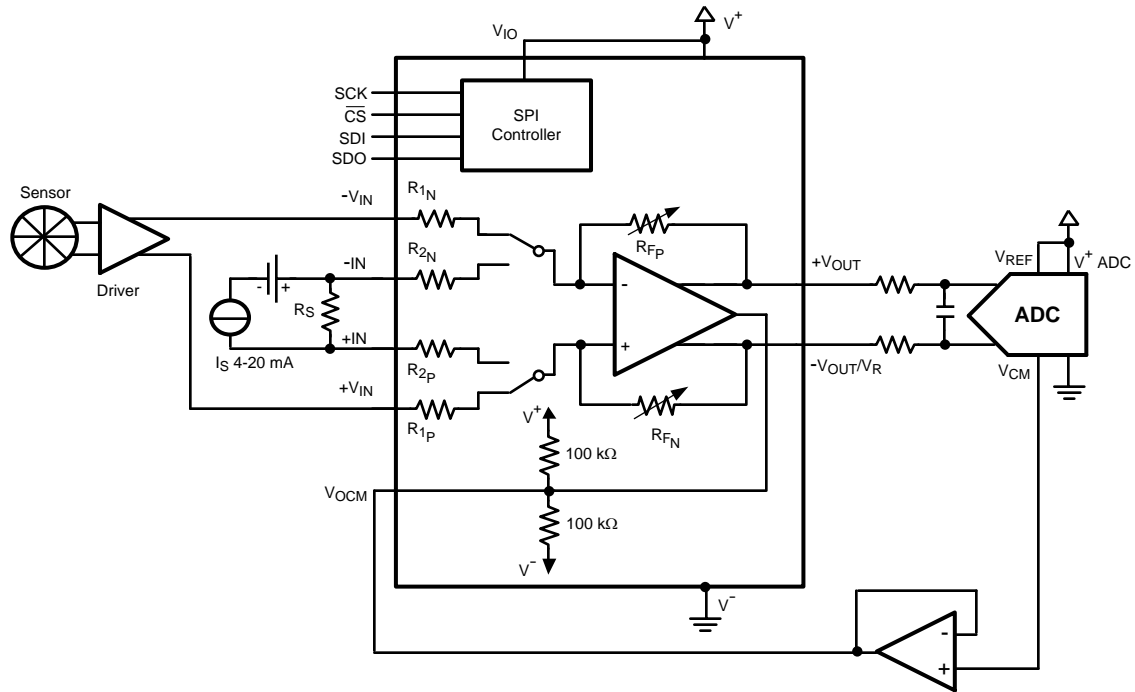
The LMP7312 is a digitally programmable variable gain amplifier/attenuator. Its wide input voltage range and superior precision make it a prime choice for applications requiring high accuracy such as data acquisition systems for IO modules in programmable logic control (PLC). The LMP7312 provides a differential output to maximize dynamic range and signal to noise ratio, thereby reducing the overall system error. It can also be configured to handle single ended input data converters by means of the  $V_{\text{OCM}}$  pin (see application section for details). The inputs of LMP7312 can be configured in attenuation mode to handle large input signals of up to +/- 15V, as well as in amplification mode to handle current loops of 0-20mA and 4-20mA. The LMP7312 is equipped with a null switch to evaluate the offset of the internal amplifier. A guaranteed 0.035% maximum gain error (for all gains) and a maximum gain drift of 5ppm over the extended industrial temperature range ( $-40^\circ$  to  $125^\circ\text{C}$ ) make the LMP7312 very attractive for high precision systems even under harsh conditions. A low input offset voltage of 100 $\mu\text{V}$  and low voltage noise of 3 $\mu\text{Vpp}$  give the LMP7312 a superior performance. The LMP7312 is fully specified from  $-40^\circ$  to  $125^\circ\text{C}$  and is available in SOIC-14 package.



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### Typical Application



LMP™ is a trademark of National Semiconductor Corporation.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)</sup>

ESD Rating <sup>(2)</sup>	
Human Body Model	2000V
Machine Body Model	150V
Charge device Model	1000V
Analog Supply Voltage ( $V_S = V^+ - V^-$ )	6V
Digital Supply Voltage ( $V_{DIO} = V_{IO} - V^-$ )	6V
Attenuation pins $-V_{IN}$ , $+V_{IN}$ referred to $V^-$	$\pm 17.5V$
Amplification pins $-IN$ , $+IN$ referred to $V^-$	$\pm 10V$
Voltage at all other pins referred to $V^-$	6V
Storage Temperature Range	$-65^\circ C$ to $150^\circ C$
For soldering specification: see product folder at <a href="http://www.national.com">www.national.com</a> and <a href="http://www.national.com/ms/MS/MS-SOLDERING.pdf">www.national.com/ms/MS/MS-SOLDERING.pdf</a>	
Junction Temperature	$150^\circ C$

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but for which specific performance is not guaranteed. For guaranteed specifications and the test conditions, see Electrical Characteristics.
- (2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

### Operating Ratings <sup>(1)</sup>

Analog Supply Voltage ( $V_S = V^+ - V^-$ ), $V^- = 0V$	4.5V to 5.5V
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- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but for which specific performance is not guaranteed. For guaranteed specifications and the test conditions, see Electrical Characteristics.

**Operating Ratings <sup>(1)</sup> (continued)**

Digital Supply Voltage ( $V_{DIO} = V_{IO} - V^-$ ), $V^- = 0V$	2.7V to 5.5V
Attenuation pins $-V_{IN}$ , $+V_{IN}$ referred to $V^-$	-15V to 15V
Amplification pins $-IN$ , $+IN$ referred to $V^-$	-2.35V to 7.35V
Temperature Range <sup>(2)</sup>	-40°C to 125°C
Package Thermal Resistance <sup>(2)</sup>	
SOIC-14	145°C/W

(2) The maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is:  $PD(\max) = (T_J(\max) - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board.

## 5V Electrical Characteristics <sup>(1)</sup>

Unless otherwise specified, all limits guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V_{IO} = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $G = 0.192\text{ V/V}$ ,  $V_{\text{CM\_ATT}} = (+V_{\text{IN}} + (-V_{\text{IN}}))/2$ ,  $V_{\text{CM\_AMP}} = (+\text{IN} + (-\text{IN}))/2$ . Differential output configuration. SE = Single Ended Output, DE = Differential Output. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$V_{\text{OS}}$	Core op-amp Input Offset Voltage	Nulling Switch Mode, DE, $V_{\text{OCM}} = 1\text{V}$ ; Nulling switch Mode, SE, $-V_{\text{OUT}}/V_{\text{R}} = 1\text{V}$	-100 <b>-250</b>		100 <b>250</b>	$\mu\text{V}$
		Nulling Switch Mode, DE, $V_{\text{OCM}} = 4\text{V}$ ; Nulling Switch Mode, SE, $-V_{\text{OUT}}/V_{\text{R}} = 4\text{V}$	-100 <b>-250</b>		100 <b>250</b>	
$\text{TCV}_{\text{OS}}$	Core op-amp Input Offset Voltage <sup>(4)</sup>	Nulling Switch Mode, DE, $V_{\text{OCM}} = 1\text{V}$ ; Nulling Switch Mode, SE, $-V_{\text{OUT}}/V_{\text{R}} = 1\text{V}$	-3	$\pm 1.5$	3	$\mu\text{V}/^\circ\text{C}$
		Nulling Switch Mode, DE, $V_{\text{OCM}} = 4\text{V}$ ; Nulling Switch Mode, SE, $-V_{\text{OUT}}/V_{\text{R}} = 4\text{V}$	-3	$\pm 1.5$	3	
$A_{\text{v}}$	Gain Error	All gains, $R_{\text{L}} = 10\text{ k}\Omega$ , $C_{\text{L}} = 50\text{ pF}$ , SE / DE	-0.035 <b>-0.045</b>		0.035 <b>0.045</b>	%
	Gain Drift	SE / DE	-5	$\pm 1$	5	$\text{ppm}/^\circ\text{C}$
$e_{\text{n}}$	Core op-amp Voltage Noise Density	RTI, Nulling Switch Mode, $f = 10\text{ kHz}$		7.25		$\text{nV}/\sqrt{\text{Hz}}$
	Core op-amp Peak to Peak Voltage Noise	RTI, Nulling Switch Mode, $f = 0.1\text{Hz}$ to $10\text{Hz}$		3		$\mu\text{V}_{\text{PP}}$
$I_{\text{VA}}$	Analog Supply Current	$+V_{\text{IN}} = -V_{\text{IN}} = V_{\text{OCM}}$			<b>2</b>	$\text{mA}$
$I_{\text{VIO}}$	Digital Supply Current	Without any load connected to SDO pin			<b>120</b>	$\mu\text{A}$
$R_{\text{IN\_CM}}$	CM Input Resistance	$G = 0.192\text{ V/V}$		62.08		$\text{k}\Omega$
		$G = 1\text{ V/V}$		40		
$R_{\text{IN\_DIFF}}$	Differential Input Resistance	$G = 0.192\text{ V/V}$		248.3		$\text{k}\Omega$
		$G = 1\text{ V/V}$		160		
$\text{CMRR}$	DC Common Mode Rejection Ratio	$G = 0.096\text{V/V}$ , $-15\text{V} < V_{\text{CM\_ATT}} < 15\text{V}$ , SE / DE	80 <b>77</b>			$\text{dB}$
		$G = 0.192\text{V/V}$ , $-11.4\text{V} < V_{\text{CM\_ATT}} < 15\text{V}$ , SE / DE				
		$G = 0.384\text{V/V}$ , $-6\text{V} < V_{\text{CM\_ATT}} < 11\text{V}$ , SE / DE				
		$G = 0.768\text{V/V}$ , $-3\text{V} < V_{\text{CM\_ATT}} < 8\text{V}$ , SE / DE				
		$G = 1\text{V/V}$ , $-2.3\text{V} < V_{\text{CM\_AMP}} < 7.3\text{V}$ , SE / DE				
		$G = 2\text{V/V}$ , $-1.15\text{V} < V_{\text{CM\_AMP}} < 6.15\text{V}$ , SE / DE.				
$\text{PSRR}$	Core op-amp DC Power Supply Rejection Ratio	Nulling Switch Mode, $4.5\text{V} < V^+ < 5.5\text{V}$	90			$\text{dB}$
$V_{\text{OCM\_OS}}$	$V_{\text{OCM}}$ Output Offset <sup>(5)</sup>	$V_{\text{OCM}} = 2.5\text{ V}$	<b>-20</b>		<b>20</b>	$\text{mV}$
$V_{\text{OUT}}$	Positive Output Voltage Swing	$R_{\text{L}} = 10\text{ k}\Omega$ , $C_{\text{L}} = 50\text{ pF}$ , $+V_{\text{IN}} = 15\text{V}$ , $-V_{\text{IN}} = -15\text{V}$			$V^+ - 0.2$	$\text{V}$
	Negative Output Voltage Swing	$R_{\text{L}} = 10\text{ k}\Omega$ , $C_{\text{L}} = 50\text{ pF}$ , $+V_{\text{IN}} = -15\text{V}$ , $-V_{\text{IN}} = 15\text{V}$		$V^- + 0.2$		
$I_{\text{OUT}}$	Short circuit current	$+V_{\text{IN}} = -V_{\text{IN}} = 2.5\text{V}$ , $+V_{\text{OUT}}$ , $-V_{\text{OUT}}/V_{\text{R}}$ connected individually to either $V^+$ or $V^-$	10			$\text{mA}$
	Current limitation	Internal current limiter			55	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_{\text{J}} = T_{\text{A}}$ . No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_{\text{J}} > T_{\text{A}}$ .

(2) All limits are guaranteed by testing, design, or statistical analysis.

(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(4) Offset voltage temperature drift is determined by dividing the change in  $V_{\text{OS}}$  at the temperature extremes by the total temperature change.

(5)  $V_{\text{OCM\_OS}}$  is the difference between the Output Common mode voltage  $(+V_{\text{OUT}} + (-V_{\text{OUT}}/V_{\text{R}}))/2$  and the Voltage on the  $V_{\text{OCM}}$  pin.

**5V Electrical Characteristics <sup>(1)</sup> (continued)**

Unless otherwise specified, all limits guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V_{IO} = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $G = 0.192\text{ V/V}$ ,  $V_{CM\_ATT} = (+V_{IN} + (-V_{IN}))/2$ ,  $V_{CM\_AMP} = (+IN + (-IN))/2$ . Differential output configuration. SE = Single Ended Output, DE = Differential Output. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
GBW	Bandwidth	Attenuation Mode, $G = 0.096\text{ V/V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$		1.2		MHz
		Attenuation Mode, $G = 0.192\text{ V/V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$		1.0		
		Attenuation Mode, $G = 0.384\text{ V/V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$		560		kHz
		Attenuation Mode, $G = 0.768\text{ V/V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$		310		
		Amplification Mode, $G = 1\text{ V/V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$		530		kHz
		Amplification Mode, $G = 2\text{ V/V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$		280		
SR	Slew Rate	$R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$ (6)		1.4		V/ $\mu\text{sec}$
THD+N	Total Harmonic Distorsion + Noise	$V_{out} = 4.096\text{ Vpp}$ , $f = 1\text{ KHz}$ , $R_L = 10\text{ k}\Omega$		0.0026		%

(6) The number specified is the average of rising and falling slew rates and is measured at 90% to 10%.

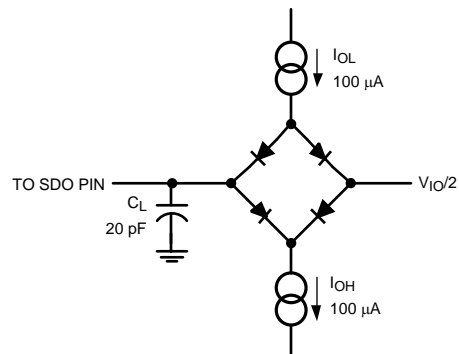
## Electrical Characteristics (Serial Interface) <sup>(1)</sup>

Unless otherwise specified. All limits guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $2.7\text{V} < V_{IO} < 5.5\text{V}$

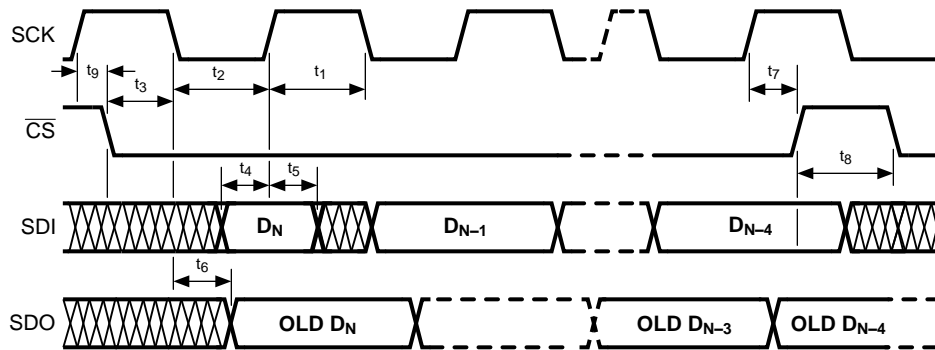
Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
VIL	Input Logic Low Threshold				0.8	V
VIH	Input Logic High Threshold (SDO pin)		2			V
VOL	Output logic Low Threshold (SDO pin)	$I_{SDO} = 100\mu\text{A}$			0.2	V
		$I_{SDO} = 2\text{mA}$			0.4	
VOH	Output logic High Threshold	$I_{SDO} = 100\mu\text{A}$	$V_{IO} - 0.2$			V
		$I_{SDO} = 2\text{mA}$	$V_{IO} - 0.6$			
$t_1$	High Period, SCK	(4)	100			ns
$t_2$	Low Period, SCK	(4)	100			ns
$t_3$	Set Up Time, $\overline{\text{CS}}$ to SCK	(4)	50			ns
$t_4$	Set Up Time, SDI to SCK	(4)	30			ns
$t_5$	Hold Time, SCK to SDI	(4)	10			ns
$t_6$	Prop. Delay, SCK to SDO	(4)			60	ns
$t_7$	Hold Time, SCK Transition to $\overline{\text{CS}}$ Rising Edge	(4)	50			ns
$t_8$	$\overline{\text{CS}}$ Inactive	(4)	100			ns
$t_9$	Hold Time, SCK Transition to $\overline{\text{CS}}$ Falling Edge	(4)	10			ns
$t_R/t_F$	Signal Rise and Fall Times	(4)	1.5		5	ns

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ .
- (2) All limits are guaranteed by testing, design, or statistical analysis.
- (3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (4) Load for these tests is shown in the Test Circuit Diagram.

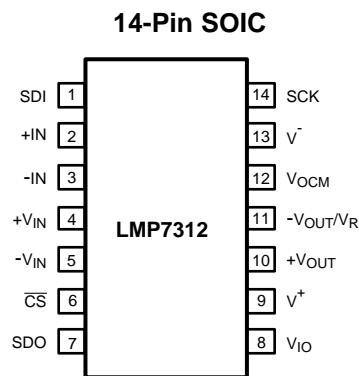
## Test Circuit Diagram



## Timing Diagram



## Connection Diagram



**Figure 1. Top View**

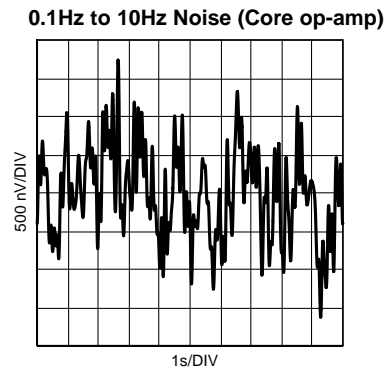
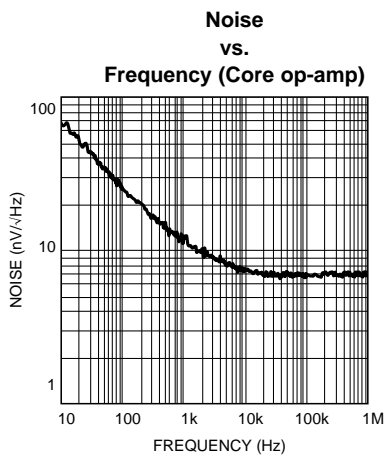
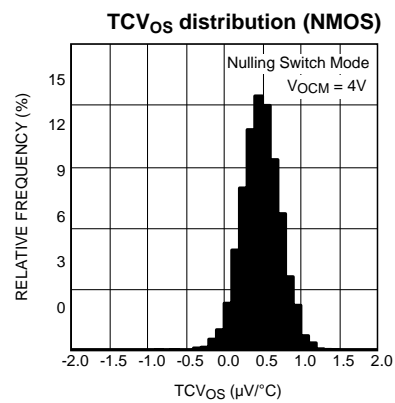
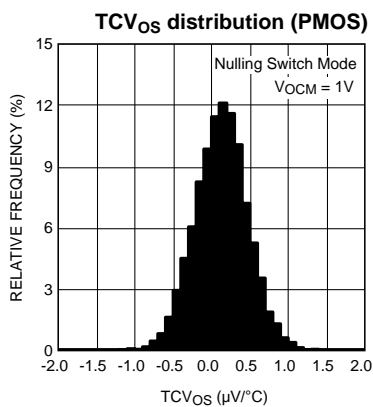
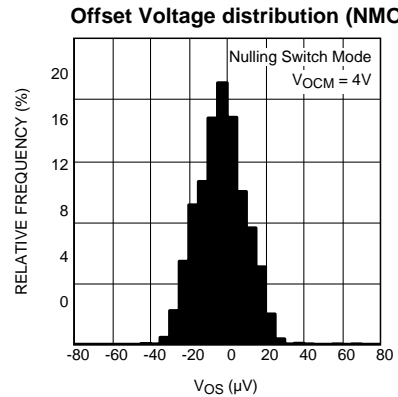
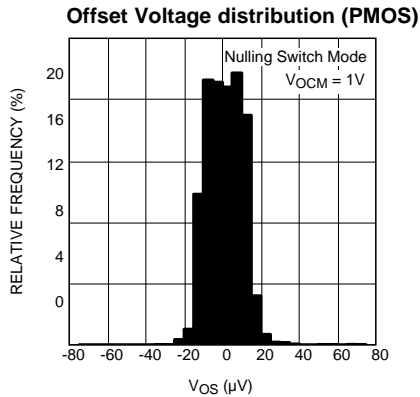
## Pin Functions

### Pin Descriptions

Pin	Name	Description
1	SDI	SPI data IN
2	+IN	Non-inverting input of Amplification pair
3	-IN	Inverting input of Amplification pair
4	+VIN	Non-inverting input of Attenuation pair
5	-VIN	Inverting input of Attenuation pair
6	$\overline{\text{CS}}$	SPI chip select
7	SDO	SPI data OUT
8	V <sub>IO</sub>	SPI supply voltage
9	V <sup>+</sup>	Positive supply voltage
10	+V <sub>OUT</sub>	Non-inverting output
11	-V <sub>OUT</sub> /V <sub>R</sub>	Inverting output in differential output mode, reference input in single-ended operation mode
12	V <sub>OCM</sub>	Output common mode voltage in DE
13	V <sup>-</sup>	Negative supply voltage, reference for both Analog and Digital supplies
14	SCK	SPI Clock

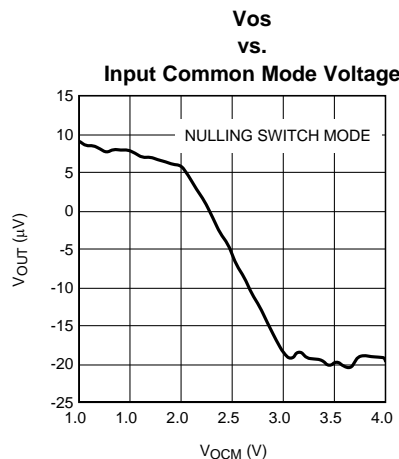
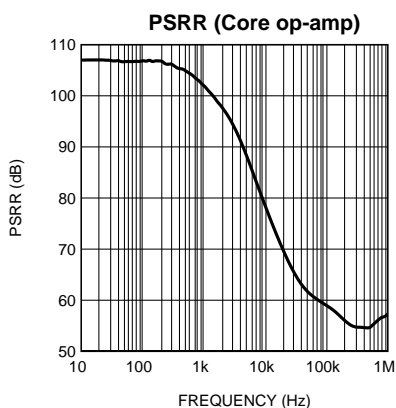
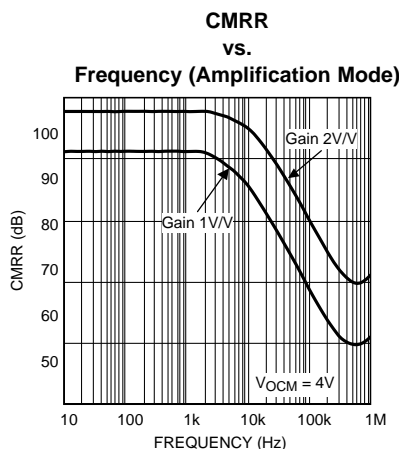
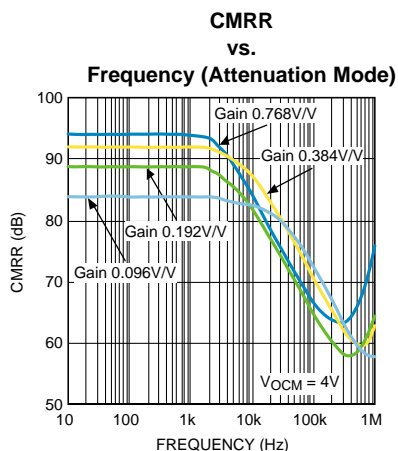
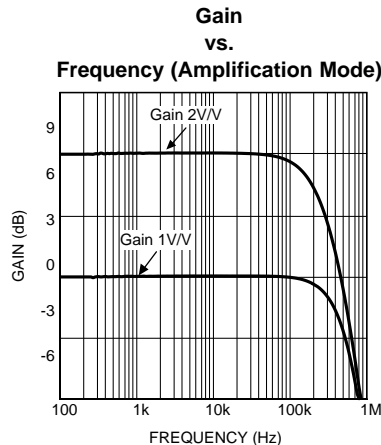
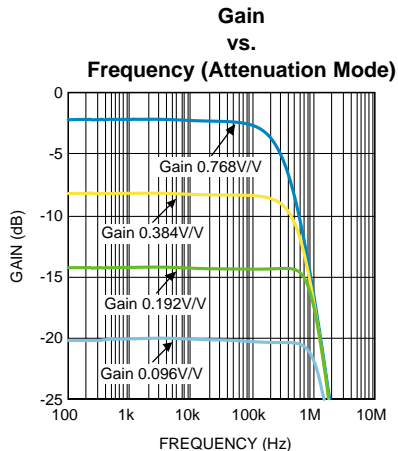
### Typical Performance Characteristics

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V_{IO} = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM\_ATT} = (+V_{IN} + (-V_{IN}))/2$ ,  $V_{CM\_AMP} = (+IN + (-IN))/2$ .  $R_L = 10\text{k}\Omega$ ,  $C_L = 50\text{pF}$ , Differential output configuration.



Typical Performance Characteristics (continued)

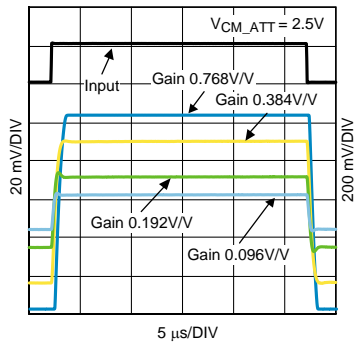
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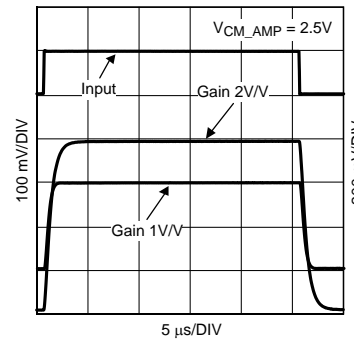
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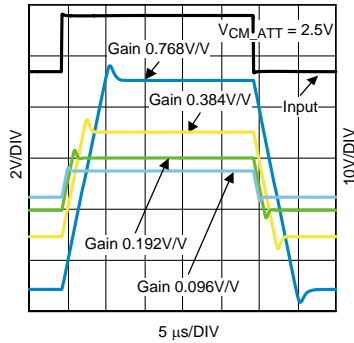
**Small signal step (Attenuation Mode)**



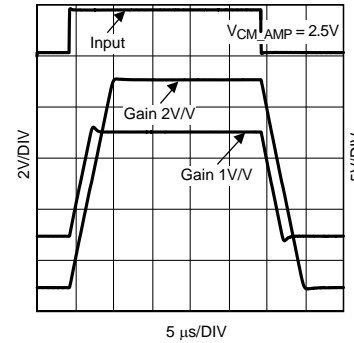
**Small signal step (Amplification Mode)**



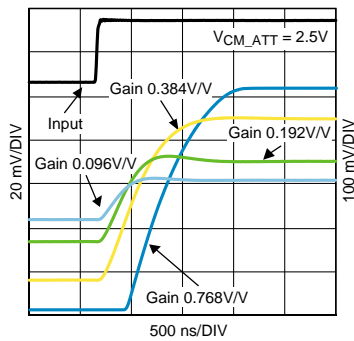
**Large signal step (Attenuation Mode)**



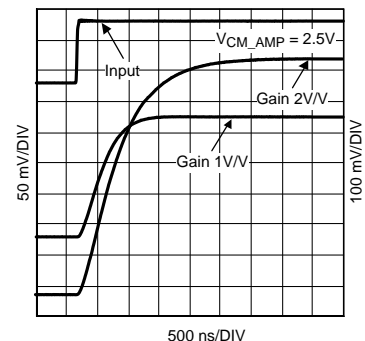
**Large signal step (Amplification Mode)**



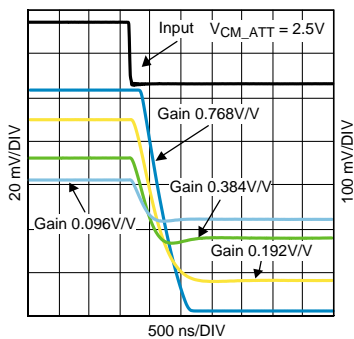
**Settling time – Rise (Attenuation Mode)**



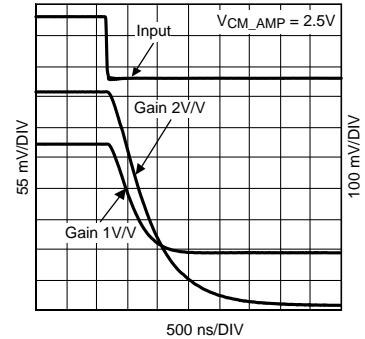
**Settling time – Rise (Amplification Mode)**



**Settling time – Fall (Attenuation Mode)**



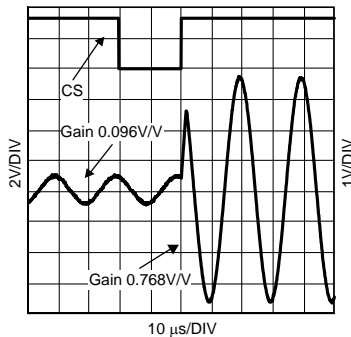
**Settling time – Fall (Amplification Mode)**



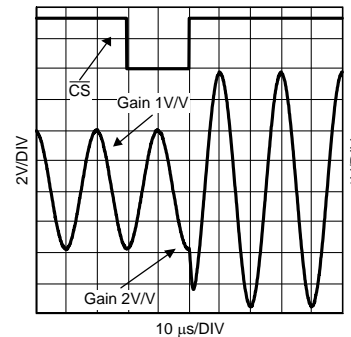
### Typical Performance Characteristics (continued)

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V_{IO} = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM\_ATT} = (+V_{IN} + (-V_{IN}))/2$ ,  $V_{CM\_AMP} = (+IN + (-IN))/2$ .  $R_L = 10\text{k}\Omega$ ,  $C_L = 50\text{pF}$ , Differential output configuration.

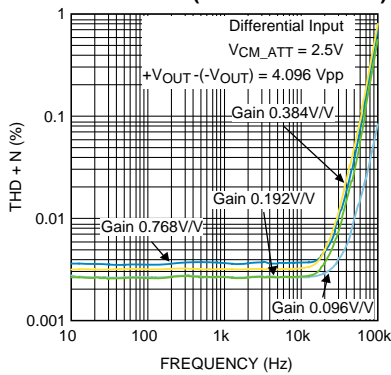
Gain change (Attenuation Mode)



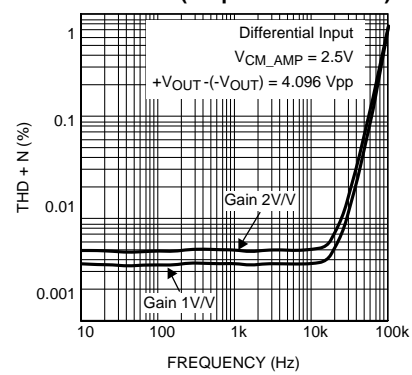
Gain change (Amplification Mode)



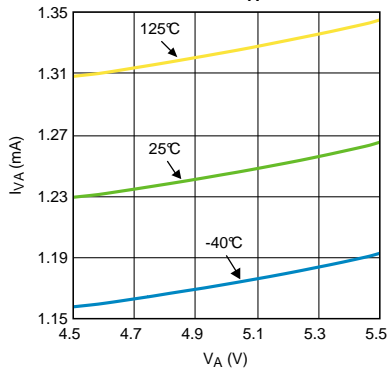
THD + N (Attenuation Mode)



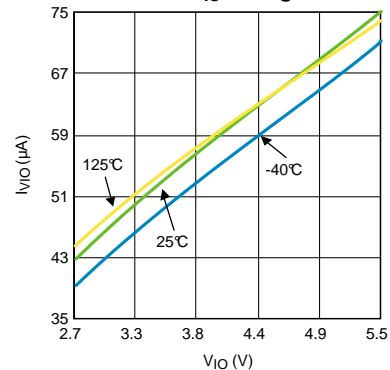
THD + N (Amplification Mode)



$I_{VA}$   
vs.  
 $V_A$



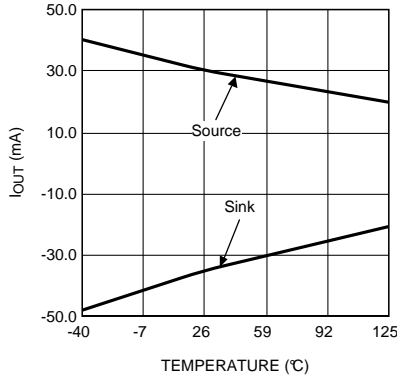
$I_{VIO}$   
vs.  
 $V_{IO}$  Voltage



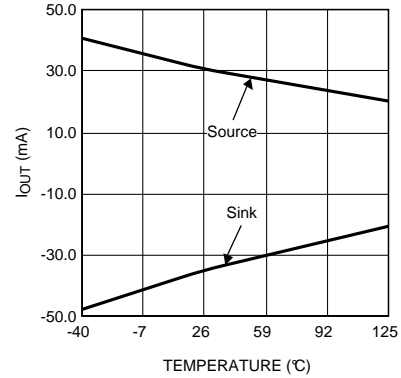
### Typical Performance Characteristics (continued)

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V_{IO} = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM\_ATT} = (+V_{IN} + (-V_{IN}))/2$ ,  $V_{CM\_AMP} = (+IN + (-IN))/2$ .  $R_L = 10\text{k}\Omega$ ,  $C_L = 50\text{pF}$ , Differential output configuration.

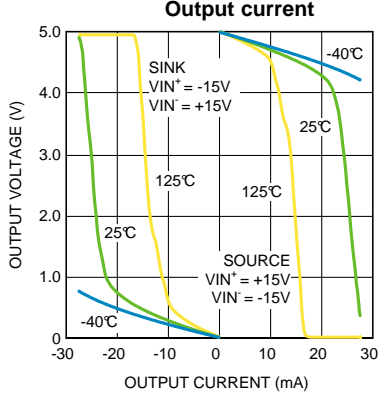
**Short Circuit Current +V<sub>OUT</sub>**  
vs.  
**Temperature**



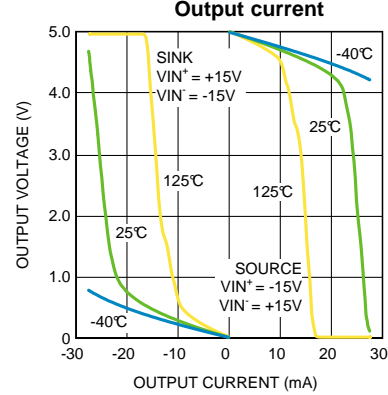
**Short Circuit Current -V<sub>OUT</sub>**  
vs.  
**Temperature**



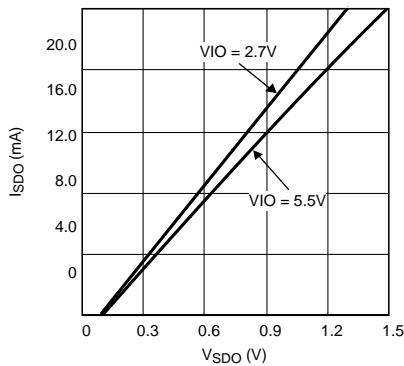
**Output voltage swing +V<sub>OUT</sub>**  
vs.  
**Output current**



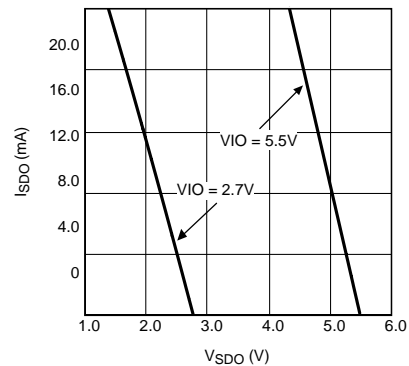
**Output voltage swing -V<sub>OUT</sub>**  
vs.  
**Output current**



**SDO sink current**  
vs.  
**SDO Voltage**



**SDO source current**  
vs.  
**SDO Voltage**



## Application Section

### GENERAL DESCRIPTION

The LMP7312 is a single supply programmable gain difference amplifier with two input pairs: Attenuation pair ( $-V_{IN}$ ,  $+V_{IN}$ ) and Amplification pair ( $-IN$ ,  $+IN$ ). The output can be configured in both single-ended and differential modes with the output common mode voltage set by the user. The input selection, the gains and the mode of operation of the LMP7312 are controlled through a 4-wire SPI interface (SCK,  $\overline{CS}$ , SDI, SDO). These features combined make the LMP7312 a very easy interface between the analog high voltage industrial buses and the low voltage digital converters.

### OUTPUT MODE CONFIGURATION

The LMP7312 is able to work in both single ended and differential output mode. The selection of the mode is made through the  $V_{OCM}$  (output common mode voltage) pin.

#### Differential Output

This mode of operation is enabled when the output common mode voltage pin ( $V_{OCM}$ ) is connected to a voltage higher than 1V, for instance the common mode voltage supplied by an ADC, (Figure 2) or a voltage reference. If the  $V_{OCM}$  pin is floating an internal voltage divider biases it at the half supply voltage. In this configuration the output signals are set on the  $V_{OCM}$  voltage level.

#### Single-Ended Output

This mode of operation is enabled when the  $V_{OCM}$  pin is tied to a voltage less than 0.5 V, for example to ground. In this mode of operation the LMP7312 behaves as a difference amplifier, where the  $+V_{OUT}$  pin is the single-ended output while the  $-V_{OUT}/V_R$  is the reference voltage.

1. In the case of bipolar input signal the non inverting output will be connected to an external reference through a buffer (Figure 3).
2. In the case of unipolar input signal the non inverting output will be connected to ground (Figure 4).

In both cases the inverting output pin is configured as an input pin.

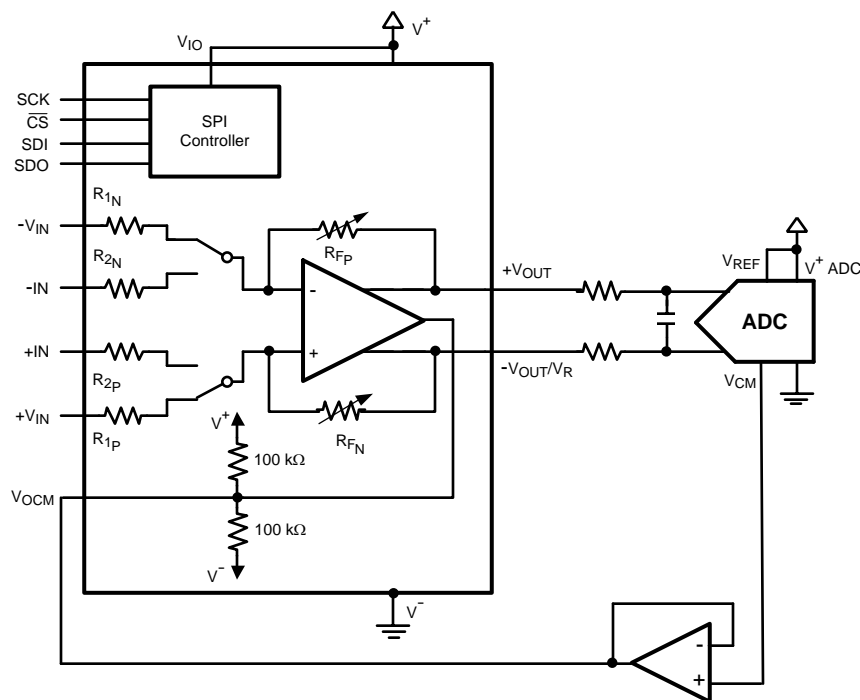


Figure 2. Differential ADC Interfacing with  $V_{CM}$  provided by the ADC

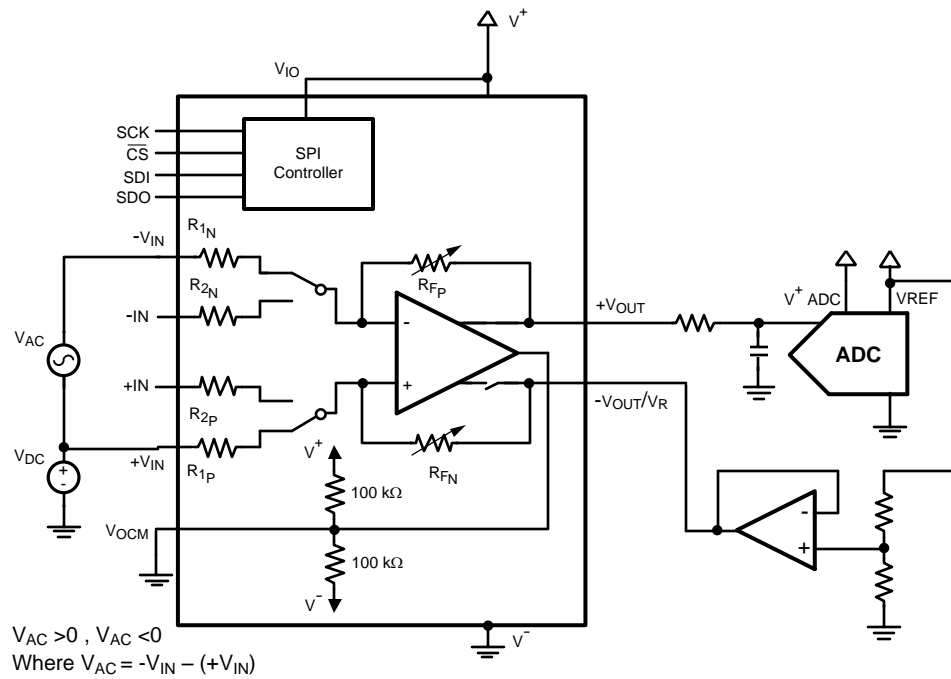


Figure 3. Bipolar Input Signal to Single-Ended ADC Interface

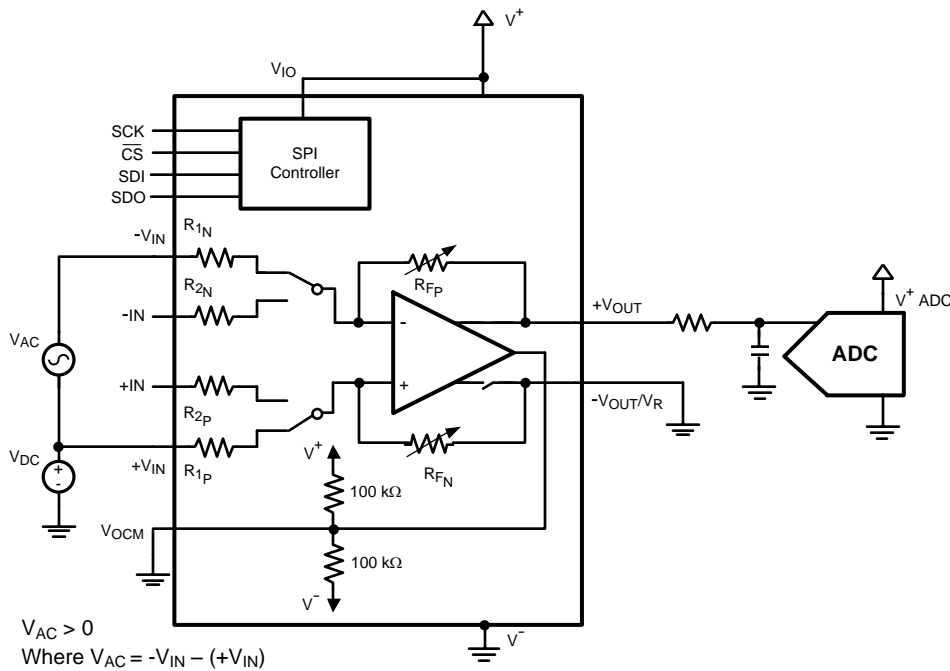


Figure 4. Unipolar Input Signal to Single-Ended ADC Interface

**INPUT VOLTAGE RANGE**

The LMP7312 has an internal OpAmp with rail-to-rail input voltage range capability. The requirement to stay within the  $V^-$  and  $V^+$  rail at the OpAmp input translates in an Input Voltage Range specification as explained in this application section.

### Differential Output

Considering a single positive supply ( $V^- = \text{GND}$ ,  $V^+ = V_S$ ) the Input Common mode voltage,  $V_{\text{CM\_ATT}} = (+V_{\text{IN}} + (-V_{\text{IN}}))/2$  for the Attenuation inputs and  $V_{\text{CM\_AMP}} = (+I_{\text{IN}} + (-I_{\text{IN}}))/2$  for the Amplification inputs, has to stay between the MIN and MAX values determined by these formulas:

$$CM_{\text{MAX}} = V_S + 1/K_V * (V_S - V_{\text{OCM}})$$

$$CM_{\text{MIN}} = -1/K_V * V_{\text{OCM}}$$

$K_V$  is a function of the Gain according to the table below:

Gain	0.096 V/V	0.192 V/V	0.384 V/V	0.768 V/V	1 V/V	2 V/V
$K_V$	0.12	0.218	0.414	0.806	1.065	2.096

Regardless to the values derived by the formula, the voltage on each input pin must never exceed the specified Absolute Maximum Ratings.

Below are some typical values:

**Table 1. Differential Input, Differential Output,  $V_S = 5\text{V}$ ,  $V_{\text{OCM}} = 2.5\text{V}$**

Gain	$V_{\text{CM\_ATT}}$		$V_{\text{CM\_AMP}}$	
	Min	Max	Min	Max
0.096 V/V	-15 V <sup>(1)</sup>	+15 V <sup>(1)</sup>		
0.192 V/V	-11.5 V	+15 V		
0.384 V/V	-6 V	+11 V		
0.768 V/V	-3.1 V	+8.1 V		
1 V/V			-2.3 V	+7.3 V
2 V/V			-1.2 V	+6.2 V

(1) Limited by the operating ratings on input pins

In the case of a single ended input referred to ground ( $-V_{\text{IN}} = \text{GND}$ ,  $-I_{\text{IN}} = \text{GND}$ ) the table below summarizes the voltage range allowed on the  $+V_{\text{IN}}$  and  $+I_{\text{IN}}$  inputs.

**Table 2. Single Ended Input, Differential Output,  $V_S = 5\text{V}$ ,  $V_{\text{OCM}} = 2.5\text{V}$ ,  $-V_{\text{IN}} = \text{GND}$ ,  $-I_{\text{IN}} = \text{GND}$**

Gain	$+V_{\text{IN}}$		$+I_{\text{IN}}$	
	Min	Max	Min	Max
0.096 V/V	-15 V <sup>(1)</sup>	+15 V <sup>(1)</sup>		
0.192 V/V	-15 V <sup>(1)</sup>	+15 V <sup>(1)</sup>		
0.384 V/V	-12 V <sup>(2)</sup>	+12 V <sup>(2)</sup>		
0.768 V/V	-6 V <sup>(2)</sup>	+6 V <sup>(2)</sup>		
1 V/V			-4.6 V <sup>(2)</sup>	+4.6 V <sup>(2)</sup>
2 V/V			-2.3 V <sup>(2)</sup>	+2.3 V <sup>(2)</sup>

(1) Limited by the operating ratings on input pins.

(2) Limited by the output voltage swing (0.2V to  $V_S - 0.2\text{V}$  on both  $+V_{\text{OUT}}$  and  $-V_{\text{OUT}}$ )

### Single Ended Output

In this mode the LMP7312 behaves as a Difference Amplifier, with  $-V_{\text{OUT}}/V_R$  being the reference output voltage when a zero volt differential input signal is applied. The voltages at the OpAmp inputs are determined by  $+V_{\text{IN}}$  and  $-V_{\text{OUT}}/V_R$  voltages. The voltage range of  $+V_{\text{IN}}$  and  $+I_{\text{IN}}$  inputs is as follows:

$$V_{\text{MAX}} = V_S + 1/K_V * (V_S - (-V_{\text{OUT}}/V_R))$$

$$V_{\text{MIN}} = -1/K_V * (-V_{\text{OUT}}/V_R)$$

Regardless of the values derived by the formula, the voltage on each input pin must never exceed the specified Absolute Maximum Ratings.

Below are some typical values:

**Table 3. Differential Input, Single Ended Output,  $V_S = 5V$ ,  $V_{OCM} = GND$ , and  $-V_{OUT}/V_R = 2.5V$** 

Gain	$+V_{IN}$		$+I_{IN}$	
	Min	Max	Min	Max
0.096 V/V	-15 V <sup>(1)</sup>	+15 V <sup>(1)</sup>		
0.192 V/V	-11.5 V <sup>(1)</sup>	+15 V		
0.384 V/V	-6 V	+11 V		
0.768 V/V	-3.1 V	+8.1 V		
1 V/V			-2.3 V	+7.3 V
2 V/V			-1.2 V	+6.2 V

(1) Limited by the operating ratings on input pins

In the case of a single ended input referred to ground ( $-V_{IN} = GND$ ,  $-IN = GND$ ) this table summarize the voltage ranges allowed on the  $+V_{IN}$  and  $+I_{IN}$  inputs.

**Table 4. Single Ended Input, Single Ended Output,  $V_S = 5V$ ,  $V_{OCM} = GND$ ,  $-V_{OUT}/V_R = 2.5V$ ,  $-V_{IN} = GND$ ,  $-I_{IN} = GND$** 

Gain	$+V_{IN}$		$+I_{IN}$	
	Min	Max	Min	Max
0.096 V/V	-15 V <sup>(1)</sup>	+15 V <sup>(1)</sup>		
0.192 V/V	-11.5 V	+12 V <sup>(2)</sup>		
0.384 V/V	-6 V <sup>(2)</sup>	+6 V <sup>(2)</sup>		
0.768 V/V	-3 V <sup>**</sup>	+3 V <sup>(2)</sup>		
1 V/V			-2.3 V <sup>(2)</sup>	+2.3 V <sup>(2)</sup>
2 V/V			-1.1 V <sup>(2)</sup>	+1.1 V <sup>(2)</sup>

(1) Limited by the operating ratings on input pins.

(2) Limited by the output voltage swing (0.2V to  $V_S - 0.2V$  on  $+V_{OUT}$ )

## SERIAL INTERFACE CONTROL OPERATION

The serial interface control of the LMP7312 can be supplied with a voltage between 2.7V and 5.5V through the  $V_{IO}$  pin for compatibility with different logic families present in the market.

The LMP7312 Attenuation, Amplification, Null switch and HiZ modes are controlled by a register. Data to be written into the control register is first loaded into the LMP7312 via the serial interface. The serial interface employs a 5-bit shift register. Data is loaded through the serial data input, SDI. Data passing through the shift register is obtained through the serial data output, SDO. The serial clock, SCK controls the serial loading process. All five data bits are required to correctly program the device. The falling edge of  $\overline{CS}$  enables the shift register to receive data. The SCK signal must be high during the falling edge of  $\overline{CS}$ . Each data bit is clocked into the shift register on the rising edge of SCK. Data is transferred from the shift register to the holding register on the rising edge of  $\overline{CS}$ . Operation is shown in the timing diagram [Timing Diagram](#).

### SPI Registers

MSB				LSB
Gain_1	Gain_0	EN_CL	Null_SW	Hi_Z

### Gain\_0, Gain\_1 bit: Gain Values

Different gains are available in Attenuation Mode or Amplification Mode according to the following Gain Table.

Gain_1	Gain_0	EN_CL	Gain Value (V/V)
0	0	0	<b>0.096</b>
0	1	0	<b>0.192</b>
1	0	0	<b>0.384</b>
1	1	0	<b>0.768</b>
1	0	1	<b>1</b>

Gain_1	Gain_0	EN_CL	Gain Value (V/V)
1	1	1	2

**EN\_CL bit:** Enable Amplification Mode

This register selects which input pair is processed.

EN_CL	Mode	Description
0	Attenuation Mode	$\pm V_{IN}$ inputs are processed through the 104.16k input resistors
1	Amplification Mode	$\pm IN$ inputs are processed through the 40k input resistors

**NULL\_SW bit:** Input Offset Nulling Switch Mode

This register selects a mode in which the amplifier is not processing any input but it is configured in unity gain to allow system level amplifier offset calibration. The Nulling Switch mode is available in both single ended and fully differential output mode. The LMP7312 in Nulling Switch and fully differential mode has the following configuration.

NULL_SW	Mode	Description
0	Normal Operation Mode	$\pm V_{IN}$ and $\pm IN$ inputs are processed depending on EN_CL register setting.
1	Nulling Switch Mode	Enables to evaluate the offset of the internal amplifier for system level calibration

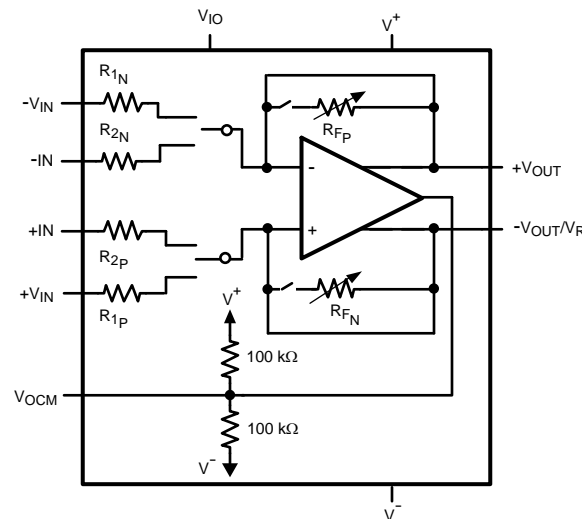


Figure 5. LMP7312 in Nulling Switch Mode

In this condition at the Output pins is possible to measure the input voltage offset of the op-amp:

Output Mode	+V <sub>OUT</sub>	-V <sub>OUT</sub> /V <sub>R</sub>
Differential	$V_{CM\_out} + V_{OS}/2$	$V_{CM\_out} - V_{OS}/2$
Single-Ended	$V_R + V_{OS}$	$V_R$

**Hi\_Z bit:** High Impedance

In this mode both outputs +V<sub>OUT</sub> and -V<sub>OUT</sub>/V<sub>R</sub> of the LMP7312 are in tri-state [Figure 6](#).

HI_Z	Mode	Description
0	Normal Operation Mode	The LMP7312 is configured according to value of the other 4 bits of the register.
1	High Impedance Mode	The LMP7312 output is in high impedance



### Shared 4-wire SPI with ADC

The LMP7312 is a good choice when interfacing to differential analog to digital converters ADC141S626 and ADC161S626 of PowerWise® Family. Its SPI interface has been designed to enable sharing CSB with the ADC. LMP7312 register access happens only when CSB is asserted low while SCK is high. However, the ADC starts conversion under any of the following conditions: (1) CSB goes low while SCK is high, (2)

CSB goes low while SCK is low, (3) CSB and SCK both going low. Therefore, if a system uses timing condition #2 above, LMP7312 and ADC1x1S626 can share CSB and SCK as shown in Figure 8. The only side-effect would be that writing to LMP7312 triggers an ADC conversion, but then the result can be ignored. At other times, the LMP7312 is not affected by the CSB assertions used to initiate normal ADC conversions.

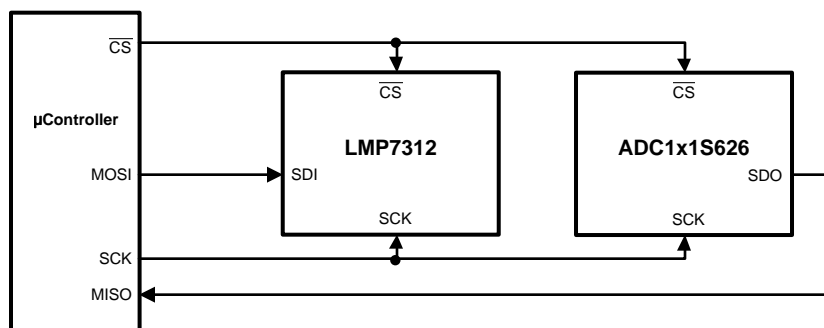


Figure 8. 4-wire SPI with ADC interface

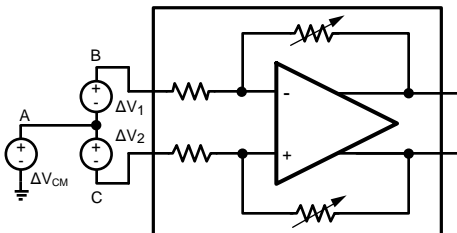
### LMP7312 IN 4-20mA CURRENT LOOP APPLICATION

The 4-20mA current loop shown in Figure 9 is a common method of transmitting sensor information in many industrial process-monitoring applications. Transmitting sensor information via a current loop is particularly useful when the information has to be sent to a remote location over long distances (1000 feet, or more). The loop's operation is straightforward: a sensor's output voltage is first converted to a proportional current, with 4mA normally representing the sensor's zero-level output, and 20mA representing the sensor's full-scale output. Then, a receiver at the remote end converts the 4-20mA current back into a voltage which in turn can be further processed by a computer or display module. A typical 4-20mA current-loop circuit is made up of four individual elements: a sensor/transducer; a voltage-to-current converter (commonly referred to as a transmitter and/or signal conditioner); a loop power supply; and a receiver/monitor. In loop powered applications, all four elements are connected in a closed, series circuit, loop configuration (Figure 9). Sensors provide an output voltage whose value represents the physical parameter being measured. The transmitter amplifies and conditions the sensor's output, and then converts this voltage to a proportional 4-20mA dc-current that circulates within the closed series-loop. The loop power-supply generally provides all operating power to the transmitter and receiver, and any other loop components that require a well-regulated dc voltage. In loop-powered applications, the power supply's internal elements also furnish a path for closing the series loop. The receiver/monitor, normally a subsection of a panel meter or data acquisition system, converts the 4-20mA current back into a voltage which can be further processed and/or displayed. The high DC performance of the LMP7312 makes this difference amplifier an ideal choice for use in current loop AFE receiver. The LMP7312 has a low input offset voltage and low input offset voltage drift when configured in amplification mode. In the circuit shown in Figure 9 the LMP7312 is in amplification mode with a gain of 2V/V and differential output in order to well match the input stage of the ADC141S626 (SAR ADC with differential input). The shunt resistor is 100ohm in order to have a max voltage drop of 2V when 20mA flows in the loop. The first order filter between the LMP7312 and the ADC141S626 reduces the noise bandwidth and allows handling input signal up to 2kHz. That frequency has been calculated taking in account the roll off of the filter and ensuring a gain error less than 1LSB of the ADC141S626. In order to utilize the maximum number of bits of the ADC141S626 in this configuration, a 4.1V reference voltage is used. With this system, the current of the 4-20mA loop is accurately gained to the full scale of the ADC and then digitized for further processing.



**Input resistance calculation**

The common mode input resistance is the resistance seen from node “A” when  $\Delta V_1 = \Delta V_2 = 0$  and a common mode voltage  $\Delta V_{CM}$  is applied to both inputs of the LMP7312. The differential input resistance is the resistance seen from the nodes “B” and “C” when  $\Delta V_{CM}=0$  and a differential voltage  $\Delta V_1 = \Delta V_2 = V/2$  is applied to the inputs of the LMP7312.



**Figure 10. Circuit for Input Resistance calculation**

Mode of Operation		Unit	Gains			
			0.096	0.192	0.384	0.768
Attenuation Mode	Common Mode Resistance	kΩ	57.08	62.08	72.08	92.08
	Differential Resistance	kΩ	228.30	248.30	288.30	368.30
Amplification Mode			1		2	
	Common Mode Resistance	kΩ	40.0		60.0	
	Differential Resistance	kΩ	160.0		240.0	

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMP7312MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMP7312MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7312MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7312MAX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0



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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

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