April 1998

LMC6953 PCI Local Bus Power Supervisor

National Semiconductor

# LMC6953 PCI Local Bus Power Supervisor

### **General Description**

The LMC6953 is a voltage supervisory chip designed to meet PCI (Peripheral Component Interconnect) Specifications Revision 2.1. It monitors 5V and 3.3V power supplies. In cases of power-up, power-down, brown-out, power failure and manual reset interrupt, the LMC6953 provides an active low reset. RESET holds low for 100 ms after both 5V and 3.3V powers recover, or after manual reset signal returns to high state. The external capacitor on pin 8 adjusts the reset delay.

This part is ideal on PCI motherboards or add-in cards to ensure the integrity of the entire system when there is a fault condition. The active low reset sets the microprocessor or local device in a known state.

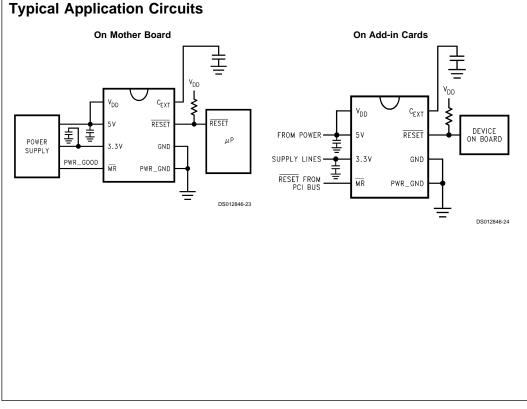
The LMC6953 has a built-in bandgap reference that accurately determines all the threshold voltages. The internal reset delay circuitry eliminates additional discrete components.

#### Features

- Compliant to PCI specifications revision 2.1.
- Under and over voltage detectors for 5V and 3.3V
- Power failure detection (5V falling under 3.3V by
- 300 mV max)
- Manual reset input pin
- Guaranteed RESET assertion at V<sub>DD</sub> = 1.5V
- Integrated reset delay circuitry
- Open drain output
- Adjustable reset delay
- Response time for over and under voltage detection: 490 ns Max
- Power failure response time: 90 ns Max
- Requires minimal external components

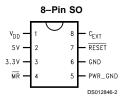
### Applications

- Desktop PCs
- PCI-Based Systems
- Network servers



© 1998 National Semiconductor Corporation DS012846

# **Connection Diagram**



Top View

# **Ordering Information**

Package	Industrial Temp Range	NSC Supp	
	–40°C to +85°C	Drawing	As
8-Pin Small	LMC6953CM	M08A	Rails
Outline	LMC6953CMX		2.5k Tape
			and Reel

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Lead Temp. (Soldering, 10 sec.)260°CStorage Temperature Range-65°C to +150°CJunction Temperature150°C

# Operating Ratings (Note 1)

2 kV	Supply Voltage	1.5V to 6V
200V	Junction Temperature Range	
7V	LMC6953C	-40°C to +85°C
7V	Thermal Resistance ( $\theta_{JA}$ )	
15 mA	M Package	165°C/W
10 mA		

## **DC Electrical Characteristics**

Current at Power Supply Pin (Note 3)

ESD Tolerance (Note 2) Human Body Model Machine Model Voltage at Input Pin Supply Voltage

Current at Output Pin

Unless otherwise specified, all **boldface** limits guaranteed for  $T_J = -40^{\circ}C$  to +85°C,  $V_{DD} = 5V$ ,  $R_{PULL-UP} = 4.7 \text{ k}\Omega$  and  $C_{EXT} = 0.01 \text{ }\mu\text{F}$ . Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
V <sub>H5</sub>	V <sub>DD</sub> Over-Voltage Threshold	$T_J = 0^{\circ}C$ to $70^{\circ}C$ (Note 4)	5.45	5.60	5.75	V
		$T_J = -40^{\circ}C$ to $85^{\circ}C$ (Note 4)	5.30	5.60	5.90	V
V <sub>L5</sub>	V <sub>DD</sub> Under-Voltage Threshold	$T_J = 0^{\circ}C$ to $70^{\circ}C$ (Note 4)	4.25	4.40	4.55	V
		$T_J = -40^{\circ}C \text{ to } 85^{\circ}C$ (Note 4)	4.10	4.40	4.70	V
V <sub>H3.3</sub>	3.3V Over-Voltage Threshold	$T_J = 0^{\circ}C$ to $70^{\circ}C$ (Note 5)	3.80	3.95	4.10	V
		$T_J = -40^{\circ}C \text{ to } 85^{\circ}C$ (Note 5)	3.60	3.95	4.30	V
V <sub>L3.3</sub>	3.3V Under-Voltage Threshold	$T_J = 0^{\circ}C$ to $70^{\circ}C$ (Note 5)	2.50	2.65	2.80	V
		$T_J = -40^{\circ}C \text{ to } 85^{\circ}C$ (Note 5)	2.30	2.65	3.00	V
V <sub>MR</sub>	Manual RESET Threshold			2.50	2.80	V
V <sub>PF</sub>	Power Failure Differential Voltage (3.3V Pin–5V Pin)	(Note 6)		150	300	mV
R <sub>IN</sub>	Input Resistance at 5V and 3.3V Pins			35		kΩ
V <sub>OL</sub>	RESET Output Low	$T_{J} = 0^{\circ}C \text{ to } 70^{\circ}C$ $V_{DD} = 1.5V \text{ to } 6V$ $T_{J} = -40^{\circ}C \text{ to } 85^{\circ}C$ $V_{DD} = 1.55V \text{ to } 6V$		0.05	0.10	V
Is	Supply Current	(Note 3)		0.8	1.50	mA

## **AC Electrical Characteristics**

Unless otherwise specified, all **boldface** limits guaranteed for  $T_J = -40^{\circ}C$  to 85°C,  $V_{DD} = 5V$ ,  $R_{PULL-UP} = 4.7 \text{ k}\Omega$  and  $C_{EXT} = 0.01 \ \mu\text{F}$ . Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Тур	LMC6953	Units
				Limit	
t <sub>D</sub>	Over or Under Voltage Response Time	(Note 7)	150	490	ns
					max
t <sub>PF</sub>	Power Failure Response Time	(Note 8)	40	90	ns
					max
t <sub>RESET</sub>	Reset Delay	C <sub>EXT</sub> = 0.01 μF	100		ms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is tended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics. Note 2: Human body model, 1.5 kΩ in series with 100 pF. Machine model. 200Ω in series with 100 pF.

# AC Electrical Characteristics (Continued)

Note 3: Supply current measured at pins 1, 2, and 3. The 4.7 kΩ pull-up resistor on pin 7 is not tied to V<sub>DD</sub>in this measurement.

Note 4: PCI Specifications Revision 2.1, Section 4.2.1.1 and Section 4.3.2.

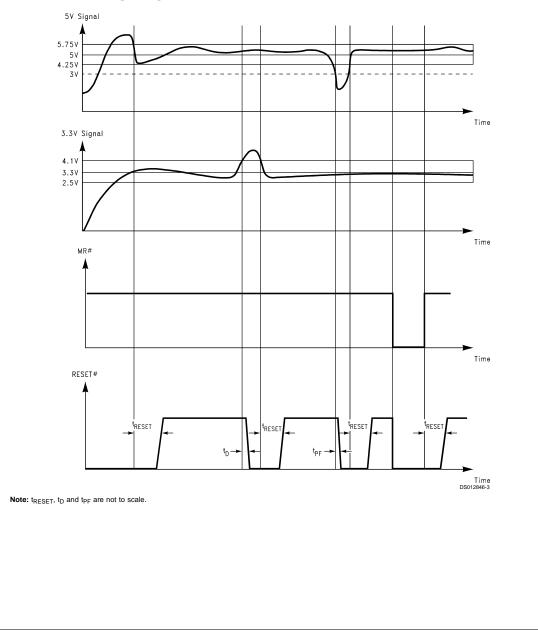
Note 5: PCI Specifications Revision 2.1, Section 4.2.2.1 and Section 4.3.2.

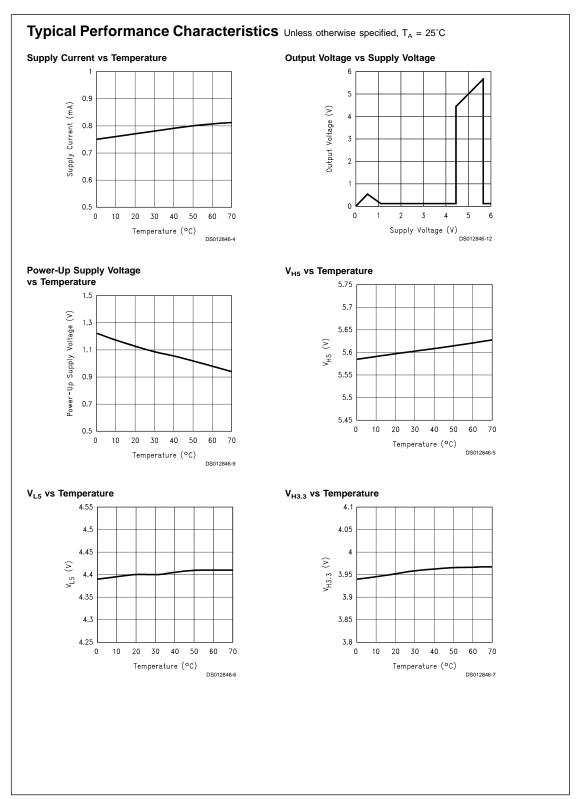
Note 6: PCI Specifications Revision 2.1 and Section 4.3.2.

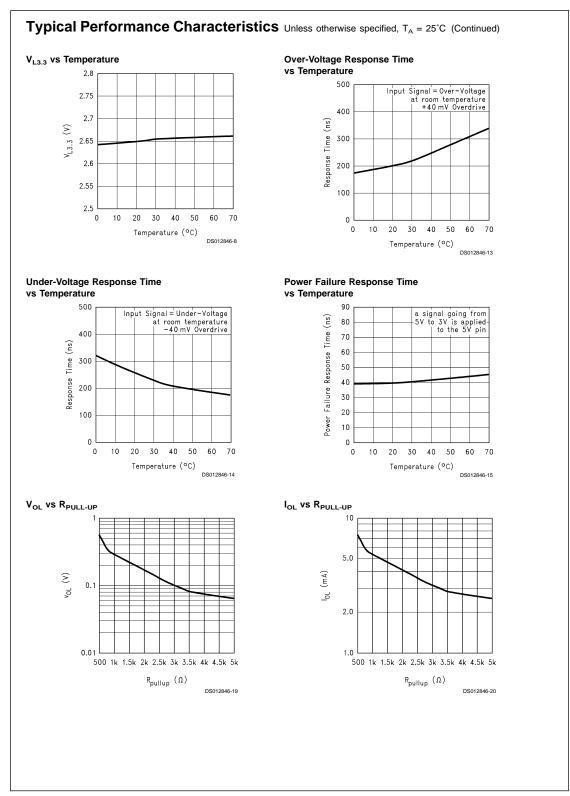
Note 7: PCI Specifications Revision 2.1, Section 4.3.2. The response time is measured individually with ±750 mV of overdrive applied to pin 2 then ±600 mV of overdrive applied to pin 3 and taking the worst number of the four measurements.

Note 8: PCI Specifications Revision 2.1, Section 4.3.2. The power failure response time is measured with a signal changing from 5V to 3V applied to pin 2 and a 3.3V DC applied to pin 3.

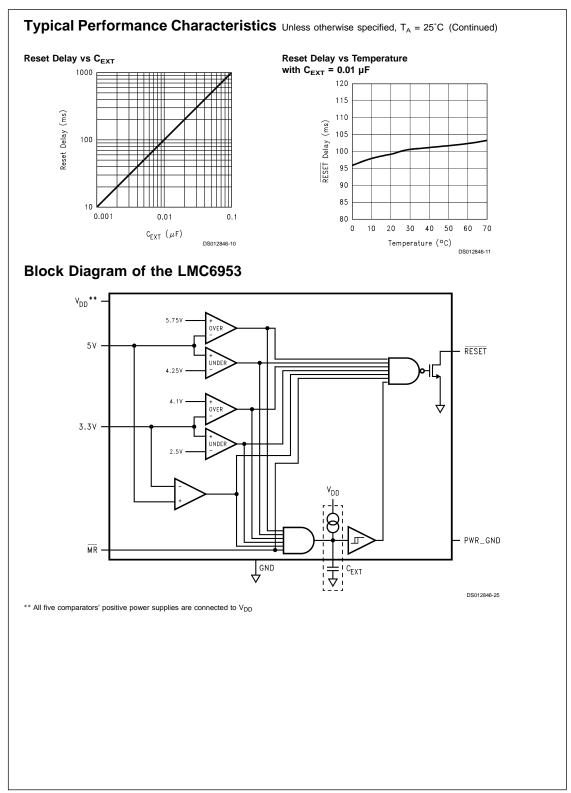
## LMC6953 Timing Diagram







6



## **Truth Table**

Power	5V	5V	3.3V	3.3V	MR	RESET
Failure	Over-Voltage	Under-Voltage	Over-Voltage	Under-Voltage		
Fail	Х	Х	Х	X	High	Low
Х	Fail	Х	Х	Х	High	Low
Х	X	Fail	Х	X	High	Low
Х	Х	Х	Fail	X	High	Low
Х	X	Х	Х	Fail	High	Low
Х	Х	Х	Х	Х	Low	Low
OK	OK	OK	OK	ОК	High	High

X = Don't Care

## **Pin Description**

Pin	Name Function				
1	V <sub>DD</sub>	5V input supply voltage. This pin supplies power to the internal comparators. It can be connected to a capacitor acting as a back-up battery. Otherwise, it should be shorted to the 5V pin.			
2	5V	5V input supply voltage. This pin is not connected to the positive power supply of the internal comparators. It provides input signal to the 5V window comparators as well as the power failure comparator.			
3	3.3V	3.3V input supply voltage. This pin provides input signal to the 3.3V window comparators and the power failure comparator.			
4	MR	Manual reset input pin. It takes 5V CMOS logic low and triggers $\overrightarrow{\text{RESET}}$ . If not used, this pin should be connected to $V_{\text{DD}}$ .			
5	PWRGND	Ground.			
6	GND	This pin should be grounded at all times.			
7	RESET	Active low reset output. RESET holds low for 100 ms after both 5V and 3.3V powers recover, or after manual reset signal returns to high state.			
8	C <sub>EXT</sub>	External capacitor pin. The value of C <sub>EXT</sub> sets the reset delay.			

## **Application Note**

#### HOW THE LMC6953 FUNCTIONS

The LMC6953 is a power supply supervisor with its performance specifications compliant to PCI Specifications Revision 2.1. The chip monitors power-up, power-down, brown-out, power failure and manual reset interrupt situations.

During power-up, the LMC6953 holds  $\overline{\text{RESET}}$  low for 100 ms after both 5V and 3.3V are within specified windows. It asserts reset in 490 ns when a brown-out is detected. Brown-out occurs when 5V supply is above 5.75V over-voltage or below 4.25V under-voltage or when 3.3V supply is above 4.1V over-voltage or 2.5V under-voltage. In case of power failure where the 5V supply falls under 3.3V supply by 300 mV maximum, reset is asserted in 90 ns.  $\overline{\text{RES}}$  SET also can be asserted by sending a 5V CMOS logic low to the manual reset pin.

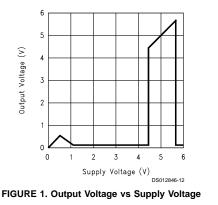
Each time  $\overline{\text{RESET}}$  is asserted, it holds low for 100 ms after a fault condition is recovered. The 100 ms reset delay is generated by the 0.01  $\mu\text{F}$  C<sub>EXT</sub> capacitor, and can be adjusted by changing the value of C<sub>EXT</sub>.

It is highly recommended to place lands on printed circuit boards for 120 pF capacitors between pin 2 and ground and

also between pin 3 and ground. As power supplies may change abruptly, there can be very high frequency noise present and the capacitors can minimize the noise,

#### MINIMUM SUPPLY VOLTAGE FOR RESET ASSERTION

The LMC6953 guarantees  $V_{DD}$  = 1.55V as the minimum supply voltage to achieve consistent RESET assertion. This ensures system stability in initialization state.



www.national.com

### Application Note (Continued)

Figure 1 is measured by shorting pins 1, 2 and 3 together when supply voltage is from 0V to 3.3V. Then pin 3 is connected with a constant 3.3  $V_{\rm DC}$  and pins 1 and 2 are connected to a separate power supply that continues to vary from 3.3V to 6V.

#### 5V AND V<sub>DD</sub> PINS

By having the 5V and the  $V_{\rm DD}$  pins separate, a capacitor can be used as a back-up power supply in event of a sudden power supply failure. This circuit is shown in the application circuit section titled "On Motherboard With Capacitor as a Back-up Power Supply." Under normal condition, the diode is forward-biased and the capacitor is charged up to  $V_{\rm DD}$  – 0.7V. If the power supply goes away, the diode becomes reverse-biased, isolating the 5V and the  $V_{\rm DD}$  pins. The capacitor provides power to the internal comparators for a short duration for the LMC6953 to operate.

#### **C**EXT SETS RESET DELAY IN LINEAR FASHION

The LMC6953 has internal delay circuitry to generate the reset delay. By choosing different values of capacitor  $C_{\text{EXT}}$ , reset delay can be programmed to the desired length for the system to stabilize after a fault condition occurs.

#### **EVALUATING THE LMC6953**

#### To Measure Over-Voltages and Under-Voltages.

Connect a 3.3V DC to the 3.3V pin and a 5V DC to the  $V_{DD}$  and the 5V pins ( $V_{DD}$  and 5V pins are shorted). RESET output is high because voltages are within window. These voltages should be monitored. While keeping the 3.3V constant, increase the 5V DC signal until a RESET low is detected. The point on the 5V DC signal at which RESET changes from high to low is the 5V over-voltage. It is typically 5.6V. To detect 5V under-voltage, start the 5V DC signal at which RESET on the 5V and decrease it until a RESET low is detected. The point on the 5V DC signal at which RESET bow is the 5V over-voltage. It is typically 5.6V. To detect 5V under-voltage, start the 5V DC signal from 5V and the 5V DC signal at which RESET changes from high to low is the 5V under-voltage. It is typically 4.4V.

To find 3.3V over-voltage and under-voltage, keep the 5V DC at 5V and vary the 3.3V DC signal until a  $\overrightarrow{\text{RESET}}$  low is detected.

#### To Measure Timing Specifications.

For evaluation purposes only, the V<sub>DD</sub> and the 5V pins should have separate signals. It is easier to measure response time in this manner. The V<sub>DD</sub> pin is connected to a steady 5V DC and the 5V pin is connected to a pulse generator. To simulate the power supply voltages going out of window, a pulse generator with disable/enable feature and rise and fall time adjustment is recommended. To measure the RESET signal, a oscilloscope is recommended because of its ability to capture and store a signal.

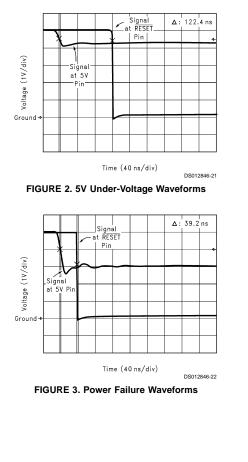
To measure the 5V under-voltage response time on the LMC6953, set the pulse generator to trigger mode and program the amplitude to have a high value of 5V and a low value of the 5V under-voltage threshold measured previously with 50 mV overdrive. For example, if the measured 5V under-voltage is 4.4V, then a 50 mV overdrive on this signal is 4.35V. The disable feature on the pulse generator should be on. Program the fall time of the pulse to be 30 ns and pro-

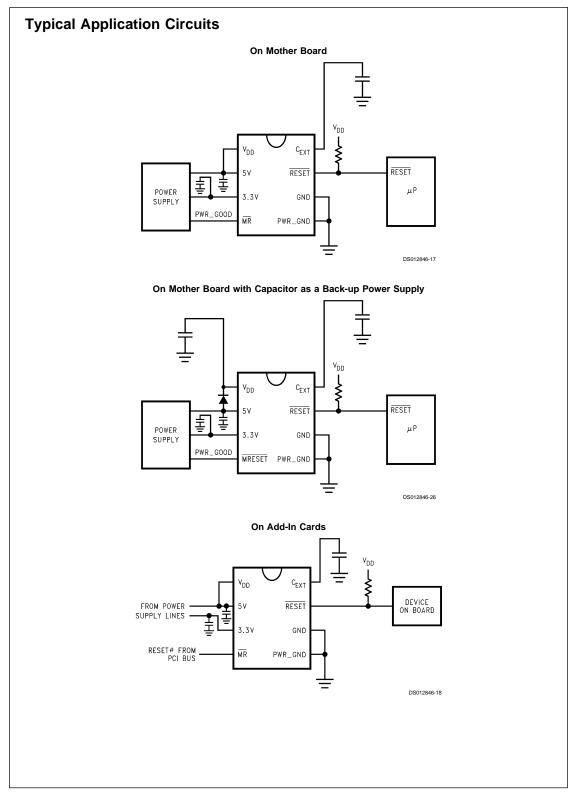
gram the scope to trigger on the falling edge, with trigger level of 4.5V. Set the scope to 200 ns/division. The probes should be connected to the 5V pin and the RESET pin. Now enable the 5V signal from the pulse generator and trigger the signal. Be aware that when the signal is enabled, there is high frequency noise present, and putting a 120 pF capacitor between the 5V pin and ground suppresses some of the noise. Response time is measured by taking the 5V under-voltage threshold on the 5V signal to the point where RESET goes low. *Figure 2* shows a scope photo of 5V under-voltage waveforms. It is taken with a signal going from 5V to 4.25V at the 5V pin.

To measure the 100 ms  $\overline{\text{RESET}}$  delay, change the scope to 50 ms/division and trigger the 5V signal again.  $\overline{\text{RESET}}$  should stay low for 100 ms after the 5V is recovered and within window.

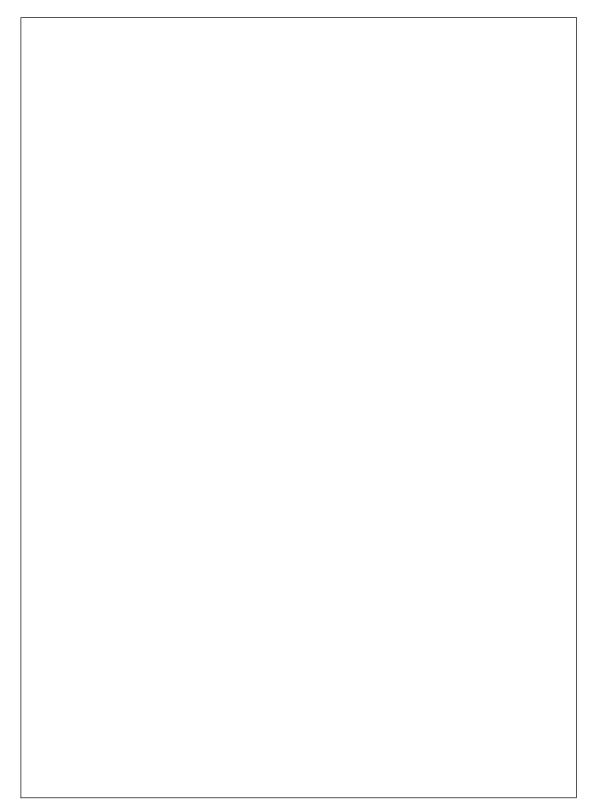
Other over-voltages and under-voltages can be measured by changing the pulse generator to different voltage steps. Putting a 120 pF capacitor between the 3.3V pin and ground is recommended in evaluating 3.3V signal.

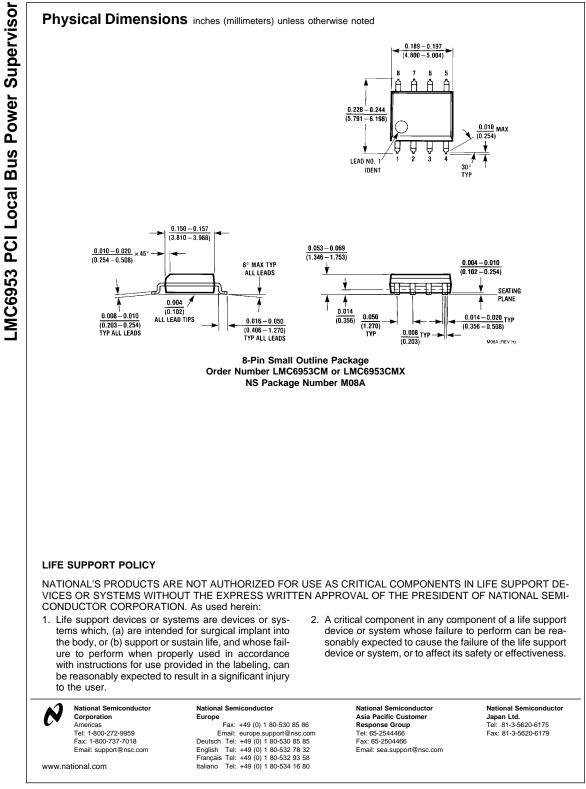
To measure power-failure response time, set the pulse generator from 5V to 3V with fall time of the pulse 3 ns and connect it to the 5V pin. RESET should go low within 90 ns of power failure. *Figure 3* shows a scope photo of power failure waveforms. It is taken with a signal going from 5V to 3V at the 5V pin.





10





National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications