LMC555 CMOS Timer

Check for Samples: LMC555

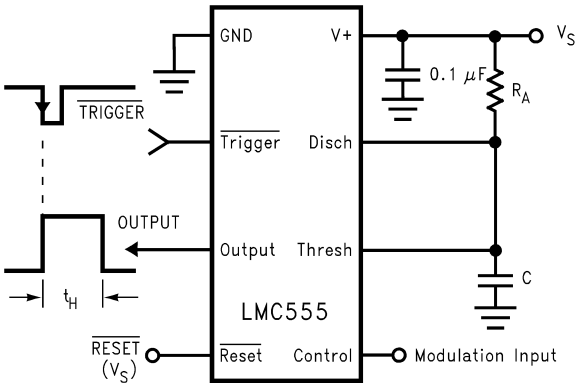
FEATURES

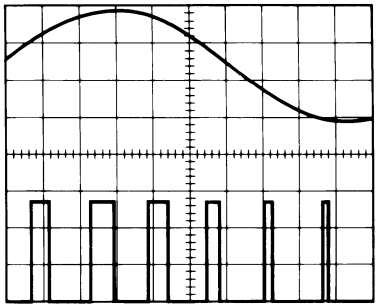
- **Less than 1 mW Typical Power Dissipation at 5V Supply**
- **3 MHz Astable Frequency Capability**
- **1.5V Supply Operating Voltage Ensured**
- **Output Fully Compatible with TTL and CMOS Logic at 5V Supply**
- **Tested to −10 mA, +50 mA Output Current Levels**
- **Reduced Supply Current Spikes During Output Transitions**
- **Extremely Low Reset, Trigger, and Threshold Currents**
- **Excellent Temperature Stability**
- **Pin-for-Pin Compatible with 555 Series of Timers**
- **Available in 8-pin VSSOP Package and 8-Bump DSBGA package**

DESCRIPTION

The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. In addition to the standard package (SOIC, VSSSOP, and PDIP) the LMC555 is also available in a chip sized package (8 Bump DSBGA) using TI's DSBGA package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the stable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of Texas Instruments' LMCMOS process extends both the frequency range and low supply capability.

Pulse Width Modulator





Connection Diagram

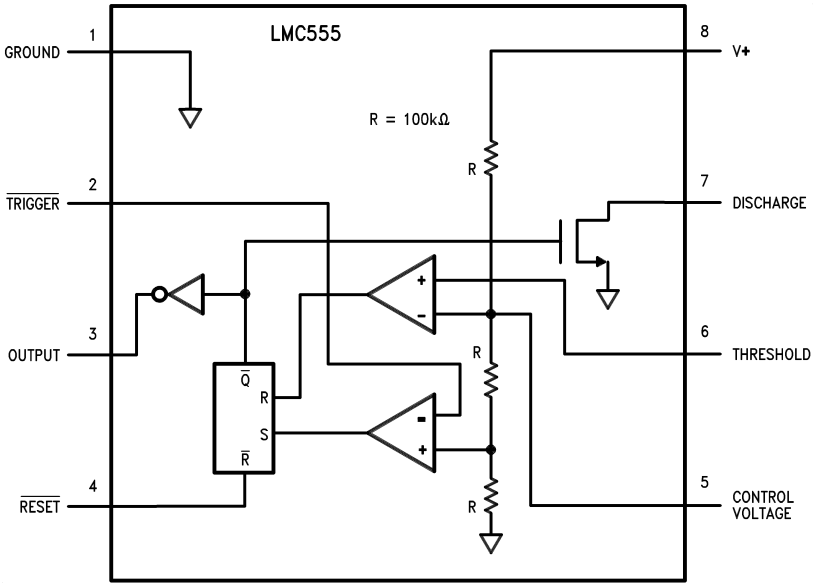


Figure 1. 8-Pin SOIC, VSSOP, PDIP
Top View

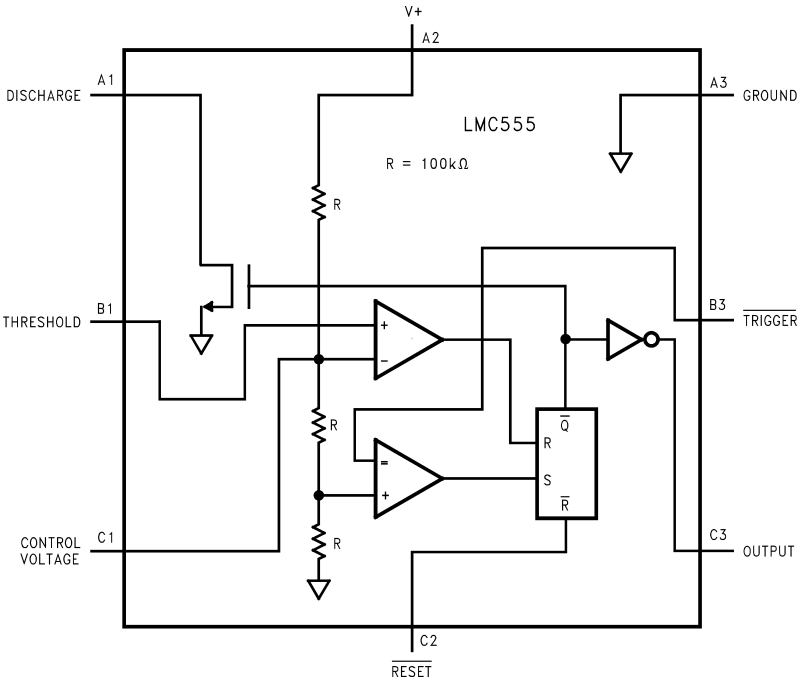


Figure 2. 8-Bump DSBGA
Top View (Bump Side Down)

Table 1. Pin Descriptions

Pin Name	Package Pin Numbers	
	8-Pin SOIC, VSSOP, and PDIP	8-Bump DSBGA
GND	1	A3
$\overline{\text{Trigger}}$	2	B3
Output	3	C3
$\overline{\text{Reset}}$	4	C2
Control Voltage	5	C1
Threshold	6	B1
Discharge	7	A1
V^+	8	A2

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage, V^+	15V
Input Voltages, V_{TRIG}, V_{RES}, V_{CTRL}, V_{THRESH}	−0.3V to V_S + 0.3V
Output Voltages, V_O, V_{DIS}	15V
Output Current I_O, I_{DIS}	100 mA
Storage Temperature Range	−65°C to +150°C
Soldering specification for PDIP package:	
Soldering (10 seconds)	260°C
Soldering specification for all other packages: see product folder at www.ti.com and http://www.ti.com/lit/SNOA549	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) See AN-1112 (SNVA009) for DSBGA considerations.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Operating Ratings(1)(2)

Temperature Range	
LMC555IM	−40°C to +125°C
LMC555CM/MM/N/TP	−40°C to +85°C
Thermal Resistance (θ_{JA}) (1)	
SOIC, 8-Pin	169°C/W
VSSOP, 8-Pin	225°C/W
PDIP, 8-Pin	111°C/W
8-Bump DSBGA	220°C/W
Maximum Allowable Power Dissipation @25°C	
PDIP-8	1126 mW
SOIC-8	740 mW
VSSOP-8	555 mW
8-Bump DSBGA	568 mW

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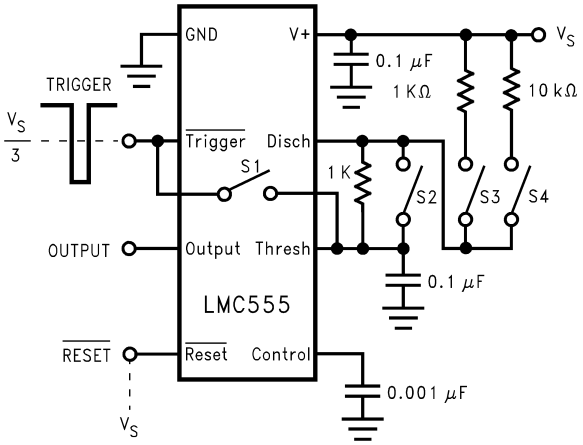
(2) See AN-1112 (SNVA009) for DSBGA considerations.

Electrical Characteristics (1) (2)

Test Circuit, T = 25°C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted

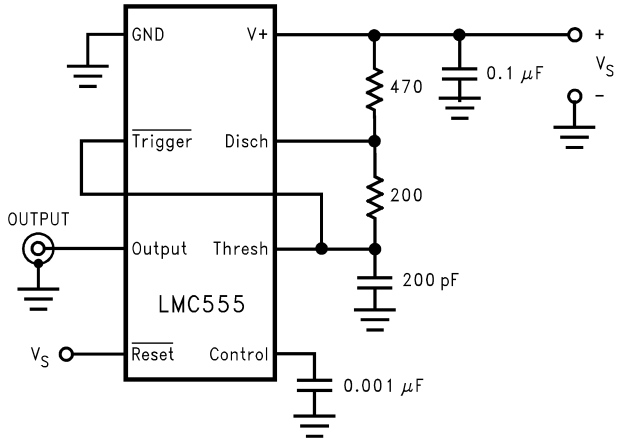
Parameter		Test Conditions	Min	Typ	Max	Units (Limits)
I_S	Supply Current	V_S = 1.5V V_S = 5V V_S = 12V		50 100 150	150 250 400	µA
V_{CTRL}	Control Voltage	V_S = 1.5V V_S = 5V V_S = 12V	0.8 2.9 7.4	1.0 3.3 8.0	1.2 3.8 8.6	V
V_{DIS}	Discharge Saturation Voltage	V_S = 1.5V, I_{DIS} = 1 mA V_S = 5V, I_{DIS} = 10 mA		75 150	150 300	mV
V_{OL}	Output Voltage (Low)	V_S = 1.5V, I_O = 1 mA V_S = 5V, I_O = 8 mA V_S = 12V, I_O = 50 mA		0.2 0.3 1.0	0.4 0.6 2.0	V
V_{OH}	Output Voltage (High)	V_S = 1.5V, I_O = −0.25 mA V_S = 5V, I_O = −2 mA V_S = 12V, I_O = −10 mA	1.0 4.4 10.5	1.25 4.7 11.3		V
V_{TRIG}	Trigger Voltage	V_S = 1.5V V_S = 12V	0.4 3.7	0.5 4.0	0.6 4.3	V
I_{TRIG}	Trigger Current	V_S = 5V		10		pA
V_{RES}	Reset Voltage	V_S = 1.5V (3) V_S = 12V	0.4 0.4	0.7 0.75	1.0 1.1	V
I_{RES}	Reset Current	V_S = 5V		10		pA
I_{THRESH}	Threshold Current	V_S = 5V		10		pA
I_{DIS}	Discharge Leakage	V_S = 12V		1.0	100	nA
t	Timing Accuracy	SW 2, 4 Closed V_S = 1.5V V_S = 5V V_S = 12V	 0.9 1.0 1.0	 1.1 1.1 1.1	 1.25 1.20 1.25	ms
$\Delta t/\Delta V_S$	Timing Shift with Supply	V_S = 5V ± 1V		0.3		%/V
$\Delta t/\Delta T$	Timing Shift with Temperature	V_S = 5V		75		ppm/°C
f_A	Astable Frequency	SW 1, 3 Closed, V_S = 12V	4.0	4.8	5.6	kHz
f_{MAX}	Maximum Frequency	Max. Freq. Test Circuit, V_S = 5V		3.0		MHz
t_R, t_F	Output Rise and Fall Times	Max. Freq. Test Circuit V_S = 5V, C_L = 10 pF		15		ns
t_{PD}	Trigger Propagation Delay	V_S = 5V, Measure Delay from Trigger to Output		100		ns

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If the $\overline{\text{RESET}}$ pin is to be used at temperatures of −20°C and below V_S is required to be 2.0V or greater.



For device pinout, please see Table 1.

Figure 3. Test Circuit



For device pinout, please see Table 1.

Figure 4. Maximum Frequency Test Circuit

APPLICATION INFORMATION

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (Figure 5). The external capacitor is initially held discharged by internal circuitry. Upon application of a negative trigger pulse of less than 1/3 V_S to the Trigger terminal, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

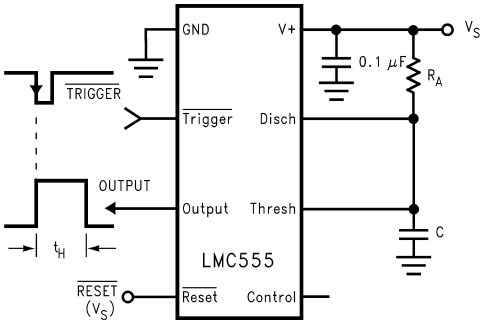
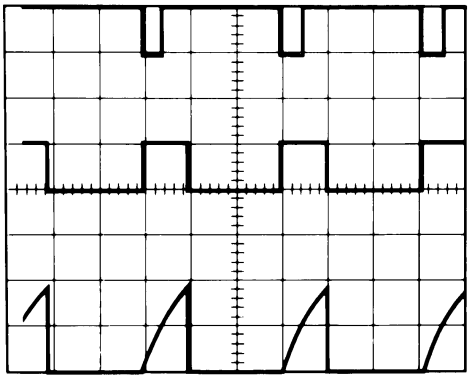


Figure 5. Monostable (One-Shot)

The voltage across the capacitor then increases exponentially for a period of t_H = 1.1 R_AC, which is also the time that the output stays high, at the end of which time the voltage equals 2/3 V_S. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 6 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



V_{CC} = 5V Top Trace: Input 5 V/Div.
TIME = 0.1 ms/Div. Middle Trace: Output 5 V/Div.
R_A = 9.1 kΩ Bottom Trace: Capacitor Voltage 2 V/Div.
C = 0.01 µF

Figure 6. Monostable Waveforms

Reset overrides Trigger, which can override threshold. Therefore the trigger pulse must be shorter than the desired t_H. The minimum pulse width for the Trigger is 20ns, and it is 400ns for the Reset. During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal. The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not use, it is recommended that it be connected to V_+ to avoid any possibility of false triggering. Figure 7 is a nomograph for easy determination of RC values for various time delays.

NOTE

In monstable operation, the trigger should be driven high before the end of timing cycle.

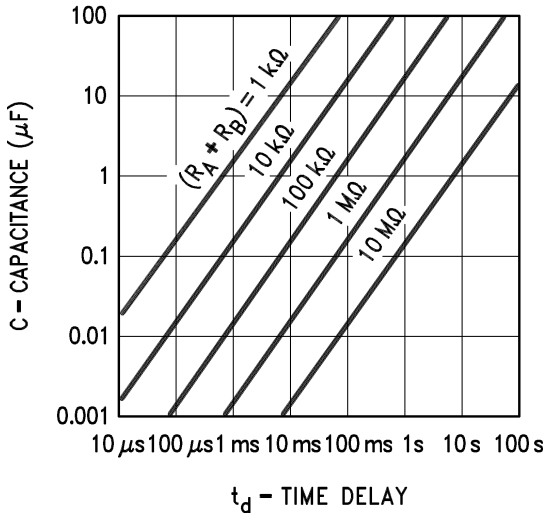


Figure 7. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in Figure 8 ($\overline{\text{Trigger}}$ and Threshold terminals connected together) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

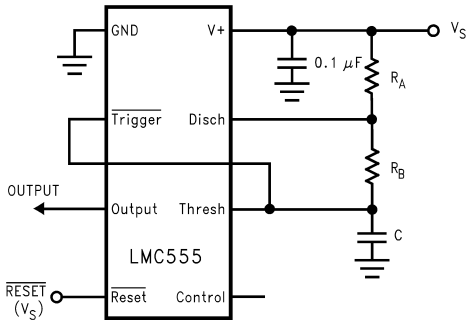
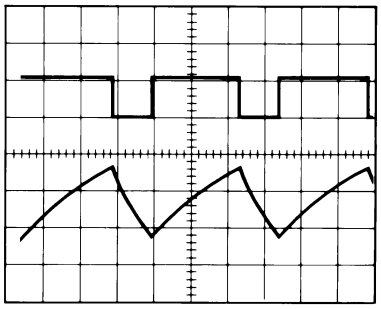


Figure 8. Astable (Variable Duty Cycle Oscillator)

In this mode of operation, the capacitor charges and discharges between 1/3 V_S and 2/3 V_S. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 9 shows the waveform generated in this mode of operation.



V_{CC} = 5V Top Trace: Output 5 V/Div.
TIME = 20 µs/Div. Bottom Trace: Capacitor Voltage 1 V/Div.
R_A = 3.9 kΩ
R_B = 9 kΩ
C = 0.01 µF

Figure 9. Astable Waveforms

The charge time (output high) is given by

$$t_1 = 0.693\ (R_A + R_B)C \quad (1)$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)C \quad (2)$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)C \quad (3)$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

Figure 10 may be used for quick determination of these RC Values. The duty cycle, as a fraction of total period that the output is low, is:

$$D = \frac{R_B}{R_A + 2R_B} \quad (5)$$

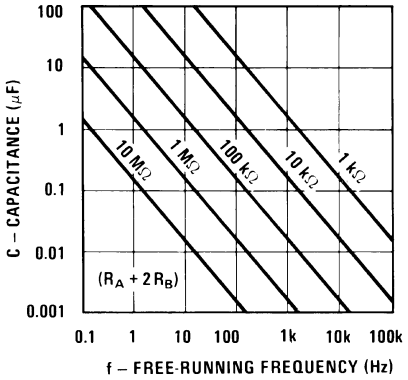
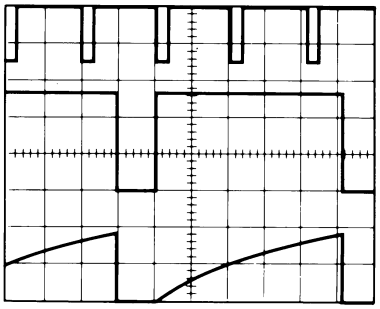


Figure 10. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of Figure 5 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 11 shows the waveforms generated in a divide by three circuit.



V_{CC} = 5V
TIME = 20 µs/Div.
R_A = 9.1 kΩ
C = 0.01 µF

Top Trace: Input 4 V/Div.
Middle Trace: Output 2 V/Div.
Bottom Trace: Capacitor 2 V/Div.

Figure 11. Frequency Divider Waveforms

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to the Control Voltage Terminal. Figure 12 shows the circuit, and in Figure 13 are some waveform examples.

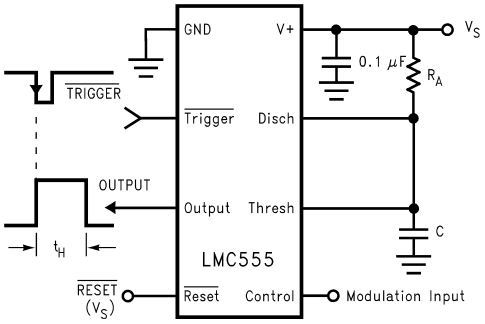
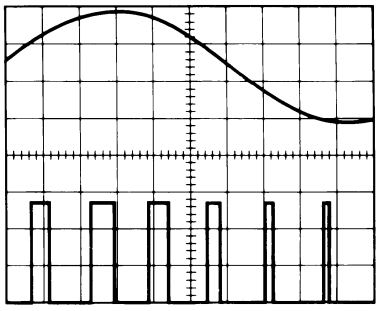


Figure 12. Pulse Width Modulator



V_{CC} = 5V
TIME = 0.2 ms/Div.
R_A = 9.1 kΩ
C = 0.01 µF

Top Trace: Modulation 1 V/Div.
Bottom Trace: Output Voltage 2 V/Div.

Figure 13. Pulse Width Modulator Waveforms

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in Figure 14, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 15 shows the waveforms generated for a triangle wave modulation signal.

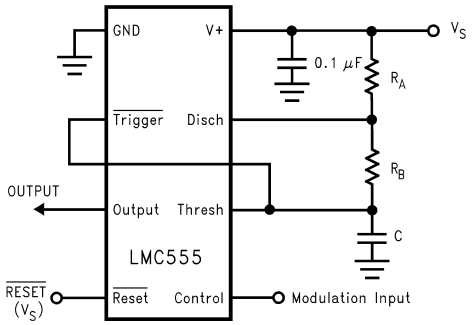
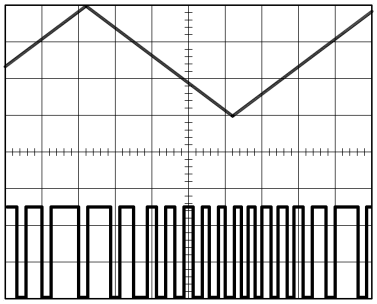


Figure 14. Pulse Position Modulator



V_{CC} = 5V
TIME = 0.1 ms/Div.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 µF

Top Trace: Modulation Input 1 V/Div.
Bottom Trace: Output Voltage 2 V/Div.

Figure 15. Pulse Position Modulator Waveforms

50% DUTY CYCLE OSCILLATOR

The frequency of oscillation is

$$f = 1/(1.4\ R_C C)$$

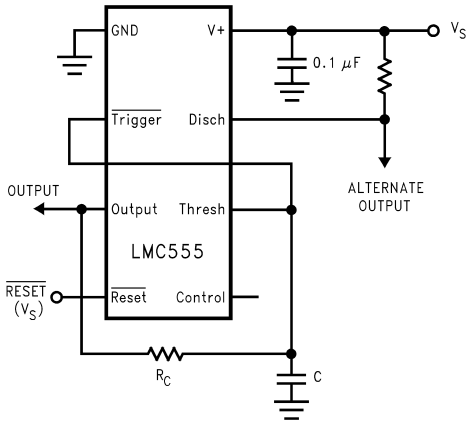


Figure 16. 50% Duty Cycle Oscillator

REVISION HISTORY

Changes from Revision I (March 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	10

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