LM98620 10-bit 70 MSPS 6 Channel Imaging Signal Processor with LVDS Output

Check for Samples: LM98620

FEATURES

- **3.3V Single Supply Operation**
- **CDS or S/H Processing**
- **35 MHz Channel Rate**
- **Enhanced ESD Protection on Timing, Control and LVDS Pins**
- **Low Power CMOS Design**
- **12 pin to 16 pin (selectable) LVDS serialized data output**
- **4-Wire Serial interface**
- **2 Channel Symmetrical Architecture**
- **Independent Gain and Offset Correction for each Channel**
- **Digital Black Level Calibration for each Channel**
- **Digital White Level Calibration for each Channel**
- **Programmable Input Clamp**

DESCRIPTION

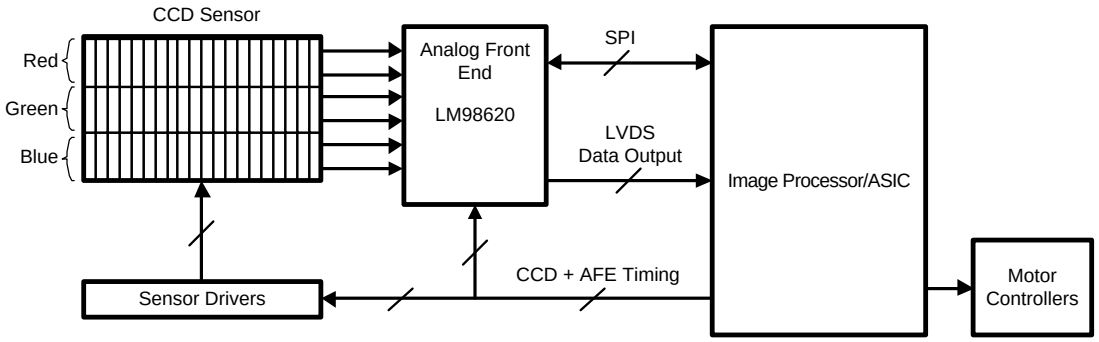
The LM98620 is a fully integrated, 10-Bit, 70 MSPS signal processing solution for high performance digital color copiers, scanners, and other image processing applications. High-speed signal throughput is achieved with an innovative six channel architecture utilizing Correlated Double Sampling (CDS), or Sample and Hold (SH) type sampling. 1x or 2x gain settings are available in the CDS/SH input stage. Each channel has a dedicated 1x to 10x (8 bit) PGA that allows accurate gain adjustment of each channel. The Digital White Level auto calibration loop can automatically set the PGA value to achieve a selected white target level. Each channel also has a ±4 bit coarse and ±10-bit fine analog offset correction DAC that allows offset correction before the sample-and-hold amplifier. These correction values can be controlled by an automated Digital Black Level correction loop. The PGA and offset DACs for each channel are programmed independently allowing unique values of gain and offset for each of the six channels. A 2-to-1 multiplexing scheme routes the signals to three 70MHz high performance ADCs. The fully differential processing channels achieve exceptional noise immunity, having a very low noise floor of -68.5dB. The 10-bit analog-to-digital converters have excellent dynamic performance making the LM98620 transparent in the image reproduction chain.

Table 1. Key Specifications

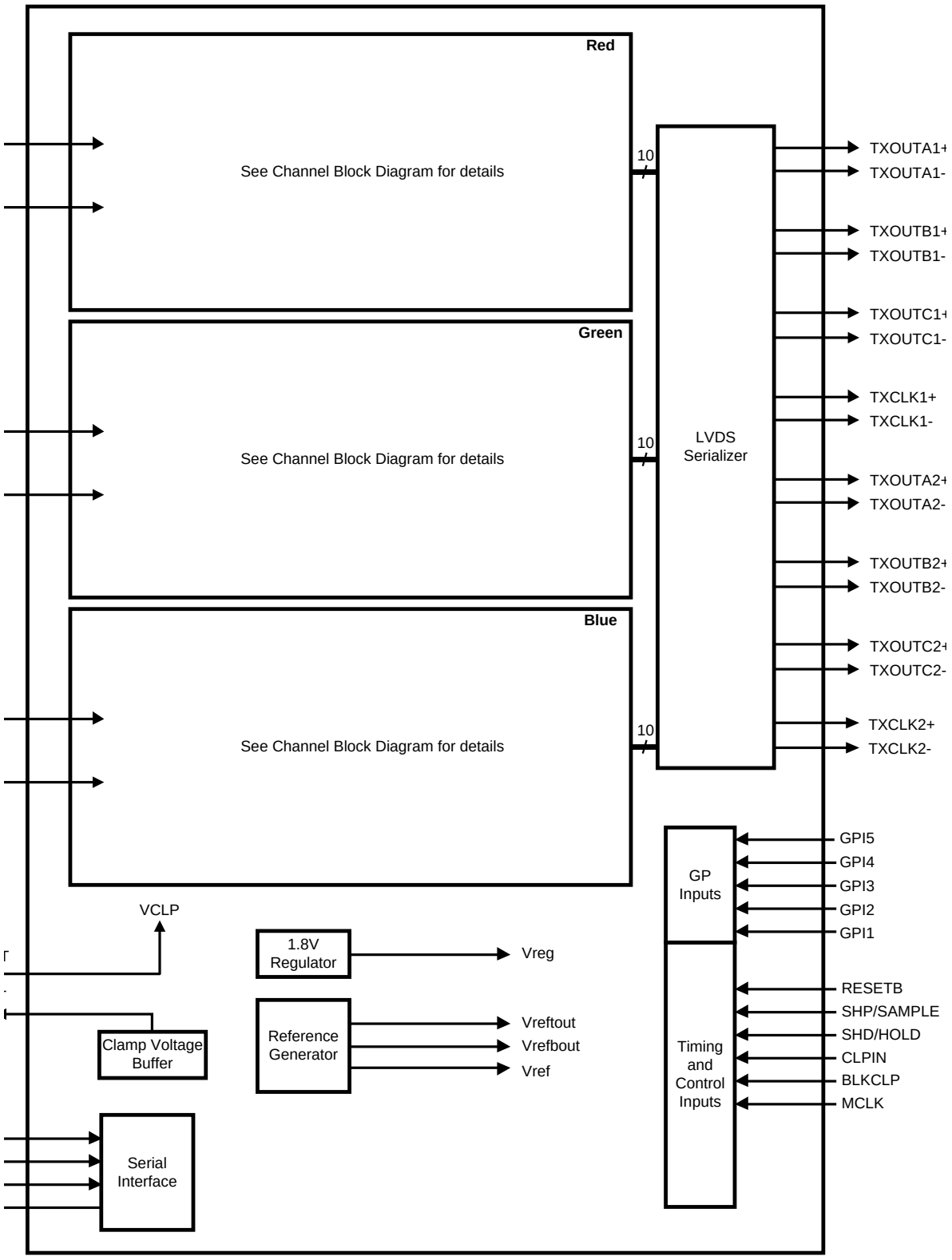
	VALUE	UNIT
Maximum Input Level	1.2 Vp-p (CDS gain = 1.0)	
	0.58 Vp-p (CDS gain = 2.0)	
Input Sample Rate	5 to 35 MSPS - 6ch mode	
	10 to 35 MSPS - 3ch mode	
PGA Gain Range	1x to 10x (0 to 20 dB)	
CDS/SH Gain Settings	1x or 2.1x	
Total Channel Gain	1x to 21x (0 to 26 dB)	
PGA Gain Resolution	8 bits - Analog	
ADC Resolution	10	bits
ADC Sampling Rate	10 to 70	MSPS
SNR	68.5 dB (Gain = 1x)	
Offset DAC Range	±111 mV or ±59.5 mV- FDAC	
	±281 mV - CDAC	
Offset DAC Resolution	±10 bits - FDAC	
	±4 bits - CDAC	
Supply voltage	3.0V to 3.6	V
Power Dissipation	1.02 W (typical)	

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

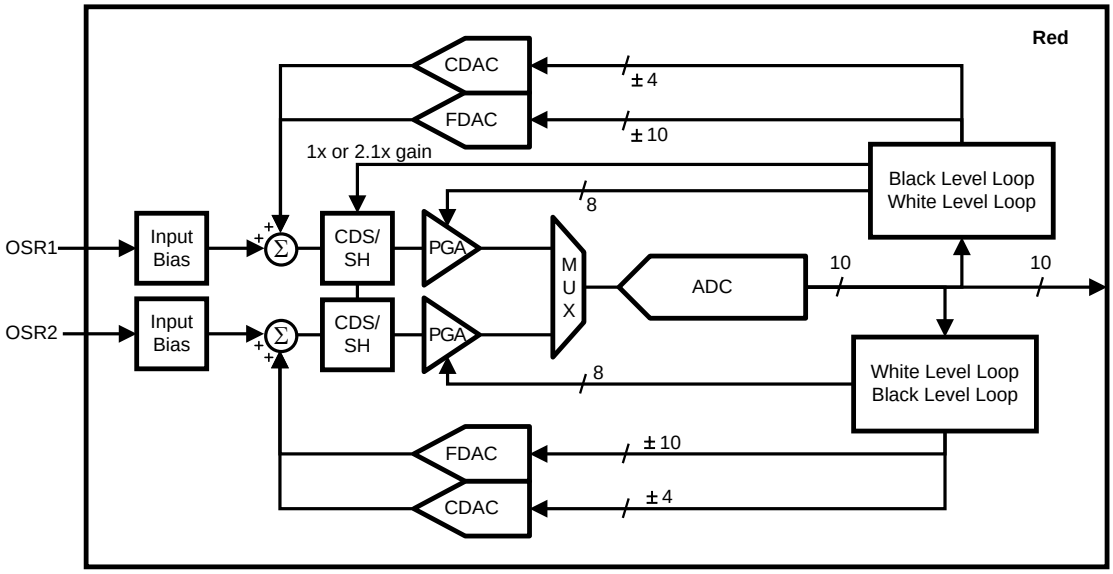
System Block Diagram



Chip Block Diagram



Channel Block Diagram



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM98620VHB/NOPB	ACTIVE	TQFP	PFC	80	119	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	0 to 70	LM98620VHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

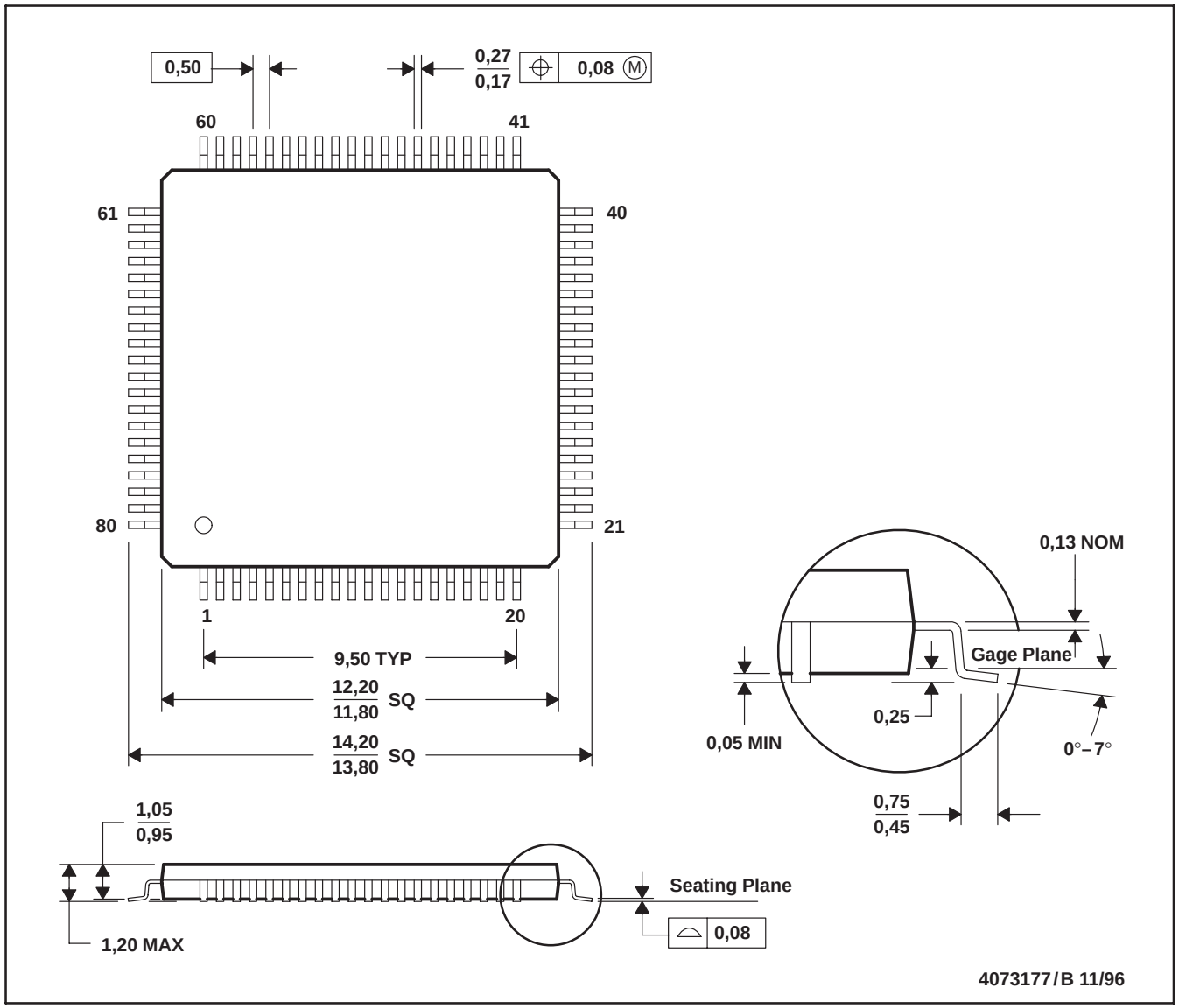
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

MTQF009A – OCTOBER 1994 – REVISED DECEMBER 1996

PFC (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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