Ordering number: EN4483



OVERVIEW

The LM7008M and LM7008HM are dual-PLL frequency synthesizer ICs for use in 250 to 380 MHz cordless telephone transceivers.

The LM7008M and LM7008HM comprise two PLL circuits, 16-bit transmit and receive programmable dividers, a crystal oscillator and two transistors for external lowpass filters (LPF). Each PLL comprises a dual charge pump and fast-lockup circuit. The standard crystal frequencies are 10.625 and 12.8 MHz. Serial data transfer is controlled from a three-wire, serial, computer control bus (C²B).

The LM7008M and LM7008HM operate from a 2.8 to 4.5 V supply and are available in 24-pin MFPs.

FEATURES

- Dual charge pump and fast-lockup circuit in each PLL for rapid locking
- 10.625 and 12.8 MHz crystal frequencies
- Crystal oscillator
- Dual LPF transistors
- C²B serial interface
- 2.8 to 4.5 V supply
- 24-pin MFP

PIN ASSIGNMENT



PACKAGE DIMENSIONS

Unit: mm

3112-MFP24S



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VBB	VSS	TVDD	CRT	
ate reverse bias	777			TEST
	Transmit-PLL programmable	16-bit divider	Transmit-PLL phase detector, charge pump, unlock detector and fast-lockup circuit	
	rence divider			
	1			
	Receive-PLL programmable	16-bit divider	Receive-PLL phase detector, charge pump. unlock detector and fast-lockup circuit	
C2B anface	L <u></u>			
	4θ-bit data shi and late	ft register ch	//	<u> </u>

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BLOCK DIAGRAM

PIN DESCRIPTION

Number	Name	Description			
1	PIR	Receive-PLL local-oscillator input			
2	RVDD	Receive PLL 2.8 to 4.5 V supply			
3	CRR	Receive-PLL fast-lockup circuit resistor and capacitor connection			
4	AOR	Receive-PLL LPF, n-channel MOS transistor output			
5	AIR	Receive-PLL LPF, n-channel MOS transistor input			
6	PDR1	Receive-PLL phase detector main tristate output			
7	PDR2	Receive-PLL phase detector secondary tristate output			
8	TEST	Test input			
9	XIN	Reference oscillator input			
10	XOUT	Reference oscillator output			
11	LDR	Receive-PLL unlock detector n-channel, open-drain output			
12	LDT	Transmit-PLL unlock detector n-channel, open-drain output			
13	DI	Serial data input			
14	CL	Clock input			
15	CE	Chip enable input			
16	VBB	Gate reverse-bias capacitor connection			

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Number	Name	Description	
17	PDT2	Transmit-PLL phase detector secondary tristate output	
18	PDT1	Transmit-PLL phase detector main tristate output	
19	AIT	Transmit-PLL LPF, n-channel MOS transistor input	
20	AOT	Transmit-PLL LPF, n-channel MOS transistor output	
21	CRT	Transmit-PLL fast-lockup circuit resistor and capacitor connection	
22	TVDD	Transmit-PLL 2.8 to 4.5 V supply	
23	PIT	Transmit-PLL local-oscillator input	
24	VSS 1	Ground	

SPECIFICATIONS

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Absolute Maximum Ratings

 $T_{a} = 25 C, V_{SS} = 0 V$

Parameter	Symbol	Rating	Unit
Receive-PLL supply voltage range	RVDD	0.3 to +5.5	v
Transmit-PLL supply voltage range	TVDD	-0.3 to +5.5	V
Gate reverse-bias voltage range	Vee	-4 to -1	V
XIN, TEST, PIR, PIT, AIR, AIT, CE, CL, DI, CRR and CRT input voltage range	VI	-0.3 to +6.0	v
XOUT, AOR, AOT, LDR, LDT, PDR1, PDR2, PDT1, PDT2, CRR and CRT output voltage range	Vo	-0.3 to +6.0	v
AOR, AOT, LDR and LDT output current range	lo	0 to 2	mA
Power dissipation	Po	350	mW
Operating temperature range	Topr	-20 to +75	°C
Storage temperature range	T _{stg}	-55 to +125	°C

Recommended Operating Conditions

T. = 25 °C

Parameter	Symbol	Rating	Unlt
Receive-PLL supply voltage range	RV _{DD}	2.8 to 4.5	v
Transmit-PLL supply voltage range	TV _{DD}	2.8 to 4.5	v

Electrical Characteristics

$V_{DD} = RV_{DD} = 7$	$\Gamma V_{DD} = 2.8$ to	4.5 V. V = $=$	$0 V. T_{2} = 25 °C$	unless otherwise noted

Paramete <i>r</i>	Symbol	Condition	, Rating			11-14
			min	typ	max	Onit
RVDD supply current	ICDI	LM7008M. See note 1.	-	18.5	24.5	mA
		LM7008HM. See note 1.	_	21.5	27.5	
RVDD + TVDD supply current		LM7008M. See note 2.	_	31.5	41.5	
	IDD2	LM7008MH. See note 2.	-	38.5	47.5	MA
CE, CL, DI, CRR and CRT LOW-level input voltage	ViL		0	-	0.4	v

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Parameter	Symbol	Condition		Unit		
Parameter	Symbol	Condition	min	typ	max	Unit
CE, CL, DI, CRR and CRT HIGH-level input voltage	ViH		2.0	-	5.5	V
	;	Sinewave, capacitive $coupling$, $f_1 = 200$ to 400 MHz	70	-	500	
PIR and PIT rms input voltage	Vn	Sinewave, capacitive coupling, V_{DD} = 2.8 to 3.3 V, f_1 = 200 to 520 MHz	100	-	500	mV
PDR1 and PDT1 LOW-level output voltage	V _{OL1}	lo = 0.1 mA	-	-	0.3	v
PDR2 and PDT2 LOW-level output voltage	VOL2	lo = 5 mA	-	-	1.5	V
EDR and EDT LOW-level output voltage	V _{OL3}	lo = 1 mA	-	-	1	v
CRR and CRT LOW-level output voltage	V _{OL4}	$l_0 = 2 \text{ mA}, V_{DD} = 3 \text{ V}$	0.7	1.0	1.4	v
AOR and AOT LOW-level output	V _{OL5}	$t_0 = 0.5 \text{ mA},$ $V_{AIR} = V_{AIT} = 1.2 \text{ V}$	-	-	0.5	M
voltage		$I_0 = 1 \text{ mA},$ $V_{AIR} = V_{AIT} = 1.3 \text{ V}$	-	-	0.5	•
PDR1 and PDT1 HIGH-level output voltage	VOHI	$l_0 = 0.1 \text{ mA}$	0.6V _{DD}	-	-	v
PDR2 and PDT2 HIGH-level output	Voue	1 ₀ = 0.1 mA	0.6V _{DD}		-	v
voltage	V OH2	l ₀ = 5 mA	0.1 V _{DD}	-	-	•
AOR, AOT, LDR, LDT, CRR and CRT output voltage	Vo		0	-	5.5	v
CE, CL, DI, CRR and CRT LOW-level input current	lici	V1 = 0 V	_	-	5	μА
XIN LOW-leve! input current	I	$V_1 = 0 V$	1		6	μА
PIR and PIT LOW-level input current	l _{IL3}	V ₁ = 0 V	2.	-	12	μΑ
AIR and AIT LOW-level input current	tila	V1 = 0 V	-	0.01	10.0	۸n
TEST LOW-level input current	IIL5	$V_{I} = 0 V$	-	_	5	μΑ
CE, CL, DI, CRR and CRT HIGH-level input current	lin1	V _i = 4.5 V	-	-	5	μA
XIN HIGH-level input current	liH2	$V_1 = 4.5 V$	1	-	6	μA
PIR and PIT HIGH-level input current	інз	$V_{1} = 4.5 V$	2	-	12	μΑ
AIR and AIT HIGH-level input current	liH4	V _I = 4.5 V	-	0.01	10.0	nA
TEST HIGH-level input current	Інь	V ₁ = 4.5 V	-	225	-	μA
LOR, LDT, CRR and CRT output leakage current	IOFF1	V _O = 4.5 V	-		5	μА
AOR and AOT output leakage current	OFF2	V _O = 4.5 V	-	-	10	μА
PDR1, PDT1, PDR2 and PDT2 output leakage current	IOFF3	$V_0 = 0.4 V \text{ or } 4.5 V$	-	0.01	10.0	nA

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Crystal oscillator frequency	İXTAL	Crystal impedance \leq 50 Ω	5	_	13	MHz

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Perometer	Symbol	Q	Rating			Fluit
r ai ai ne (e)	Symbol	Condition	min	typ	max	- Onin
PIR and PIT input frequency		Sinewave, capacitive coupling, $V_1 = 70 \text{ mV}$	200	-	400	
	fu :	Sinewave, capacitive coupling, $V_{DD} = 2.8$ to 3.2 V, $V_I = 100$ mV	200	- 520		MHz
XIN feedback resistance	Ru	V _{DD} = 4.5 V	750	1000	4500	kΩ
PIR and PIT feedback resistance	R _{f2}	V _{DD} = 4.5 V	375	500	2250	kΩ
TEST pull-down resistance	" Rp		-	20	-	kΩ
XIN, PIR and PIT input capacitance	Cı		-	2.5	-	pF

Notes

1. $f_{XIN} = 12.8$ MHz, $V_{PIR} = 70$ mV at 400 MHz, all other inputs = 0 V, all outputs open

2. $f_{XIN} = 12.8$ MHz, $V_{PIR} = V_{PIT} = 70$ mV at 400 MHz, all other inputs = 0 V, all outputs open

FUNCTIONAL DESCRIPTION

C²B Data Format

The C²B input data format is shown in figure 1, and the input timing, in figure 2. The input data comprises 48 bits input serially on DI. TD0 is the first bit received.



Figure 1. C²B data format

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Figure 2. Serial data timing

The timing diagram parameters t_i (t_1 , t_2 and t_3) should all be greater than $32/f_{XIN}$, where f_{XIN} is the XIN frequency. For XIN frequencies of 10.625 and 12.8 MHz, t_i should be greater than 3.02 and 2.5 µs, respectively.

The outputs are undefined until the frequency synthesizer is programmed. The serial data should be input only after RVDD and f_{XIN} have become stable. Note that CE, CL and DI HIGH-level and LOW-level voltages are independent of RVDD.

Reference Divider

Data bits FR0 to FR4 set the reference frequency divider ratio. The standard crystal oscillator input frequencies, f_{XIN} , are 12.8 and 10.625 MHz.

The reference divider ratios for $f_{ref} = 6.25$ kHz with 12.5 kHz channel spacing for f_{XIN} are shown in table 1.

Table) 1.	Reference	divider	ratios

f _{XIN} (MHz)	FR4	FR3	FR2	FR1	FR0	Divider ratio
12.8	0	0	0	0	0	2048
10.625	1	1	1	1	1	1700

Transmit- and Receive-PLL Programmable Dividers

Data bits TD0 to TD15 and RD0 to RD15 set the transmit- and receive-PLL programmable divider ratios, respectively. Bits TD0 and RD0 are the least significant bits.

The allowable divider ratios are in the range 256 to 65535. The PLL frequency divisions are two times the division setting of $f_{osc}/12.5$ kHz.

pulled down and PDT2 (PDR2) has the same output state as PDT1 (PDR1).

Table 2. Phase detector output states

Cone	PDT1 (PDR1)	
f _{IN} /N _T > f _{ref}	Leading	HIGH
f _{IN} /N _T < f _{ret}	Lagging	LOW
f _{IN} /NT = f _{ref}	Coincidence	High impedance

Unlock-detector Threshold

Data bits UD0 to UD2 determine the unlock-detector threshold. The PLL unlock-detector output, \overline{LDT} (\overline{LDR}), is pulled LOW when the phase error between the reference and the divided input, ϕ_E , exceeds the threshold. The threshold values for the standard frequencies are shown in table 3.

Table 3. Unlock-detector thresholds

UD2 UD1	1101	1100	Phase-error threshold (μs)		
	001	000	f _{XIN} = 12.8 MHz	f _{XIN} = 10.625 MHz	
0	0	0	0	0	
0	0	1	0.15	0.19	
0	1	0	0.3	Illegal	
0	1	1	lliegal	lilegal	
1	0	0	1.25	0.94 ±0.19	
1	0	1	1.25	0.94 ±0.19	
1	1	0	5	4.70 ±0.94	
1	1	1	5	4.70 ±0.94	

Phase Detector

The phase detector output states of PDT1 (PDR1) are shown in table 2. When the PLL unlocks, $\overline{\text{LDT}}$ ($\overline{\text{LDR}}$) is

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Unlock Extension

Data bit UE selects the unlock extension period. The period is extended by 2.5 ms, when UE = 0, and by 5 ms, when UE = 1, as shown in figure 3. The unlock extension is ignored when UD0 = UD1 = UD2 = 0.



Figure 3. Unlock extension

Dead-zone Mode

Data bits DZ0 and DZ1 select the phase-insensitive bandwidth, or dead zone, of the PLL phase comparator as shown in table 4. Modes DZB, DZC and DZD have successively larger dead zones.

Table 4. Dead-zone modes

DZ1	DZ0	Dead-zone mode
0	0	lliegal
0	1	DZB
1	0	DZC
1	1	DZD

Fast-lockup Control

Data bits HST and HSR select fast-lockup mode for the transmit and receive PLLs, respectively. Fast-lockup mode is selected when each data bit is 1, and deselected, when 0.

Data bit HSM selects the fast-lockup operating mode as shown in figure 4. Fast-lockup operates continuously,

when HSM = 1, and during unlock only, when HSM = 0.





When fast lockup is not selected, CRT and CRR should be either open or tied to ground.

Power Supply

TVDD supplies the transmit-PLL programmable divider, phase detector, unlock detector and fast-lockup circuits. RVDD supplies the C²B interface, reference divider and receive-PLL circuits.

LPF Transistors

Open-drain transistors are provided for the transmit- and receive-PLL loop filters.

Test Mode (T0, T1)

Data bits T0 and T1 are normally not used and should be set to 0. Also, TEST should be open or tied to ground.

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DESIGN INFORMATION

Dual Charge Pump and Fast-lockup Circuit

The dual charge pump and fast-lockup circuit is shown in figure 5. The phase detector secondary output goes active after a channel change causes the PLL to unlock. R1 becomes R1MIR1S, reducing the LPF time constant and decreasing the PLL lock time. When the PLL locks, the phase detector secondary output becomes high impedance and R1 becomes R1M, thereby increasing the LPF time constant and improving sideband and FM response.



Figure 5. Dual charge pump and fast-lockup circuit

Phase-error Threshold

Gate Reverse Bias

The phase-error threshold should be small during channel change to ensure precise phase-error checking and phase-detector secondary output operation. Unlocking caused by phase error is unlikely during FM operation. The phase-error threshold should be large after the PLL locks.

A 0.01 μ F capacitor should be connected between VBB and ground for the gate reverse bias.

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