

## LM5111 Dual 5A Compound Gate Driver

Check for Samples: [LM5111](#)

### FEATURES

- Independently Drives Two N-Channel MOSFETs
- Compound CMOS and Bipolar Outputs Reduce Output Current Variation
- 5A Sink/3A Source Current Capability
- Two Channels can be Connected in Parallel to Double the Drive Current
- Independent Inputs (TTL Compatible)
- Fast Propagation Times (25 ns Typical)
- Fast Rise and Fall Times (14 ns/12 ns Rise/Fall with 2 nF Load)
- Available in Dual Non-Inverting, Dual Inverting and Combination Configurations
- Supply Rail Under-Voltage Lockout Protection (UVLO)
- LM5111-4 UVLO Configured to Drive PFET through OUT\_A and NFET through OUT\_B
- Pin Compatible with Industry Standard Gate Drivers

### DESCRIPTION

The LM5111 Dual Gate Driver replaces industry standard gate drivers with improved peak output current and efficiency. Each “compound” output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 5A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Under-voltage lockout protection is also provided. The drivers can be operated in parallel with inputs and outputs connected to double the drive current capability. This device is available in the SOIC package or the thermally enhanced VSSOP package.

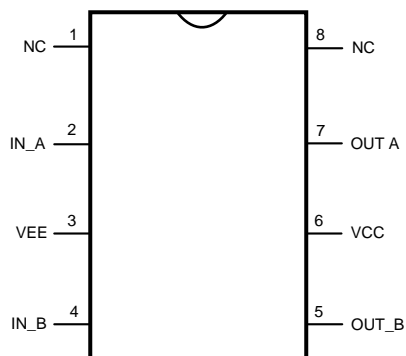
### TYPICAL APPLICATIONS

- Synchronous Rectifier Gate Drivers
- Switch-mode Power Supply Gate Driver
- Solenoid and Motor Drivers

### PACKAGES

- SOIC
- Thermally Enhanced VSSOP

### CONNECTION DIAGRAM



**Figure 1. 8-Lead SOIC or VSSOP  
See D or DGN0008A Package**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

### PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	NC	No Connect	
2	IN_A	'A' side control input	TTL compatible thresholds.
3	VEE	Ground reference for both inputs and outputs	Connect to power ground.
4	IN_B	'B' side control input	TTL compatible thresholds.
5	OUT_B	Output for the 'B' side driver.	Voltage swing of this output is from VCC to VEE. The output stage is capable of sourcing 3A and sinking 5A.
6	VCC	Positive output supply	Locally decouple to VEE.
7	OUT_A	Output for the 'A' side driver.	Voltage swing of this output is from VCC to VEE. The output stage is capable of sourcing 3A and sinking 5A.
8	NC	No Connect	
		EP (VSSOP Package)	It is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PC board to aid thermal dissipation.

### Configuration Table

Part Number	"A" Output Configuration	"B" Output Configuration	Package
LM5111-1M/-1MX/-1MY/-1MYX	Non-Inverting (Low in UVLO)	Non-Inverting (Low in UVLO)	SOIC, VSSOP
LM5111-2M/-2MX/-2MY/-2MYX	Inverting (Low in UVLO)	Inverting (Low in UVLO)	SOIC, VSSOP
LM5111-3M/-3MX/-3MY/-3MYX	Inverting (Low in UVLO)	Non-Inverting (Low in UVLO)	SOIC, VSSOP
LM5111-4M/-4MX/-4MY/-4MYX	Inverting (High in UVLO)	Non-Inverting (Low in UVLO)	SOIC, VSSOP



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

$V_{CC}$ to $V_{EE}$	-0.3V to 15V
IN to $V_{EE}$	-0.3V to 15V
Storage Temperature Range, ( $T_{STG}$ )	-55°C to +150°C
Maximum Junction Temperature, ( $T_{J(max)}$ )	+150°C
Operating Junction Temperature	+125°C
ESD Rating	2kV

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the [Electrical Characteristics](#).
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

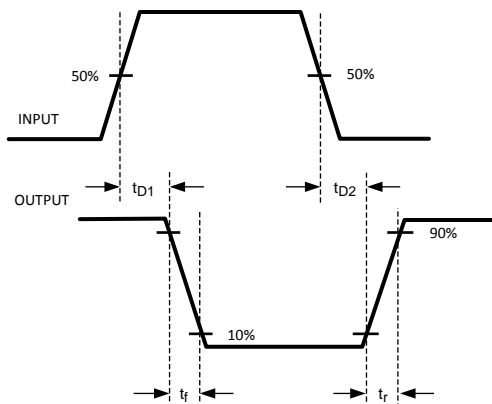
## Electrical Characteristics

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC} = 12\text{V}$ ,  $V_{EE} = 0\text{V}$ , No Load on OUT\_A or OUT\_B, unless otherwise specified.

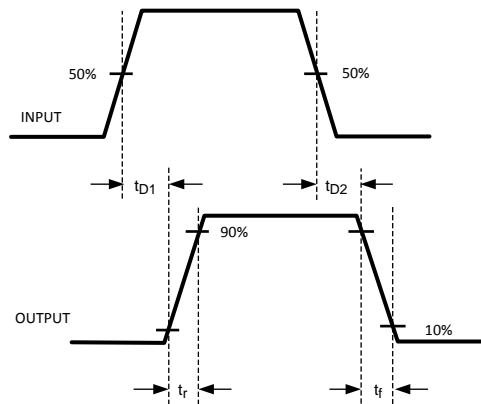
Symbol	Parameter	Conditions	Min	Typ	Max	Units
	$V_{CC}$ Operating Range	$V_{CC}-V_{EE}$	3.5		14	V
$V_{CCR}$	$V_{CC}$ Under Voltage Lockout (rising)	$V_{CC}-V_{EE}$	2.3	2.9	3.5	V
$V_{CCH}$	$V_{CC}$ Under Voltage Lockout Hysteresis			230		mV
$I_{CC}$	$V_{CC}$ Supply Current ( $I_{CC}$ )	IN_A = IN_B = 0V (5111-1)		1	2	mA
		IN_A = IN_B = $V_{CC}$ (5111-2)		1	2	
		IN_A = $V_{CC}$ , IN_B = 0V (5111-3)		1	2	
<b>CONTROL INPUTS</b>						
$V_{IH}$	Logic High		2.2			V
$V_{IL}$	Logic Low				0.8	V
$V_{thH}$	High Threshold		1.3	1.75	2.2	V
$V_{thL}$	Low Threshold		0.8	1.35	2.0	V
HYS	Input Hysteresis			400		mV
$I_{IL}$	Input Current Low	IN_A=IN_B= $V_{CC}$ (5111-1-2-3)	-1	0.1	1	$\mu\text{A}$
$I_{IH}$	Input Current High	IN_B= $V_{CC}$ (5111-3)	10	18	25	
		IN_A=IN_B= $V_{CC}$ (5111-2)	-1	0.1	1	
		IN_A=IN_B= $V_{CC}$ (5111-1)	10	18	25	
		IN_A= $V_{CC}$ (5111-3)	-1	0.1	1	
<b>OUTPUT DRIVERS</b>						
$R_{OH}$	Output Resistance High	$I_{OUT} = -10\text{ mA}^{(1)}$		30	50	$\Omega$
$R_{OL}$	Output Resistance Low	$I_{OUT} = +10\text{ mA}^{(1)}$		1.4	2.5	$\Omega$
$I_{Source}$	Peak Source Current	OUTA/OUTB = $V_{CC}/2$ , 200 ns Pulsed Current		3		A
$I_{Sink}$	Peak Sink Current	OUTA/OUTB = $V_{CC}/2$ , 200 ns Pulsed Current		5		A
<b>SWITCHING CHARACTERISTICS</b>						
td1	Propagation Delay Time Low to High, IN rising (IN to OUT)	$C_{LOAD} = 2\text{ nF}$ See <a href="#">Figure 2</a> and <a href="#">Figure 3</a>		25	40	ns
td2	Propagation Delay Time High to Low, IN falling (IN to OUT)	$C_{LOAD} = 2\text{ nF}$ See <a href="#">Figure 2</a> and <a href="#">Figure 3</a>		25	40	ns
$t_r$	Rise Time	$C_{LOAD} = 2\text{ nF}$ See <a href="#">Figure 2</a> and <a href="#">Figure 3</a>		14	25	ns
$t_f$	Fall Time	$C_{LOAD} = 2\text{ nF}$ See <a href="#">Figure 2</a> and <a href="#">Figure 3</a>		12	25	ns
<b>LATCHUP PROTECTION</b>						
	AEC - Q100, Method 004	$T_J = 150^{\circ}\text{C}$		500		mA
<b>THERMAL RESISTANCE</b>						
$\theta_{JA}$	Junction to Ambient, 0 LFPM Air Flow	SOIC Package VSSOP Package		170 60		$^{\circ}\text{C/W}$
$\theta_{JC}$	Junction to Case	SOIC Package VSSOP Package		70 4.7		$^{\circ}\text{C/W}$

(1) The output resistance specification applies to the MOS device only. The total output current capability is the sum of the MOS and Bipolar devices.

### Timing Waveforms



**Figure 2. Inverting**



**Figure 3. Non-Inverting**

Typical Performance Characteristics

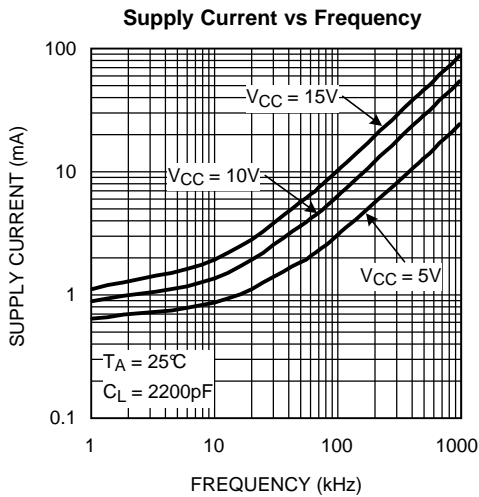


Figure 4.

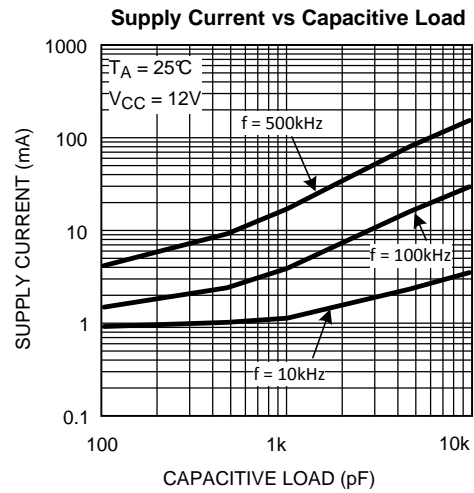


Figure 5.

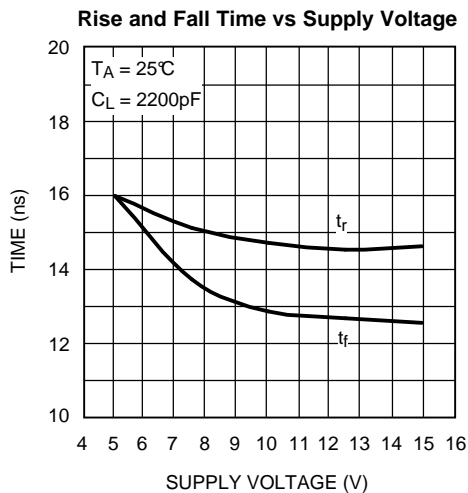


Figure 6.

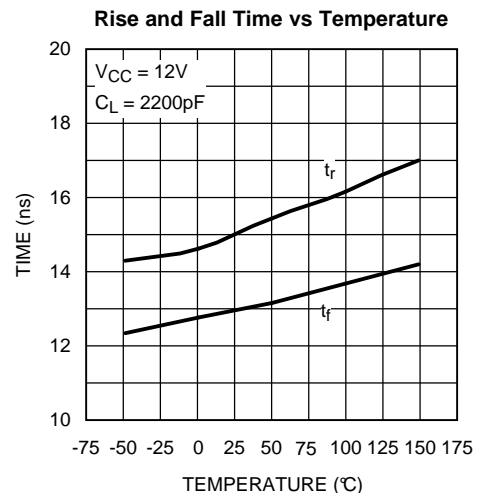


Figure 7.

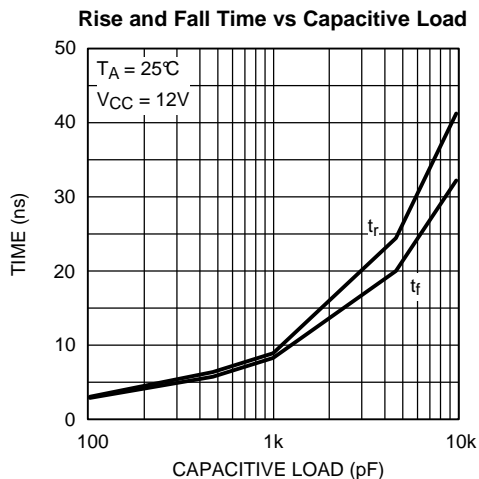


Figure 8.

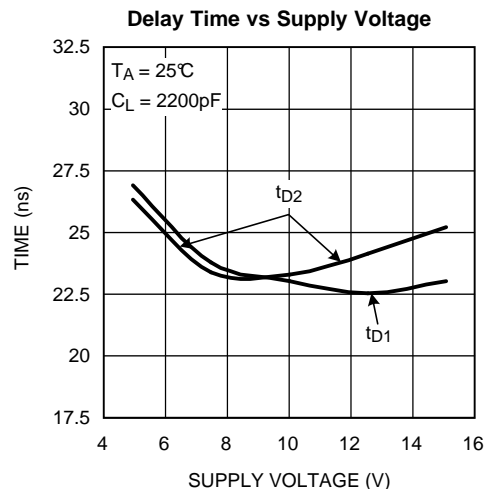


Figure 9.

**Typical Performance Characteristics (continued)**

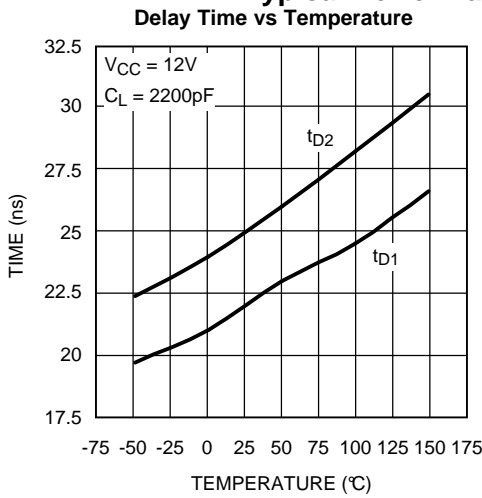


Figure 10.

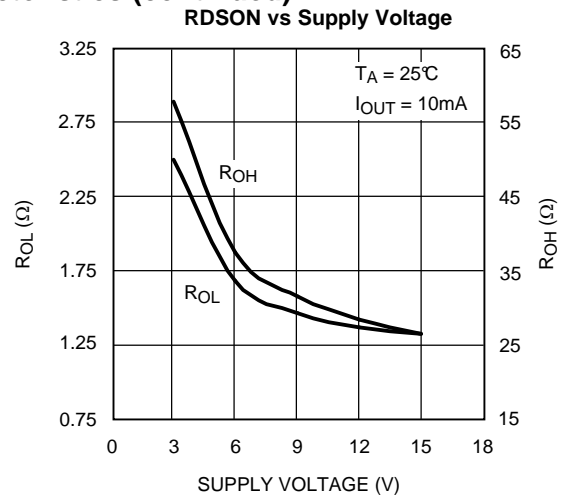


Figure 11.

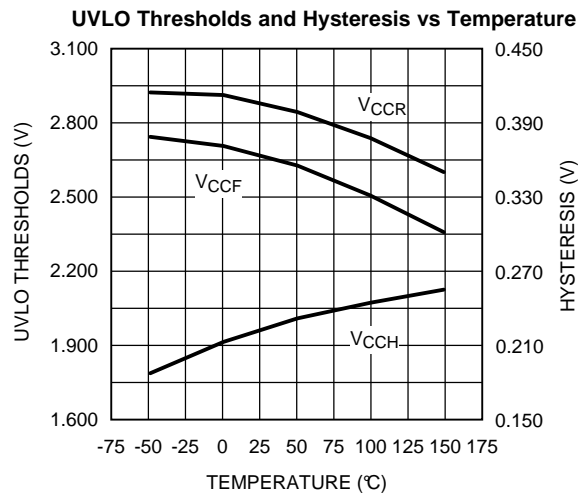


Figure 12.

### Block Diagram

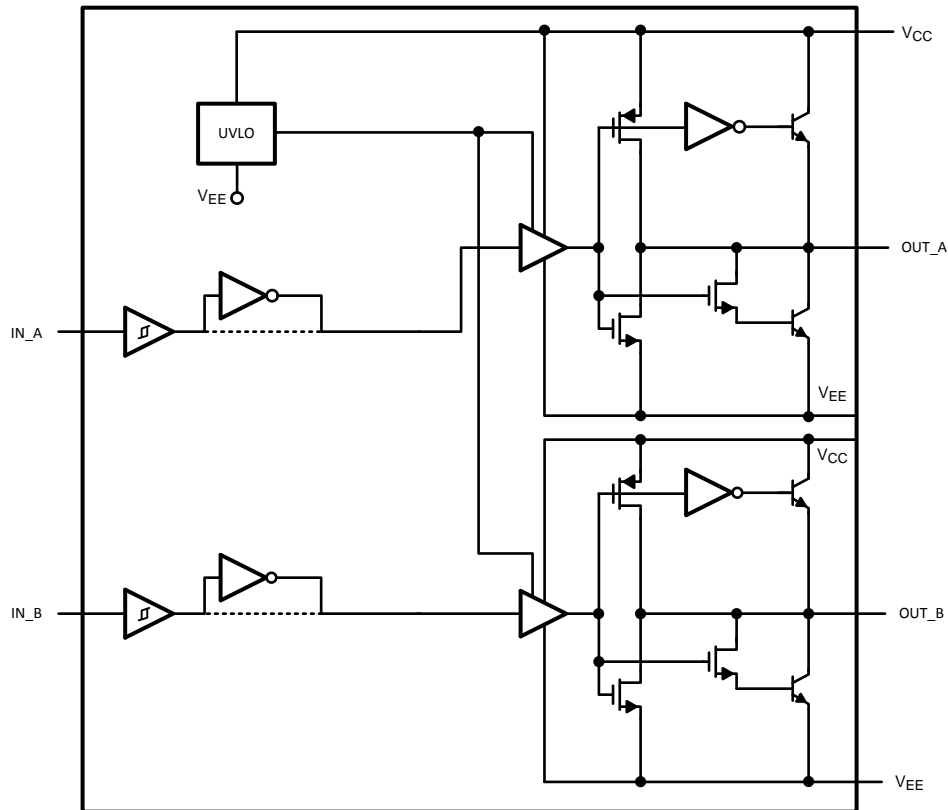


Figure 13. Block Diagram of LM5111

### Detailed Operating Description

LM5111 dual gate driver consists of two independent and identical driver channels with TTL compatible logic inputs and high current totem-pole outputs that source or sink current to drive MOSFET gates. The driver output consist of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical threshold region of the MOSFET VGS while the MOS devices provide rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage  $V_{CC}$  and the power ground potential at the  $V_{EE}$  pin.

The control inputs of the drivers are high impedance CMOS buffers with TTL compatible threshold voltages. The LM5111 pinout was designed for compatibility with industry standard gate drivers in single supply gate driver applications.

The input stage of each driver should be driven by a signal with a short rise and fall time. Slow rising and falling input signals, although not harmful to the driver, may result in the output switching repeatedly at a high frequency.

The two driver channels of the LM5111 are designed as identical cells. Transistor matching inherent to integrated circuit manufacturing ensures that the AC and DC performance of the channels are nearly identical. Closely matched propagation delays allow the dual driver to be operated as a single with inputs and output pins connected. The drive current capability in parallel operation is precisely 2X the drive of an individual channel. Small differences in switching speed between the driver channels will produce a transient current (shoot-through) in the output stage when two output pins are connected to drive a single load. Differences in input thresholds

between the driver channels will also produce a transient current (shoot-through) in the output stage. Fast transition input signals are especially important while operating in a parallel configuration. The efficiency loss for parallel operation has been characterized at various loads, supply voltages and operating frequencies. The power dissipation in the LM5111 increases by less than 1% relative to the dual driver configuration when operated as a single driver with inputs/ outputs connected.

An Under Voltage Lock Out (UVLO) circuit is included in the LM5111, which senses the voltage difference between  $V_{CC}$  and the chip ground pin,  $V_{EE}$ . When the  $V_{CC}$  to  $V_{EE}$  voltage difference falls below 2.8V both driver channels are disabled. The UVLO hysteresis prevents chattering during brown-out conditions and the driver will resume normal operation when the  $V_{CC}$  to  $V_{EE}$  differential voltage exceeds approximately 3.0V.

The LM5111-1, -2 and -3 devices hold both outputs in the low state in the under-voltage lockout (UVLO) condition. The LM5111-4 is distinguished from the LM5111-3 by the active high output state of OUT\_A during UVLO. When  $V_{CC}$  is less than the UVLO threshold voltage, OUT\_A of the LM5111-4 will be locked in the high state while OUT\_B will be disabled in the low state. This configuration allows the LM5111-4 to drive a PFET through OUT\_A and an NFET through OUT\_B with both FETs safely turned off during UVLO.

The LM5111 is available in dual non-inverting (-1), dual Inverting (-2) and the combination inverting plus non-inverting (-3, -4) configurations. All configurations are offered in the SOIC and VSSOP plastic packages.

## Layout Considerations

Attention must be given to board layout when using LM5111. Some important considerations include:

1. A Low ESR/ESL capacitor must be connected close to the IC and between the  $V_{CC}$  and  $V_{EE}$  pins to support high peak currents being drawn from  $V_{CC}$  during turn-on of the MOSFET.
2. Proper grounding is crucial. The drivers need a very low impedance path for current return to ground avoiding inductive loops. The two paths for returning current to ground are a) between LM5111  $V_{EE}$  pin and the ground of the circuit that controls the driver inputs, b) between LM5111  $V_{EE}$  pin and the source of the power MOSFET being driven. All these paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance. All these ground paths should be kept distinctly separate to avoid coupling between the high current output paths and the logic signals that drive the LM5111. A good method is to dedicate one copper plane in a multi-layered PCB to provide a common ground surface.
3. With the rise and fall times in the range of 10 ns to 30 ns, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated by the LM5111.
4. The LM5111 footprint is compatible with other industry standard drivers including the TC4426/27/28 and UCC27323/4/5.
5. If either channel is not being used, the respective input pin (IN\_A or IN\_B) should be connected to either  $V_{EE}$  or  $V_{CC}$  to avoid spurious output signals.

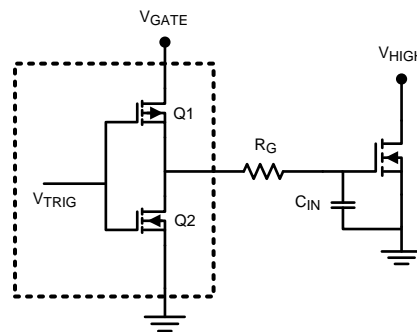
## Thermal Performance

### INTRODUCTION

The primary goal of thermal management is to maintain the integrated circuit (IC) junction temperature ( $T_J$ ) below a specified maximum operating temperature to ensure reliability. It is essential to estimate the maximum  $T_J$  of IC components in worst case operating conditions. The junction temperature is estimated based on the power dissipated in the IC and the junction to ambient thermal resistance  $\theta_{JA}$  for the IC package in the application board and environment. The  $\theta_{JA}$  is not a given constant for the package and depends on the printed circuit board design and the operating environment.

### DRIVE POWER REQUIREMENT CALCULATIONS IN LM5111

The LM5111 dual low side MOSFET driver is capable of sourcing/sinking 3A/5A peak currents for short intervals to drive a MOSFET without exceeding package power dissipation limits. High peak currents are required to switch the MOSFET gate very quickly for operation at high frequencies.



The schematic above shows a conceptual diagram of the LM5111 output and MOSFET load. Q1 and Q2 are the switches within the gate driver.  $R_G$  is the gate resistance of the external MOSFET, and  $C_{IN}$  is the equivalent gate capacitance of the MOSFET. The gate resistance  $R_G$  is usually very small and losses in it can be neglected. The equivalent gate capacitance is a difficult parameter to measure since it is the combination of  $C_{GS}$  (gate to source capacitance) and  $C_{GD}$  (gate to drain capacitance). Both of these MOSFET capacitances are not constants and vary with the gate and drain voltage. The better way of quantifying gate capacitance is the total gate charge  $Q_G$  in coulombs.  $Q_G$  combines the charge required by  $C_{GS}$  and  $C_{GD}$  for a given gate drive voltage  $V_{GATE}$ .

Assuming negligible gate resistance, the total power dissipated in the MOSFET driver due to gate charge is approximated by

$$P_{DRIVER} = V_{GATE} \times Q_G \times F_{SW}$$

where

- $F_{SW}$  = switching frequency of the MOSFET (1)

For example, consider the MOSFET MTD6N15 whose gate charge specified as 30 nC for  $V_{GATE} = 12V$ .

The power dissipation in the driver due to charging and discharging of MOSFET gate capacitances at switching frequency of 300 kHz and  $V_{GATE}$  of 12V is equal to

$$P_{DRIVER} = 12V \times 30 \text{ nC} \times 300 \text{ kHz} = 0.108W. \quad (2)$$

If both channels of the LM5111 are operating at equal frequency with equivalent loads, the total losses will be twice as this value which is 0.216W.

In addition to the above gate charge power dissipation, - transient power is dissipated in the driver during output transitions. When either output of the LM5111 changes state, current will flow from  $V_{CC}$  to  $V_{EE}$  for a very brief interval of time through the output totem-pole N and P channel MOSFETs. The final component of power dissipation in the driver is the power associated with the quiescent bias current consumed by the driver input stage and Under-voltage lockout sections.

Characterization of the LM5111 provides accurate estimates of the transient and quiescent power dissipation components. At 300 kHz switching frequency and 30 nC load used in the example, the transient power will be 8 mW. The 1 mA nominal quiescent current and 12V  $V_{GATE}$  supply produce a 12 mW typical quiescent power.

Therefore the total power dissipation

$$P_D = 0.216 + 0.008 + 0.012 = 0.236W. \quad (3)$$

We know that the junction temperature is given by

$$T_J = P_D \times \theta_{JA} + T_A \quad (4)$$

Or the rise in temperature is given by

$$T_{RISE} = T_J - T_A = P_D \times \theta_{JA} \quad (5)$$

For SOIC package,  $\theta_{JA}$  is estimated as 170°C/W for the conditions of natural convection. For VSSOP,  $\theta_{JA}$  is typically 60°C/W.

Therefore for SOIC  $T_{RISE}$  is equal to

$$T_{RISE} = 0.236 \times 170 = 40.1^\circ\text{C} \quad (6)$$

### CONTINUOUS CURRENT RATING OF LM5111

The LM5111 can deliver pulsed source/sink currents of 3A and 5A to capacitive loads. In applications requiring continuous load current (resistive or inductive loads), package power dissipation, limits the LM5111 current capability far below the 5A sink/3A source capability. Rated continuous current can be estimated both when sourcing current to or sinking current from the load. For example when sinking, the maximum sink current can be calculated as:

$$I_{SINK (MAX)} := \sqrt{\frac{T_J(MAX) - T_A}{\theta_{JA} \cdot R_{DS (ON)}}$$

where

- $R_{DS(on)}$  is the on resistance of lower MOSFET in the output stage of LM5111 (7)

Consider  $T_J(max)$  of 125°C and  $\theta_{JA}$  of 170°C/W for an SO-8 package under the condition of natural convection and no air flow. If the ambient temperature ( $T_A$ ) is 60°C, and the  $R_{DS(on)}$  of the LM5111 output at  $T_J(max)$  is 2.5Ω, this equation yields  $I_{SINK(max)}$  of 391mA which is much smaller than 5A peak pulsed currents.

Similarly, the maximum continuous source current can be calculated as

$$I_{SOURCE (MAX)} := \frac{T_J(MAX) - T_A}{\theta_{JA} \cdot V_{DIODE}}$$

where

- $V_{DIODE}$  is the voltage drop across hybrid output stage which varies over temperature and can be assumed to be about 1.1V at  $T_J(max)$  of 125°C (8)

Assuming the same parameters as above, this equation yields  $I_{SOURCE(max)}$  of 347mA.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM5111-1M	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	5111 -1M	<a href="#">Samples</a>
LM5111-1M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -1M	<a href="#">Samples</a>
LM5111-1MX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	5111 -1M	<a href="#">Samples</a>
LM5111-1MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -1M	<a href="#">Samples</a>
LM5111-1MY	ACTIVE	MSOP- PowerPAD	DGN	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM		SJKB	<a href="#">Samples</a>
LM5111-1MY/NOPB	ACTIVE	MSOP- PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJKB	<a href="#">Samples</a>
LM5111-1MYX	ACTIVE	MSOP- PowerPAD	DGN	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM		SJKB	<a href="#">Samples</a>
LM5111-1MYX/NOPB	ACTIVE	MSOP- PowerPAD	DGN	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJKB	<a href="#">Samples</a>
LM5111-2M	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	5111 -2M	<a href="#">Samples</a>
LM5111-2M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -2M	<a href="#">Samples</a>
LM5111-2MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -2M	<a href="#">Samples</a>
LM5111-2MY	ACTIVE	MSOP- PowerPAD	DGN	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM		SJLB	<a href="#">Samples</a>
LM5111-2MY/NOPB	ACTIVE	MSOP- PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJLB	<a href="#">Samples</a>
LM5111-2MYX	ACTIVE	MSOP- PowerPAD	DGN	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM		SJLB	<a href="#">Samples</a>
LM5111-2MYX/NOPB	ACTIVE	MSOP- PowerPAD	DGN	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJLB	<a href="#">Samples</a>
LM5111-3M	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	5111 -3M	<a href="#">Samples</a>
LM5111-3M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -3M	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM5111-3MX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	5111 -3M	<a href="#">Samples</a>
LM5111-3MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -3M	<a href="#">Samples</a>
LM5111-3MY	ACTIVE	MSOP- PowerPAD	DGN	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM		SJNB	<a href="#">Samples</a>
LM5111-3MY/NOPB	ACTIVE	MSOP- PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJNB	<a href="#">Samples</a>
LM5111-3MYX	ACTIVE	MSOP- PowerPAD	DGN	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM		SJNB	<a href="#">Samples</a>
LM5111-3MYX/NOPB	ACTIVE	MSOP- PowerPAD	DGN	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJNB	<a href="#">Samples</a>
LM5111-4M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5111 -4M	<a href="#">Samples</a>
LM5111-4MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5111 -4M	<a href="#">Samples</a>
LM5111-4MY/NOPB	ACTIVE	MSOP- PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SSYB	<a href="#">Samples</a>
LM5111-4MYX/NOPB	ACTIVE	MSOP- PowerPAD	DGN	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SSYB	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

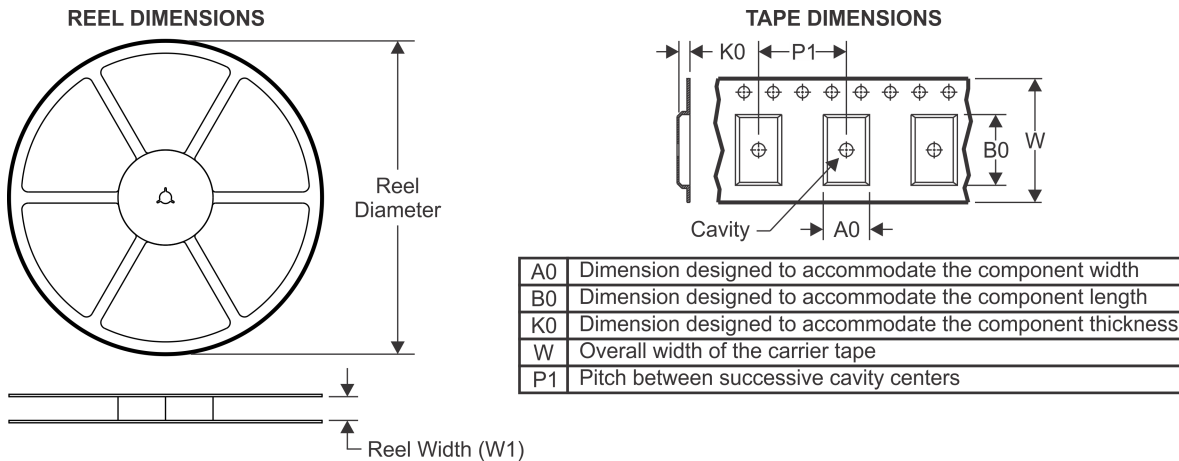
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5111-1MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-1MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-1MY	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-1MY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-1MYX	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-1MYX/NOPB	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-2MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-2MY	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-2MY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-2MYX	MSOP-	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

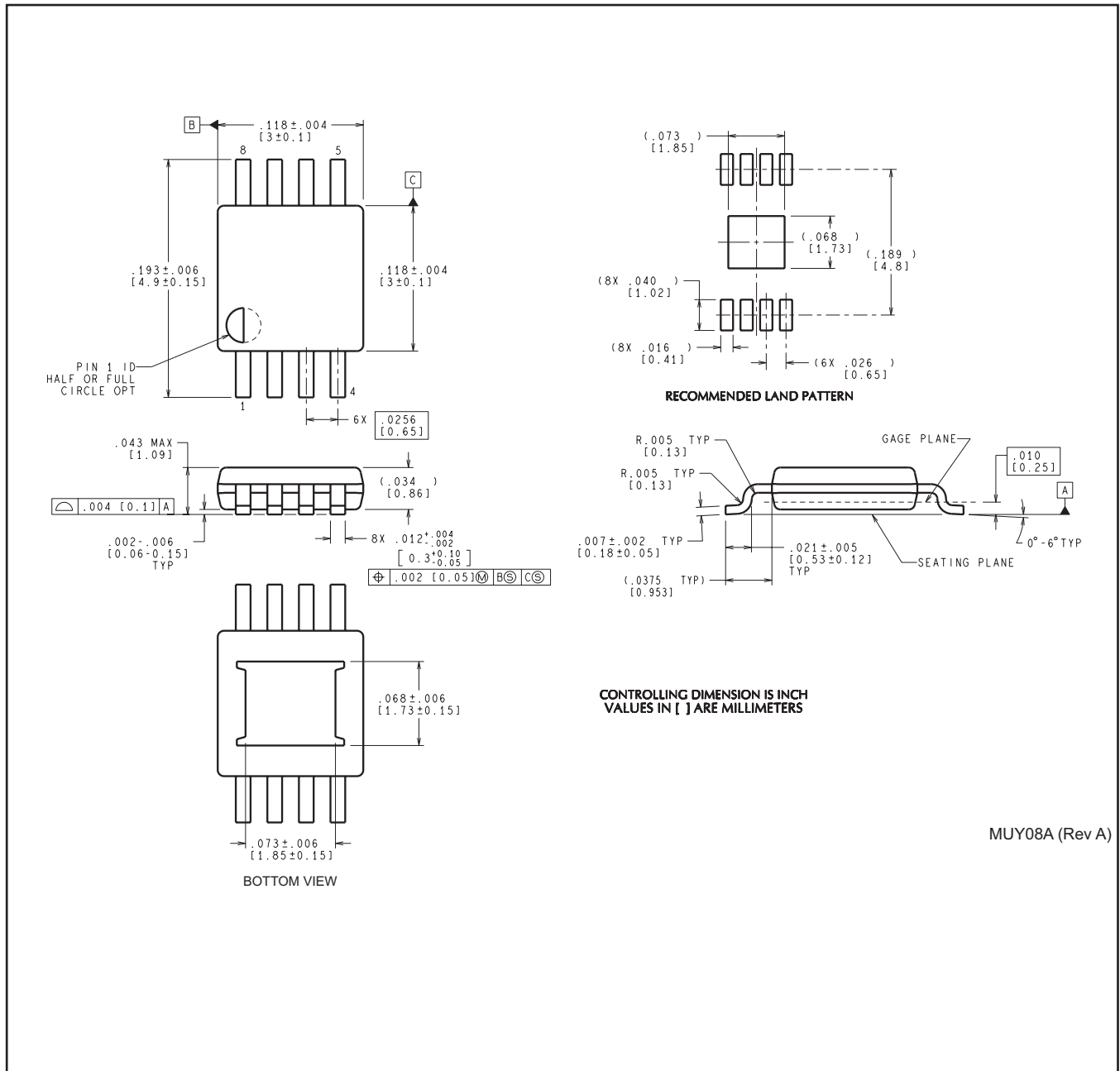
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	Power PAD											
LM5111-2MYX/NOPB	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-3MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-3MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-3MY	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-3MY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-3MYX	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-3MYX/NOPB	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-4MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-4MY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-4MYX/NOPB	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5111-1MX	SOIC	D	8	2500	349.0	337.0	45.0
LM5111-1MX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LM5111-1MY	MSOP-PowerPAD	DGN	8	1000	203.0	190.0	41.0
LM5111-1MY/NOPB	MSOP-PowerPAD	DGN	8	1000	203.0	190.0	41.0
LM5111-1MYX	MSOP-PowerPAD	DGN	8	3500	349.0	337.0	45.0
LM5111-1MYX/NOPB	MSOP-PowerPAD	DGN	8	3500	349.0	337.0	45.0
LM5111-2MX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LM5111-2MY	MSOP-PowerPAD	DGN	8	1000	203.0	190.0	41.0
LM5111-2MY/NOPB	MSOP-PowerPAD	DGN	8	1000	203.0	190.0	41.0
LM5111-2MYX	MSOP-PowerPAD	DGN	8	3500	349.0	337.0	45.0
LM5111-2MYX/NOPB	MSOP-PowerPAD	DGN	8	3500	349.0	337.0	45.0
LM5111-3MX	SOIC	D	8	2500	349.0	337.0	45.0
LM5111-3MX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LM5111-3MY	MSOP-PowerPAD	DGN	8	1000	203.0	190.0	41.0
LM5111-3MY/NOPB	MSOP-PowerPAD	DGN	8	1000	203.0	190.0	41.0
LM5111-3MYX	MSOP-PowerPAD	DGN	8	3500	349.0	337.0	45.0
LM5111-3MYX/NOPB	MSOP-PowerPAD	DGN	8	3500	349.0	337.0	45.0
LM5111-4MX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LM5111-4MY/NOPB	MSOP-PowerPAD	DGN	8	1000	203.0	190.0	41.0
LM5111-4MYX/NOPB	MSOP-PowerPAD	DGN	8	3500	349.0	337.0	45.0

DGN0008A



MUY08A (Rev A)



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)